JD79653A

Rev. 0.01

DATA SHEET

All-in-one driver with TCON for Color application

fitipower integrated technology Inc.

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All-in-one driver with TCON for Color application

1. GENERAL DESCRIPTION

This driver is an all-in-one driver with timing controller for color application. The outputs have 1-bit white/black and 1-bit red resolution output per pixel. The timing controller provides control signals for the source driver and gate drivers.

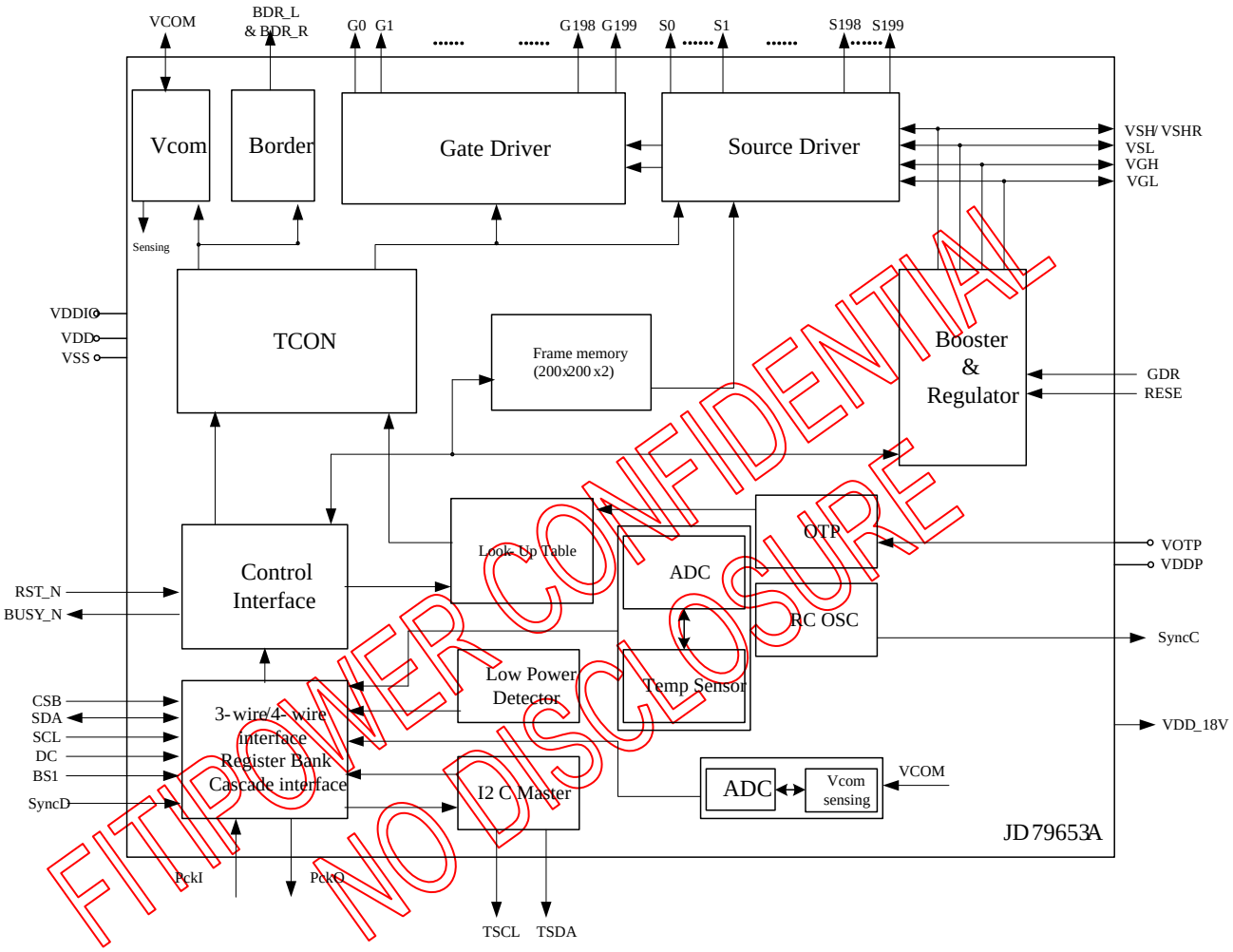
*The DC-DC controller allows to generate the source ou*tput voltage VSH/VSL (+/-6.4V~+/-15V). The chip also includes an output buffer for the supply of the common electrode (VCOMAC or VCOMDC). The system is configurable through a 3-wire/4-wire (SPI) serial.

2. FEATURES

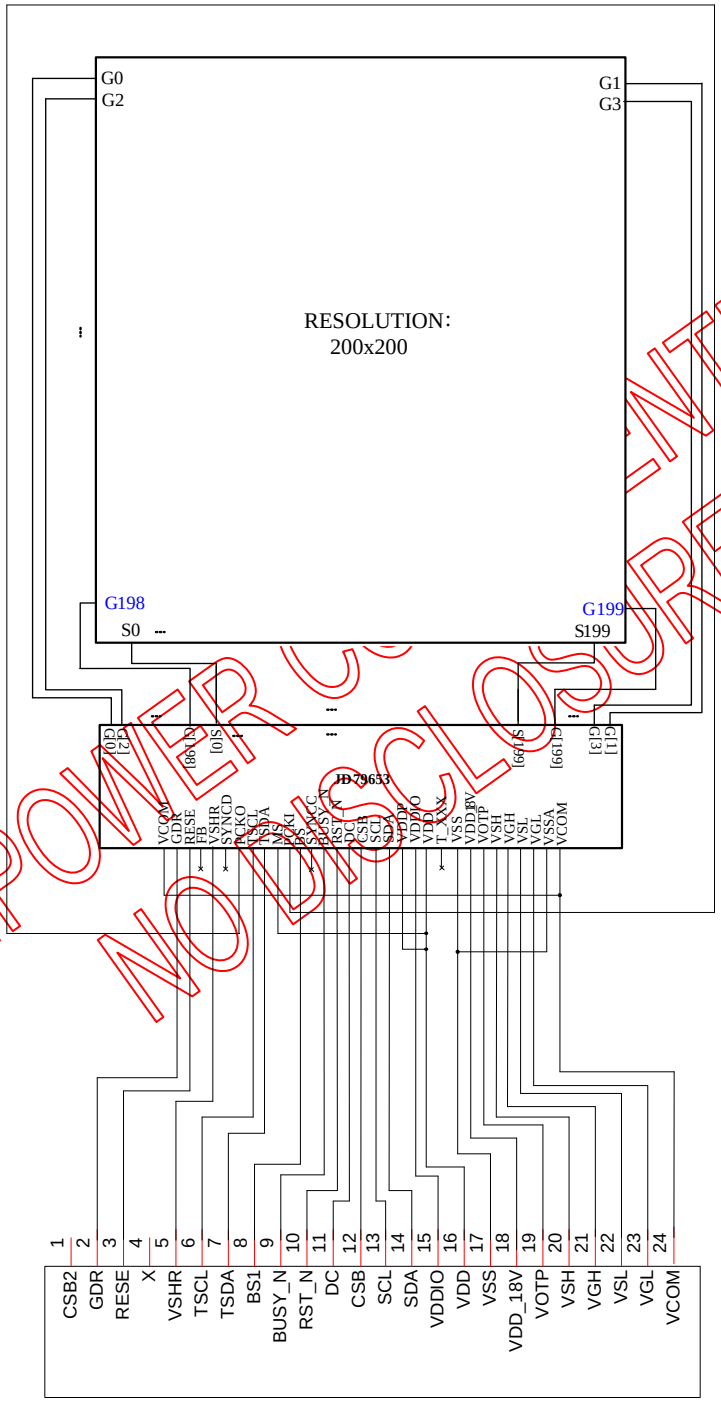
- System-on-chip (SOC) for color application
- Timing controller support several all resolution
  - Normally, resolution 200x200
- Support source & gate driver function:
  - 200 Outputs source driver with 1-bit white/black & 1-bit red per pixel:
    - Output dynamic range: VSH (+3.6~+15V)& VSL (-3.6~-15V) (programmable, black/white)
      VSHR: +2.4~+15V (programmable, red)
    - Output deviation: 0.1V
    - Left and Right shift capability
  - 200 Output gate driver:
    - Output dynamic range: VGH and VGL: +10~22V, -10V~-22V
    - Up and Down shift capability
- Common electrode level
  - AC-VCOM and DC-VCOM
  - Support sensing function (6-bit digital status)
  - Support LUT
- Charge Pump: On-chip booster and regulator
- Built in Frame memory maximum: (200x 200 x 1 bit) x 2 SRAM
- Built in temperature sensor:
  - On-Chip: -25~0 ^{o}C & 30~50 ^{o}C ± 2.0^{o}C, 0~30^{o}C ± 1.0^{o}C / 10-bit status
  - Off-Chip: -55~125^{o}C ± 2.0^{o}C / 11-bit status (I^2C/LM75)
- Support LPD, Low Power detection (V_{DD}< 2.2V~2.5V)

- PLL : On-chip RC oscillator
- 3-wire/4-wire (SPI) serial interface for system configuration
- Digital supply voltage: 2.3~3.6V
- OTP: 6K-byte OTP for LUT
- Partial update
- Support cascade
- Package-COG
- Support HV(VGH/VSH/VSL/VSHR) power detection
- FPC connector check
- CRC check mechanism
- OTP content protection
- Support BIST (build-in self test)mode
- Internal VOTP
- Extra 16 bytes reserved for user
- Low voltage application

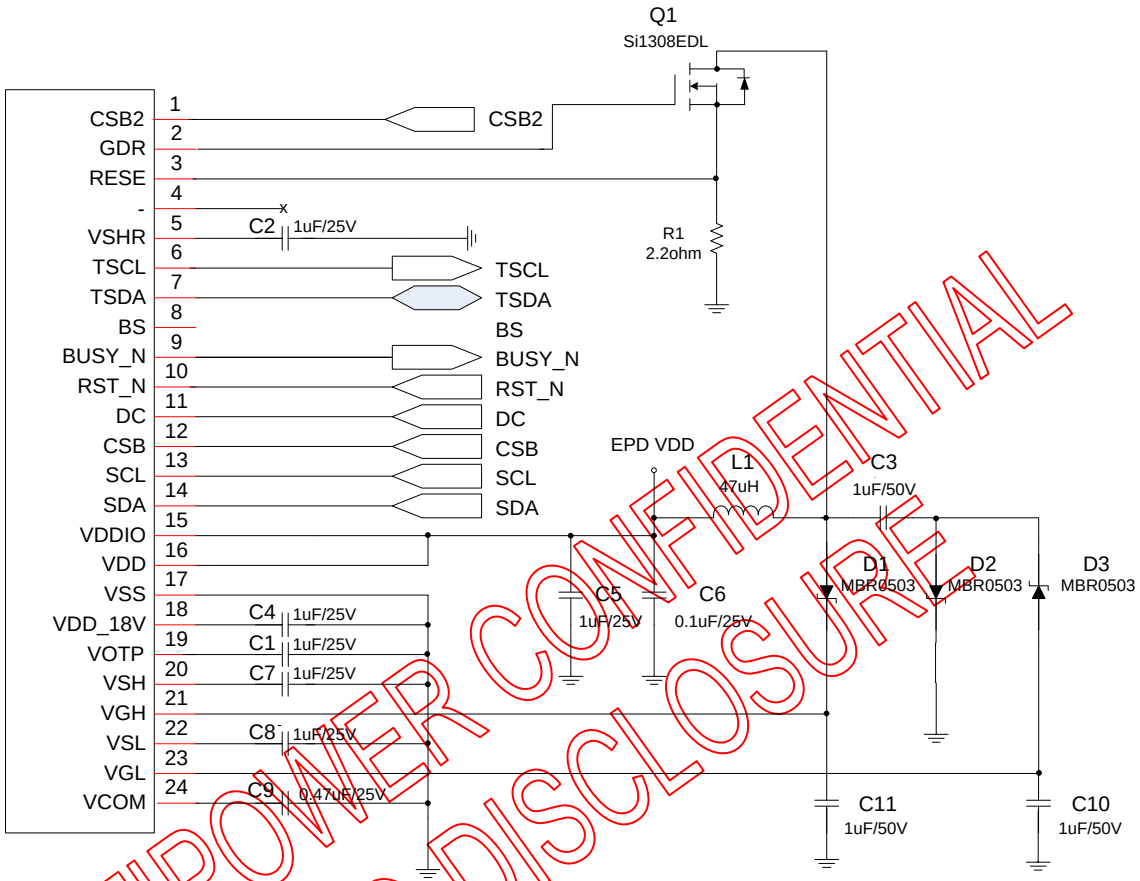
3. BLOCK DIAGRAM

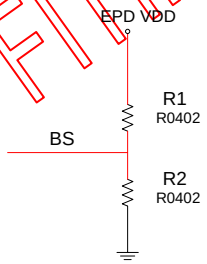


Normal type 1 (200x200.)



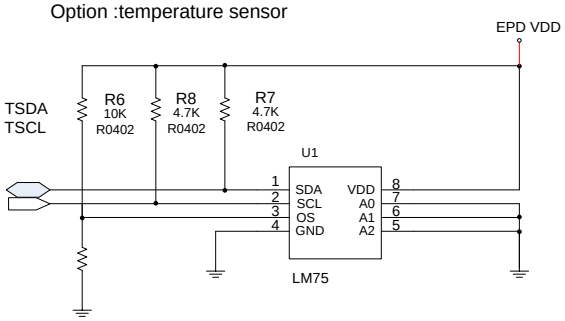
4. APPLICATION CIRCUIT





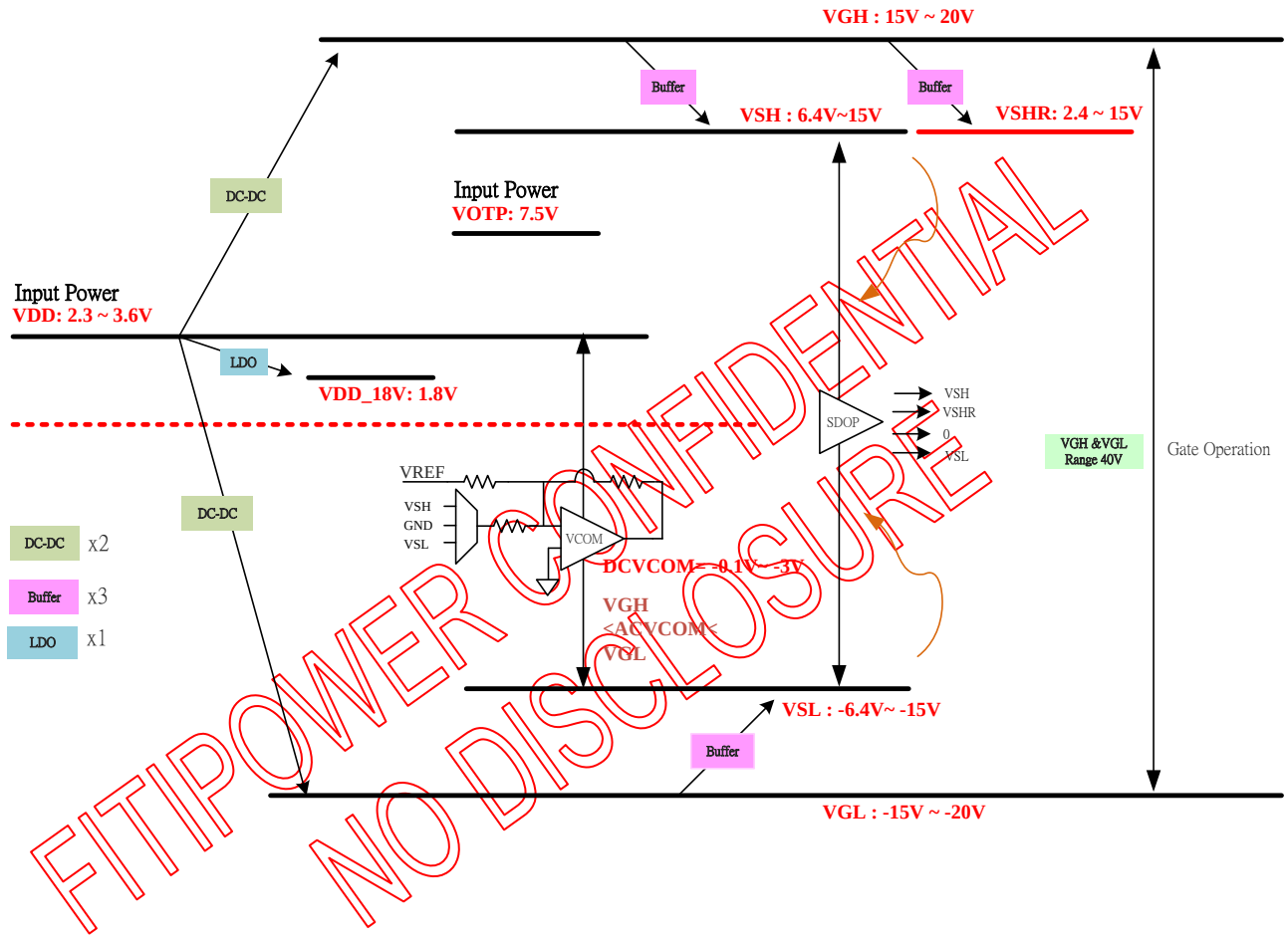
	R1	R2
3- wire SPI (CS#, SDA, SCL)	10K	NC
4-wire SPI (D/C#, CS#, SDA, SCL)	NC	10K

Option :temperature sensor



5. APPLICATION POWER CIRCUIT

5.1 Power Generation



6. PIN DESCRIPTION

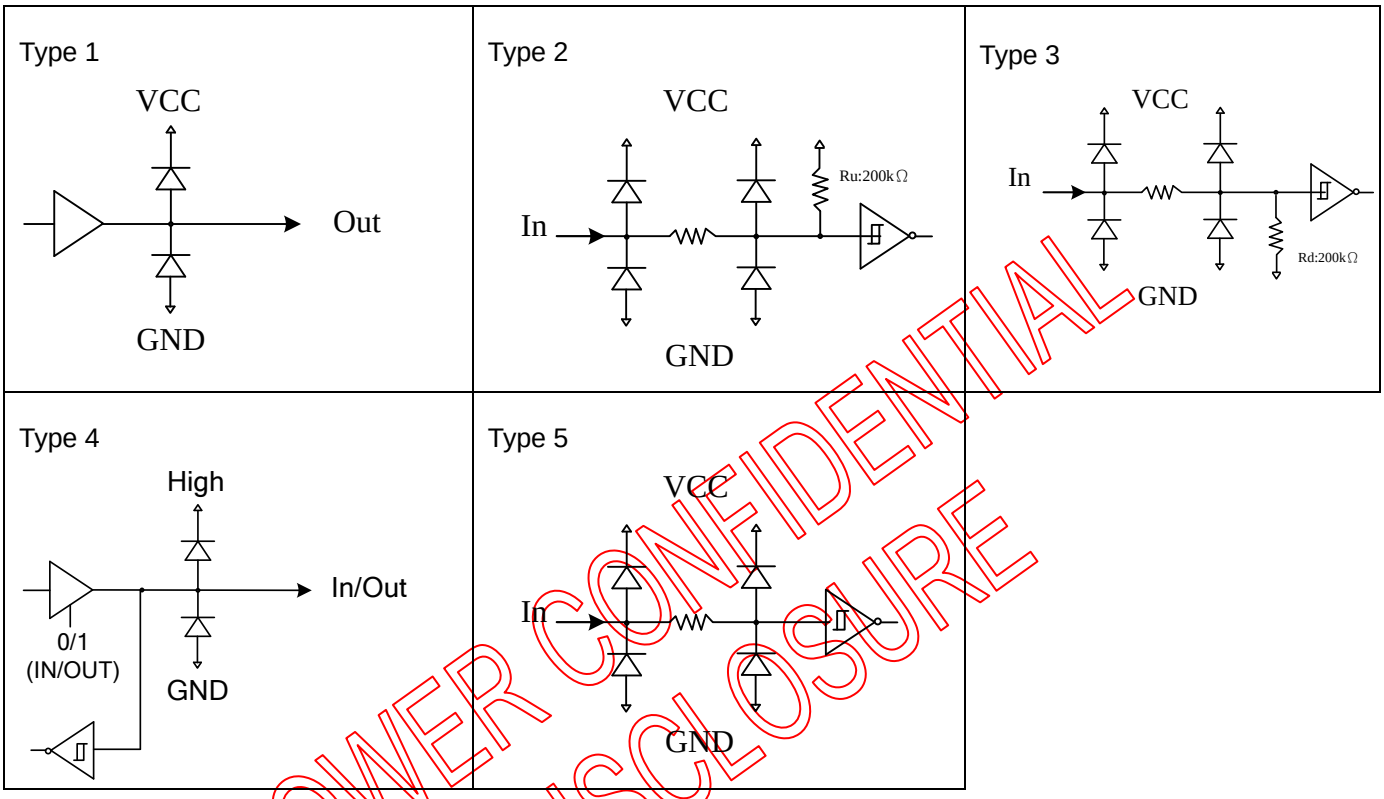
6.1 Pin define

Pin Name	Pin Type	I/O Structure	Description
Serial Communication Interface			
CSB	I	Type 5	Serial communication chip select.
SDA	I/O	Type 4	Serial communication data input.
SCL	I	Type 5	Serial communication clock input.
DC	I	Type 5	Serial communication Command/Data input L: Command H: data (default) Connect to VDD if BS=High.
Control Interface			
RST_N	I	Type 2	Global reset pin. Low reset. **(normal pull high)** When RST_N become low, driver will reset. All register will reset to default value. all driver function will disable. SD output and VCOM will be released to floating.
BUSY_N	O	Type1	This pin indicates the driver status. BUSY_N= "0" : Driver is busy, data/VCOM is transforming. BUSY_N= "1" : non-busy. Host side can send command/data to driver.
BS	I	Type 5	Input interface setting. Select 3 wire/ 4 wire SPI interface L: 4-wire IF H:3-wire IF(Default)
TSCL	O	Type1	I^2C clock for external temperature sensor
TSDA	I/O	Type 4	I^2C data for external temperature sensor
MS	I	Type 5	Master/Slave selection for cascade mode Low: Slave High: Master In single-chip mode, MS should be connect to VDD
Output Driver			
S[199:0]	O	-	Source driver output signals.
G[199:0]	O	-	Gate driver output signals.
Border			
VBD[4:1]	O	-	Border output pins. It outputs black WF.
VCOM GENERATOR			
VCOM	O	Type 1	VCOM output. VCOM has follow four voltage state: 1. (-VCM_DC) v 2. (VSH-VCM_DC) 3. (VSL-VCM_DC) v. 4. Floating
Power Circuit			
GDR	O	-	This pin is N-MOS gate control.
RESE	P	-	Current sense input for control loop.
FB	P	-	Keep open
VGH	P	Type 5	Positive gate voltage
VGL	P	Type 4	Negative gate voltage.
VSH	P	Type 1	Positive source voltage

Pin Name	Pin Type	I/O Structure	Description
VSL	P	Type 1	Negative source voltage.
VSHR	P	Type 1	Positive source voltage for Red
Power Supply			
VDDP	P	-	DCDC power input
VDD	P	-	Digital/Analog power.
VSS	P	-	Digital ground
VSSA	P		Analog Ground
VDDIO	P	-	IO voltage supply
VDD_18V	P	-	1.8V voltage input &output
VOTP	P	-	OTP program power (7.5V)
Reserved Pins			
TP [21:0]	I/O	-	Test pin
SyncD	I/O	Type 4	Cascade Data signal
SyncC	I/O	Type 4	Cascade Clock signal
PckI	I	Type 3	Break panel check input. Leave open if it is not used.
PckO	O	Type 1	Break panel check output. Leave open if it is not used.
Dummy	O	Type 1	Leave open.

Note: I: Input, O: Output, P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output, I/O: Input / Output. PS: Power Setting, C: Capacitor pin.

6.2 I/O Pin Structure



6.3 Value of wiring resistance to each pin

Pin name	Wiring resistance value(Ω)	Pin name	Wiring resistance value(Ω)
VCOM	5ohm	TSDA	100ohm
VGL	5ohm	TSCL	100ohm
VSHR	5ohm	BUSY_N	100ohm
VGH	5ohm	BS	100ohm
VSH	5ohm	RESE	5ohm
VOTP	5ohm	GDR	5ohm
VDD_18V	5ohm	SDA	100ohm
VSSA	5ohm	SCL	100ohm
VDDIO	5ohm	CSB	100ohm
VSS	5ohm	DC	100ohm
VDDP	5ohm	RST_N	100ohm
VDD	5ohm	SyncD	100ohm
VSL	5ohm	SyncC	100ohm
MS	100ohm	PCKI	100ohm
TP [21:0]	100ohm	PCKO	100ohm

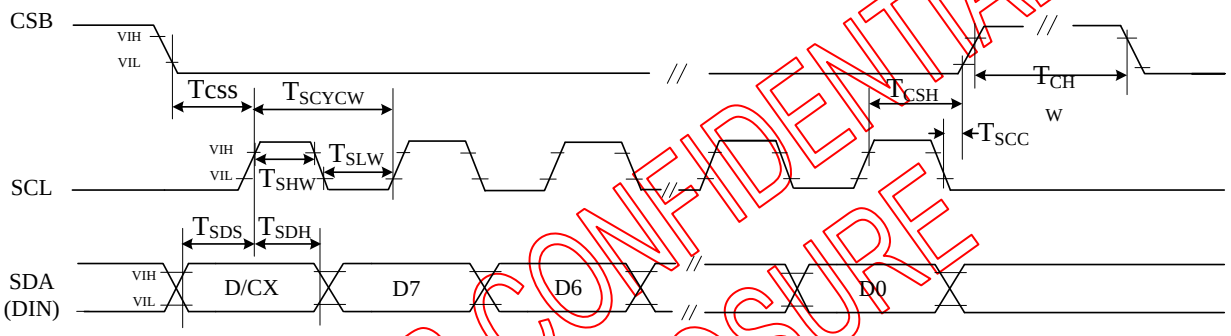
7. SPI COMMAND DESCRIPTION

7.1 “3-Wire” Serial Port Interface

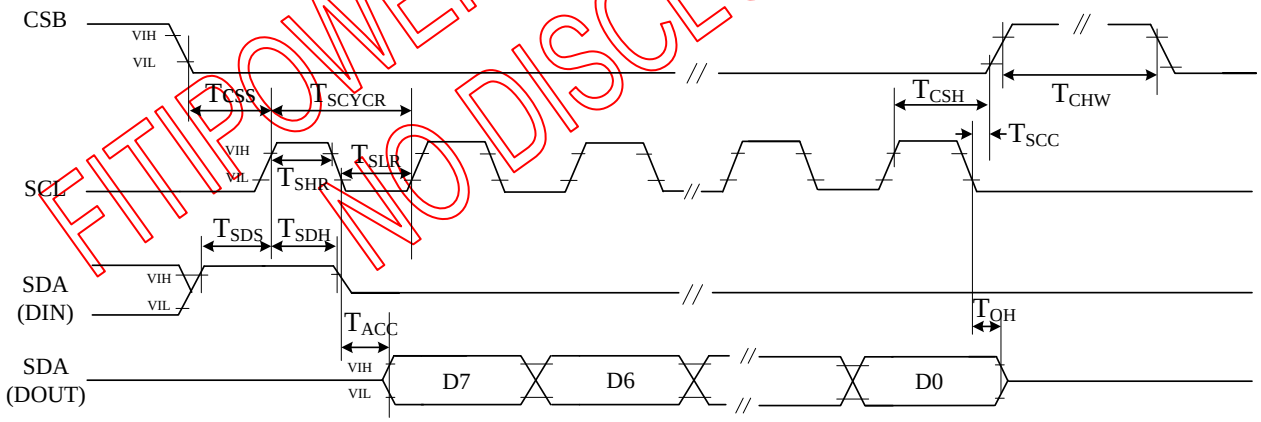
JD79653 use the 3-wire serial port as communication interface for all the function and command setting.

3-Wire communication can be bi-directional controlled by the “R/W” bit in address field. JD79653 3-Wire engine act as a “slave mode” for all the time, and will not issue any command to the 3-Wire bus itself.

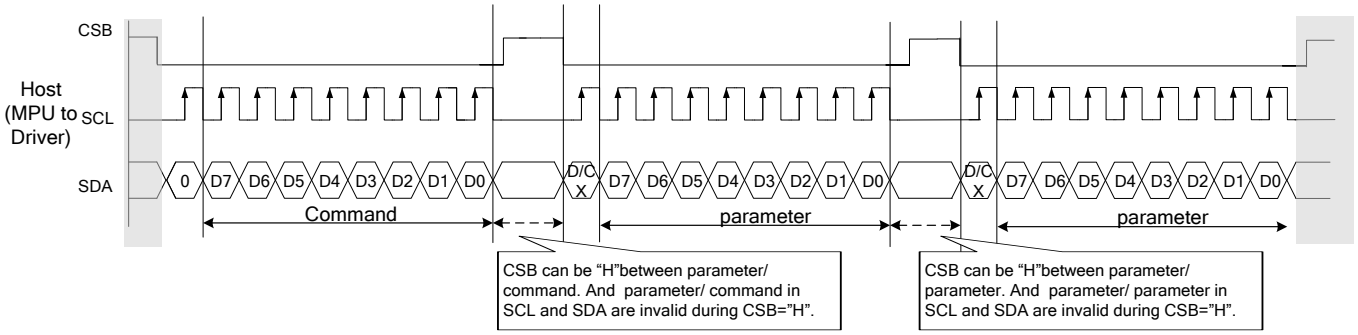
Under read mode, 3-Wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”.



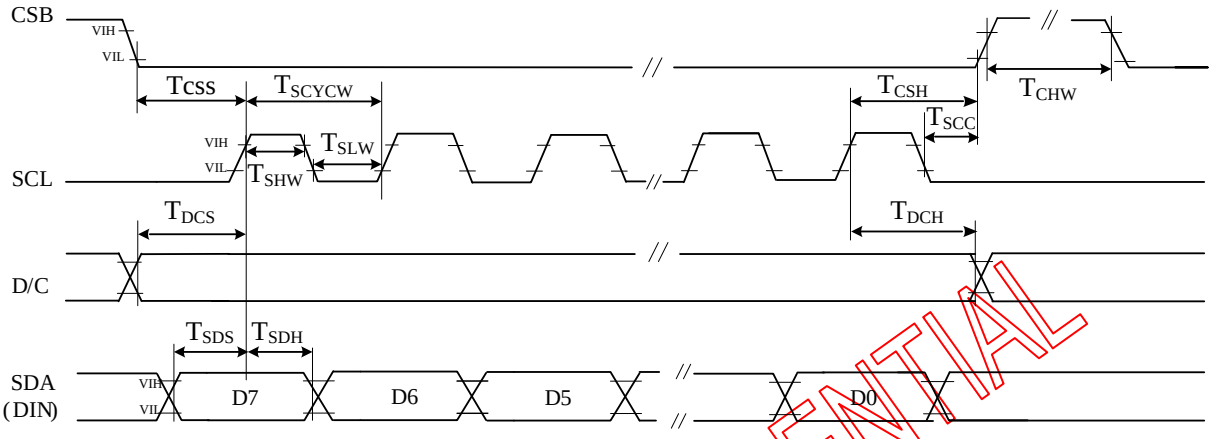
3 pin serial interface characteristics (write mode)



3 pin serial interface characteristics (read mode)

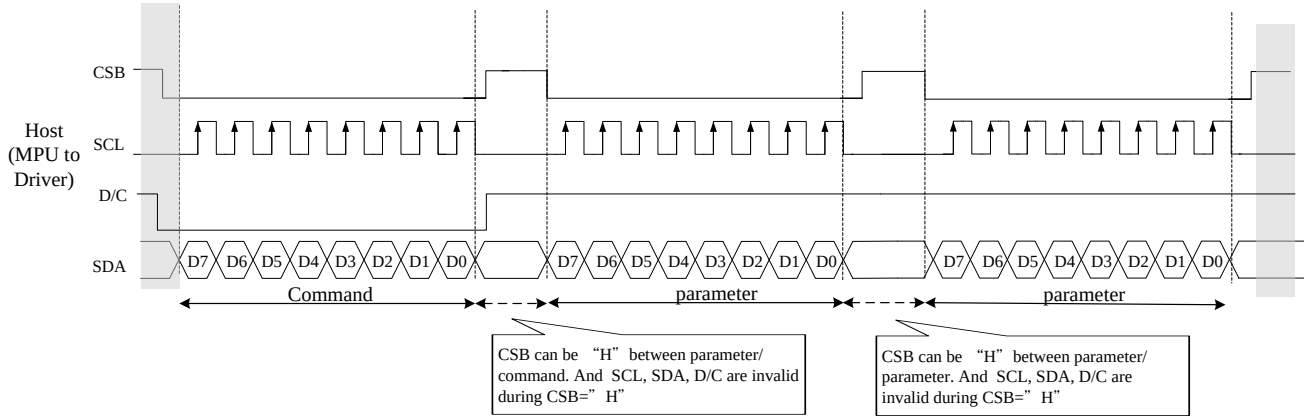


7.2 “4-Wire” Serial Port Interface



4 pin serial interface characteristics(write mode)

4 pin serial interface characteristics(read mode)



8. SPI CONTROL REGISTERS:

8.1 Register Table

Following table list all the SPI control registers and bit name definition for JD79653A. Refer to the next section for detail register function description.

Address	command	Bit										
		R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
R00H	Panel setting (PSR)	W	0		0	0	0	0	0	0	0	00H
		W	1	RES[1]	RES[0]	REG_EN	BWR	UD	SHL	SHD_N	RST_N	0Fh
		W	1	-	-	-	VCMZ	TS_AUTO	VCOMTIEG	NORG	VC_LUTZ	09h
R01H	Power setting (PWR)	W	0	0	0	0	0	0	0	0	1	01H
		W	1	-	-	-	-	-	-	VDS_EN	VDG_EN	0Ah
		W	1			-	VCOM_HV	VGHL_LV[1]	VGHL_LV [0]	VGHL_LV [1]	VGHL_LV [0]	39h
		W	1			VSH [5]	VSH [4]	VSH [3]	VSH [2]	VSH [1]	VSH [0]	39h
		W	1			VSL [5]	VSL [4]	VSL [3]	VSL [2]	VSL [1]	VSL [0]	26h
		W	1	OPTEN	VSHR [6]	VSHR [5]	VSHR [4]	VSHR [3]	VSHR [2]	VSHR [1]	VSHR [0]	06h
R02H	Power OFF(POF)	W	0	0	0	0	0	0	0	1	0	02H
R03H	Power off Sequence Setting(PFS)	W	0	0	0	0	0	0	0	1	1	03H
		W	1	-		T_VDS_OFF [1]	T_VDS_OFF [0]	T_VSHR_OFF [1]	T_VSHR_OFF [0]	-	-	00h
R04H	Power ON (PON)	W	0	0	0	0	0	0	1	0	0	04H
R05H	Power ON Measure (PMES)	W	0	0	0	0	0	0	1	0	1	05H
R06H	Booster Soft Start (BTST)	W	0	0	0	0	0	0	1	1	0	06H
		W	1	BT_PHA[7]	BT_PHA[6]	BT_PHA[5]	BT_PHA[4]	BT_PHA[3]	BT_PHA[2]	BT_PHA[1]	BT_PHA[0]	17h
		W	1	BT_PHB[7]	BT_PHB[6]	BT_PHB[5]	BT_PHB[4]	BT_PHB[3]	BT_PHB[2]	BT_PHB[1]	BT_PHB[0]	17h
		W	1	-	-	BT_PHC[5]	BT_PHC[4]	BT_PHC[3]	BT_PHC[2]	BT_PHC[1]	BT_PHC[0]	17h
		W	1	1	0	1	0	0	1	0	1	A5h
		W	1	FT_PHC[3]	FT_PHC[2]	FT_PHC[1]	FT_PHC[0]	FT_PHB[3]	FT_PHB[2]	FT_PHB[1]	FT_PHB[0]	00h
R07H	Deep Sleep(DSLP)	W	0	0	0	0	0	0	1	1	1	07H
		W	1	1	0	1	0	0	1	0	1	A5h
R10H	Data Start transmission1 (DTM1)	W	0	0	0	0	1	0	0	0	0	10H
		W	1	#	#	#	#	#	#	#	#	00H
R11H	Data Stop (DSP)	W	0	0	0	0	1	0	0	0	1	11H
		R	1	Data_flag	-	-	-	-	-	-	-	--
R12H	Display Refresh (DRF)	W	0	0	0	0	1	0	0	1	0	12H
R13H	Data Start transmission 2(DTM2)	W	0	0	0	0	1	0	0	1	1	13H
		W	1	#	#	#	#	#	#	#	#	00h
R17H	Auto sequence (AUTO)	W	0	0	0	0	1	0	1	1	1	17H
		W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	A5h
R18H	BIST	W	1	0	0	0	1	1	0	0	0	18H
		W	1	0	0	0	0	0	0	0	0	00h
		W	1	0	0	0	0	0	0	0	0	00h
R19H	BIST_PS	W	1	0	0	0	1	1	0	0	1	19H
		W	1	0	0	0	0	0	0	0	0	00h
		W	1	W [7:3]								00h
		W	1	L[7:0]								00h
		W	1	X1[7:3]					0	0	0	00h
		W	1	Y1[7:0]								00h
		W	1	X2[7:3]					1	1	1	00h

		W	1	Y2[7:0]								00h
R20H	LUT for VCOM (LUT1)	W	0	0	0	1	0	0	0	0	0	20H
		W	1	#	#	#	#	#	#	#	#	00h
R21H	White to White LUT (LUTWW)	W	0	0	0	1	0	0	0	0	1	21H
		W	1	#	#	#	#	#	#	#	#	00h
R22H	Black to White LUT (LUTBW/LUTR)	W	0	0	0	1	0	0	0	1	0	22H
		W	1	#	#	#	#	#	#	#	#	00h
R23H	White to Black LUT (LUTWB/LUTW)	W	0	0	0	1	0	0	0	1	1	23H
		W	1	#	#	#	#	#	#	#	#	00h
R24H	Black to Black LUT (LUTBB/LUTB)	W	0	0	0	1	0	0	1	0	0	24H
		W	1	#	#	#	#	#	#	#	#	00h
R25H	Group frame rate	W	0	0	0	1	0	0	1	0	1	25H
		W	1			Group1 M[2:0]			Group1 N[2:0]			3ch
		W	1			Group2 M[2:0]			Group2 N[2:0]			3ch
		W	1			Group3 M[2:0]			Group3 N[2:0]			3ch
		W	1			Group4 M[2:0]			Group4 N[2:0]			3ch
		W	1			Group5 M[2:0]			Group5 N[2:0]			3ch
		W	1			Group6 M[2:0]			Group6 N[2:0]			3ch
		W	1			Group7 M[2:0]			Group7 N[2:0]			3ch
		W	1			Group8 M[2:0]			Group8 N[2:0]			3ch
R26H	Set LUT States (SET_GROUP)	W	0	0	0	1	0	0	1	1	0	26H
		W	1	0	0	0	0	0	0	0	0	00h
R2AH	LUTC option	W	0	0	0	1	0	0	1	0	1	2AH
		W	1	EOPT	-	-	-	-	-	-	-	00h
		W	1	STATE_XON[7:0]								00h
		W	1	STATE_XON[15:8]								00h
R30H	PLL control (PLL)	W	0	0	0	1	1	0	0	0	0	30H
		W	1	-		M[2:0]			N[2:0]			3Ah
R31H	PLL mode selection	W	0	0	0	1	1	0	0	0	1	31H
		W	1	0	0	0	0	0	0	0	PLL option	01h
R40H	Temperature Sensor Command (TSC)	W	0	0	1	0	0	0	0	0	0	40H
		R	1	D10/TS[9]	D9/TS[8]	D8/TS[7]	D7/TS[6]	D6/TS[5]	D5/TS[4]	D4/TS[3]	D3/TS[2]	--
		R	1	D2/TS[1]	D1/ TS[0]	D0	-	-	-	-	-	--
R41H	Temperature Sensor Calibration (TSE)	W	0	0	1	0	0	0	0	0	1	41H
		W	1	TSE	-	-	-	TO[3]	TO[2]	TO[1]	TO0]	00h
R42H	Temperature Sensor Write (TSW)	W	0	0	1	0	0	0	0	1	0	42H
		W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
		W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
		W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h
R43H	Temperature Sensor Read (TSR)	W	0	0	1	0	0	0	0	1	1	43H
		R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	--
		R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	--
R44H	Panel Glass Check (PBC)	W	0	0	1	0	0	0	1	0	0	44H
		R	1	-	-	-	-	-	-	-	PSTA	-
R50H	VCOM and DATA interval setting (CDI)	W	0	0	1	0	1	0	0	0	0	50H
		W	1	VBD[1]	VBD[0]	DDX[1]	DDX[0]	CDI[3]	CDI[2]	CDI[1]	CDI[0]	D7h
R51H	Lower Power Detection (LPD)	W	0	0	1	0	1	0	0	0	1	51H
		R	1	GHD	SHD	SLD	SHRD-	-	-	-	LPD	--
R60H	TCON setting (TCON)	W	0	0	1	1	0	0	0	0	0	60H
		W	1	S2G[3]	S2G[2]	S2G[1]-	S2G[0]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	22h
R61H	Resolution	W	0	0	1	1	0	0	0	0	1	61H

	setting(TRES)	W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	-	-	-	00h	
		W	1	-	-	-	-	-	-	-	VRES(8)	00h	
		W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h	
R65H	Gate/Source Start Setting (GSST)	W	0	0	1	1	0	0	0	1	0	65H	
		W	1	S_start (7)	S_start (6)	S_start (5)	S_start (4)	S_start (3)	-	-	-	00h	
		W	1				gscan				G_start [8]	00h	
		W	1	G_start (7)	G_start (6)	G_start (6)	G_start (4)	G_start (3)	G_start (2)	G_start (1)	G_start (0)	00h	
R68H	Internal VOTP	W	0	0	1	1	0	1	0	0	0	68H	
		W	1	Internal VOTP[7:0]								00h	
R70H	REVISION (REV)	W	0	0	1	1	1	0	0	0	0	70H	
		R	1	REV[7]	REV[6]	REV[5]	REV[4]	REV[3]	REV[2]	REV[1]	REV[0]	--	
		R	1	REV[15]	REV[14]	REV[13]	REV[12]	REV[11]	REV[10]	REV[09]	REV[08]	--	
		R	1	Vendor ID				CHIP_REV				--	
R71H	Status register(FLG)	W	0	0	1	1	1	0	0	0	1	71H	
		R	1	Con_fb	PTL_flag	I^2C_ERR	I^2C_BUSYN	Data_flag	PON	POF	BUSY_N	-	
R7FH	Read Reserved Bytes	W	0	0	1	1	1	1	1	1	1	7FH	
		R	1	#	#	#	#	#	#	#	#		
R80H	Auto Measure Vcom (AMV)	W	0	1	0	0	0	0	0	0	0	80 H	
		W	1	-	-	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	10h	
R81H	Vcom Value (VV)	W	0	1	0	0	0	0	0	0	1	81H	
		R	1	-	-	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	--	
R82H	Vcom_DC Setting register(VDCS)	W	0	1	0	0	0	0	0	1	0	82H	
		W	1	-	-	VDCS[5]	VDCS[4]	VDCS[3]	VDCS[2]	VDCS[1]	VDCS[0]	00h	
R90H	Partial Window (PTL)	W	0	1	0	0	1	0	0	0	0	90H	
		W	1	HRST[7:3]				0	0	0	00h	00h	
		W	1	HRED[7:3]				1	1	1	00h	00h	
		W	1	-	-	-	-	-	-	-	VRST[8]	00h	
		W	1	VRST[7:0]								00h	
		W	1	-	-	-	-	-	-	-	VRED[8]	00h	
		W	1	VRED[7:0]								00h	
		W	1	-	-	-	-	-	-	-	PT_SCA	00h	
R91H	Partial In(PTIN)	W	0	1	0	0	1	0	0	0	1	91H	
R92H	Partial Out(PTOUT)	W	0	1	0	0	1	0	0	1	0	92H	
R94H	CRCS	W	0	1	0	0	1	0	1	0	0	94H	
R95H	CRCO	W	0	1	0	0	1	0	1	0	1	95H	
R96H	CRC status read	W	0	1	0	0	1	0	1	1	0	96H	
		R	1	CRC_MSB[7:0]								-	
		R	1	CRC_LSB[7:0]								-	
R97H	Write OTP key	W	0	1	0	0	1	0	1	1	1	97H	0
		W	1	CRC_MSB[7:0]								-	
		W	1	CRC_LSB[7:0]								-	
RA0H	Program Mode(PGM)	W	0	1	0	1	0	0	0	0	0	A0H	
RA1H	Active Program (APG)	W	0	1	0	1	0	0	0	0	1	A1H	
RA2H	Read OTP Data (ROTP)	W	0	1	0	1	0	0	0	1	0	A2H	
		R	1	#	#	#	#	#	#	#	#	--	
RE0H	CASCADE setting (CCSET)	W	0	1	1	1	0	0	0	0	0	E0H	
		W	1	-	-	-	-	-	-	TSFIX	CCEIN	00h	
RE1H	Set OTP program bank (SET_OTP_BANK)	W	0	1	1	1	0	0	0	0	1	E1H	
		W	1	-	-	-	-	-	-	LUT_bank0	reg_bank0	03h	
RE3H	Power saving	W	0	1	1	1	0	0	0	1	1	E3H	

		W	1	VCOM_W [3]	VCOM_W [2]	VCOM_W [1]	VCOM_W [0]	SD_W[3]	SD_W[2]	SD_W[2]	SD_W[0]	00h
RE4H	LVD voltage Select	W	0	1	1	1	0	0	1	0	0	E4H
		W	1	-	-	-	-	-	-	LVD_SEL [1]	LVD_SEL [0]	03h
RE5H	Force Temperature	W	0	1	1	1	0	0	1	0	1	E5H
		W	1	TS_SET[7]	TS_SET[6]	TS_SET[5]	TS_SET[4]	TS_SET[3]	TS_SET[2]	TS_SET[1]	TS_SET[0]	00h

8.2 Register Description

R/W: 0:Write Cycle 1:Read Cycle
D/CX:0:Command/1:Data
D7~D0:-:Don't Care

8.2.1R00H (PSR): Panel setting Register

R00H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PSR	W	0	0	0	0	0	0	0	0	0	00H
1st Parameter	W	1	RES[1]	RES[0]	REG_EN	BWR	UD	SHL	SHD_N	RST_N	0Fh
2nd Parameter	W	1	-	-	-	VCMZ	TS_AUTO	VGLTIEG	NORG	VC_LUTZ	09h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st parameter

Bit	Name	Description
0	RST_N	RST_N function 1: no effect. (default) 0: Booster OFF, Register data are set to their default values, and SEG/BG/VCOM:floating
1	SHD_N	SHD_N function 0 : Booster OFF, register data are kept, and SEG/BG/VCOM are kept floating. 1 : Booster on. (default)
2	SHL	SHL function 0: Shift left; First data=Sn→Sn-1 →…→S2→Last data=S1. 1: Shift right: First data=S1→S2 →…→Sn-1→Last data=Sn. (default)
3	UD	UD function 0:Scan down; First line=Gn→Gn-1 →…→G2→Last line=G1. 1:Scan up; First line=G1→G2 →…→Gn-1→Last line=Gn. (default)
4	BWR	Color selection setting 0: Pixel with B/W/Red. Run both LU1 and LU2. (default) 1: Pixel with B/W. Run LU1 only
5	REG_EN	LUT selection setting 0 : Using LUT from OTP(default) 1 : Using LUT from register
7-6	RES[1,0]	Resolution setting 11: Display resolution is 200x200 Others: no define.

Notes:
1. When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD turn off. SD output and VCOM will base on previous condition and keep floating.

2. When RST_N become low, driver will reset. All register will reset to default value. All of the driver's functions will disable. SD output and VCOM will base on previous condition and keep floating.

2nd parameter

	<table><tr><th>Bit</th><th>Name</th><th>Description</th></tr><tr><td>0</td><td>VC_LUTZ</td><td>VCOM status function 0 : Display off, VCOM keep to power off 1 : Display off, VCOM is set to floating (default)</td></tr><tr><td>1</td><td>NORG</td><td>VCOM status function 0 : No effect (default) 1 : Expect refreshing display, VCOM is tied to GND</td></tr><tr><td>2</td><td>VGLTIEG</td><td>VGL power off status function 0 : Power off, VGL will be floating (default) 1 : Power off, VGL will be tied to GND</td></tr><tr><td>3</td><td>TS_AUTO</td><td>Temperature sensing will be activated automatically one time 0 : Before enabling refresh, temperature sensing on 1 : Before enabling booster, temperature sensing on (default)</td></tr><tr><td>4</td><td>VCMZ</td><td>VCOM status function 0 : No effect (default) 1 : VCOM is always floating</td></tr></table> Priority of VCOM setting: VCMZ > NORG > VC_LUTZ
Restriction	

8.2.2 R01H (PWR): Power setting Register

R01H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWR	W	0	0	0	0	0	0	0	0	1	01h
1st Parameter	W	1	-	-	-	-	-	-	VDS_EN	VDG_EN	03h
2nd Parameter	W	1		-	-	VCOM_HV -	- VGHL_LV [3]	VGHL_LV [2]	VGHL_LV [1]	VGHL_LV [0]	0Ah
3rd Parameter	W	1	-	-	VSH [5]	VSH [4]	VSH [3]	VSH [2]	VSH [1]	VSH [0]	39h
4th Parameter	W	1	-	-	VSL [5]	VSL [4]	VSL [3]	VSL [2]	VSL [1]	VSL [0]	39h
5th Parameter	W	1	OPTEN	VSHR [6]	VSHR [5]	VSHR [4]	VSHR [3]	VSHR [2]	VSHR [1]	VSHR [0]	06h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st Parameter:

Bit	Name	Description
0	VDG_EN	**Gate power selection.** 0 : External VDNS power from VGH/VGL pins. (VDNG_EN open) 1 : Internal DCDC function for generate VGH/VGL. (default)
1	VDS_EN	**Source power selection.** 0 : External source power from VSH/VSL/VSHR pins. 1 : Internal DC/DC function for generate VSH/VSL/VSHR (default)

2nd Parameter:

Bit	Name	Description
3-0	VGHL_LV	**VGHL_LV Voltage Level.** 0000: VGH=10 v, VGL=-10v 0001: VGH=11 v, VGL=-11v 0010: VGH=12 v, VGL=-12v 0011: VGH=13 v, VGL=-13v 0100: VGH=14 v, VGL=-14v 0101: VGH=15 v, VGL=-15v 0110: VGH=16 v, VGL=-16v 0111: VGH=17 v, VGL=-17v 1000: VGH=18 v, VGL=-18v 1001: VGH=19 v, VGL=-19v 1010: VGH=20 v, VGL=-20v 1011: VGH=21 v, VGL=-21v 1100: VGH=22 v, VGL=-22v
4	VCOM_HV	**VCOM Voltage Level** 0: VCOMH=VSH+VCOMDC (default) VCOML=VSL+VCOMDC 1: VCOMH=VGH VCOML=VGL

3rd Parameter: Internal VSH power selection for B/W LUT.

Bit	Name	Description
5-0	**VSH**	**Internal VSH power selection.**

VSH[5:0]		Voltage(V)	VSH[5:0]		Voltage(V)	VSH[5:0]		Voltage(V)
000000	00h	3.6	010110	16h	8	101100	2Ch	12.4
000001	01h	3.8	010111	17h	8.2	101101	2Dh	12.6
000010	02h	4	011000	18h	8.4	101110	2Eh	12.8
000011	03h	4.2	011001	19h	8.6	101111	2Fh	13
000100	04h	4.4	011010	1Ah	8.8	110000	30h	13.2
000101	05h	4.6	011011	1Bh	9	110001	31h	13.4
000110	06h	4.8	011100	1Ch	9.2	110010	32h	13.6
000111	07h	5.0	011101	1Dh	9.4	110011	33h	13.8
001000	08h	5.2	011110	1Eh	9.6	110100	34h	14
001001	09h	5.4	011111	1Fh	9.8	110101	35h	14.2
001010	0Ah	5.6	100000	20h	10	110110	36h	14.4
001011	0Bh	5.8	100001	21h	10.2	110111	37h	14.6
001100	0Ch	6	100010	22h	10.4	111000	38h	14.8
001101	0Dh	6.2	100011	23h	10.6	111001	39h	15
001110	0Eh	6.4	100100	24h	10.8	others		15
001111	0Fh	6.6	100101	25h	11			
010000	10h	6.8	100110	26h	11.2			
010001	11h	7	100111	27h	11.4			
010010	12h	7.2	101000	28h	11.6			
010011	13h	7.4	101001	29h	11.8			
010100	14h	7.6	101010	2Ah	12			
010101	15h	7.8	101011	2Bh	12.2			

4th Parameter: Internal VSL power selection for B/W LUT.

Bit	Name	Description
5-0	**VSL**	**Internal VSL power selection.**

VSL[5:0]		Voltage(V)	VSL[5:0]		Voltage(V)	VSL[5:0]		Voltage(V)
000000	00h	-3.6	010110	16h	-8	101100	2Ch	-12.4
000001	01h	-3.8	010111	17h	-8.2	101101	2Dh	-12.6
000010	02h	-4	011000	18h	-8.4	101110	2Eh	-12.8
000011	03h	-4.2	011001	19h	-8.6	101111	2Fh	-13
000100	04h	-4.4	011010	1Ah	-8.8	110000	30h	-13.2
000101	05h	-4.6	011011	1Bh	-9	110001	31h	-13.4
000110	06h	-4.8	011100	1Ch	-9.2	110010	32h	-13.6

000111	07h	-5.0	011101	1Dh	-9.4	110011	33h	-13.8
001000	08h	-5.2	011110	1Eh	-9.6	110100	34h	-14
001001	09h	-5.4	011111	1Fh	-9.8	110101	35h	-14.2
001010	0Ah	-5.6	100000	20h	-10	110110	36h	-14.4
001011	0Bh	-5.8	100001	21h	-10.2	110111	37h	-14.6
001100	0Ch	-6	100010	22h	-10.4	111000	38h	-14.8
001101	0Dh	-6.2	100011	23h	-10.6	111001	39h	-15
001110	0Eh	-6.4	100100	24h	-10.8	others		-15
001111	0Fh	-6.6	100101	25h	-11			
010000	10h	-6.8	100110	26h	-11.2			
010001	11h	-7	100111	27h	-11.4			
010010	12h	-7.2	101000	28h	-11.6			
010011	13h	-7.4	101001	29h	-11.8			
010100	14h	-7.6	101010	2Ah	-12			
010101	15h	-7.8	101011	2Bh	-12.2			

5th Parameter:

Bit	Name	Description
5-0	**VSHR**	**Internal VSHR power selection.**

VSHR[5:0]		Voltage(V)	VSHR[5:0]		Voltage(V)	VSHR[5:0]		Voltage(V)
000000	00h	2.4	010110	16h	6.8	101100	2Ch	11.2
000001	01h	2.6	010111	17h	7	101101	2Dh	11.4
000010	02h	2.8	011000	18h	7.2	101110	2Eh	11.6
000011	03h	3.0	011001	19h	7.4	101111	2Fh	11.8
000100	04h	3.2	011010	1Ah	7.6	110000	30h	12
000101	05h	3.4	011011	1Bh	7.8	110001	31h	12.2
000110	06h	3.6	011100	1Ch	8	110010	32h	12.4
000111	07h	3.8	011101	1Dh	8.2	110011	33h	12.6
001000	08h	4	011110	1Eh	8.4	110100	34h	12.8
001001	09h	4.2	011111	1Fh	8.6	110101	35h	13
001010	0Ah	4.4	100000	20h	8.8	110110	36h	13.2
001011	0Bh	4.6	100001	21h	9	110111	37h	13.4
001100	0Ch	4.8	100010	22h	9.2	111000	38h	13.6
001101	0Dh	5	100011	23h	9.4	111001	39h	13.8
001110	0Eh	5.2	100100	24h	9.6	111010	3Ah	14
001111	0Fh	5.4	100101	25h	9.8	111011	3Bh	14.2
010000	10h	5.6	100110	26h	10	111100	3Ch	14.4
010001	11h	5.8	100111	27h	10.2	111101	3Dh	14.6
010010	12h	6	101000	28h	10.4	111110	3Eh	14.8

010011	13h	6.2	101001	29h	10.6	111111	3Fh	15
010100	14h	6.4	101010	2Ah	10.8	others		
010101	15h	6.6	101011	2Bh	11			

OPTEN=1:enable step -0.1 voltage selection(2.4~15V)
Internal VSHR power selection for Red LUT.

Bit	Name	Description
6-0	VSHR	**Internal VSHR power selection.**

VSHR[6:0]		Voltage(V)	VSHR[6:0]		Voltage(V)	VSHR[6:0]		Voltage(V)
0000000	00h	2.4	0011101	1Dh	5.3	0111010	3Ah	8.2
0000001	01h	2.5	0011110	1Eh	5.4	0111011	3Bh	8.3
0000010	02h	2.6	0011111	1Fh	5.5	0111100	3Ch	8.4
0000011	03h	2.7	0100000	20h	5.6	0111101	3Dh	8.5
0000100	04h	2.8	0100001	21h	5.7	0111110	3Eh	8.6
0000101	05h	2.9	0100010	22h	5.8	0111111	3Fh	8.7
0000110	06h	3	0100011	23h	5.9	1000000	40h	8.8
0000111	07h	3.1	0100100	24h	6	1000001	41h	8.9
0001000	08h	3.2	0100101	25h	6.1	1000010	42h	9
0001001	09h	3.3	0100110	26h	6.2	1000011	43h	9.1
0001010	0Ah	3.4	0100111	27h	6.3	1000100	44h	9.2
0001011	0Bh	3.5	0101000	28h	6.4	1000101	45h	9.3
0001100	0Ch	3.6	0101001	29h	6.5	1000110	46h	9.4
0001101	0Dh	3.7	0101010	2Ah	6.6	1000111	47h	9.5
0001110	0Eh	3.8	0101011	2Bh	6.7	1001000	48h	9.6
0001111	0Fh	3.9	0101100	2Ch	6.8	1001001	49h	9.7
0010000	10h	4	0101101	2Dh	6.9	1001010	4Ah	9.8
0010001	11h	4.1	0101110	2Eh	7	1001011	4Bh	9.9
0010010	12h	4.2	0101111	2Fh	7.1	1001100	4Ch	10
0010011	13h	4.3	0110000	30h	7.2	1001101	4Dh	10.1
0010100	14h	4.4	0110001	31h	7.3	1001110	4Eh	10.2
0010101	15h	4.5	0110010	32h	7.4	1001111	4Fh	10.3
0010110	16h	4.6	0110011	33h	7.5	1010000	50h	10.4
0010111	17h	4.7	0110100	34h	7.6	1010001	51h	10.5
0011000	18h	4.8	0110101	35h	7.7	1010010	52h	10.6
0011001	19h	4.9	0110110	36h	7.8	1010011	53h	10.7
0011010	1Ah	5	0110111	37h	7.9	1010100	54h	10.8
0011011	1Bh	5.1	0111000	38h	8	1010101	55h	10.9
0011100	1Ch	5.2	0111001	39h	8.1	1010110	56h	11
1010111	57h	11.1	1100101	65h	12.5	1110011	73h	13.9
1011000	58h	11.2	1100110	66h	12.6	1110100	74h	14
1011001	59h	11.3	1100111	67h	12.7	1110101	75h	14.1

1011010	5Ah	11.4	1101000	68h	12.8	1110110	76h	14.2
1011011	5Bh	11.5	1101001	69h	12.9	1110111	77h	14.3
1011100	5Ch	11.6	1101010	6Ah	13	1111000	78h	14.4
1011101	5Dh	11.7	1101011	6Bh	13.1	1111001	79h	14.5
1011110	5Eh	11.8	1101100	6Ch	13.2	1111010	7Ah	14.6
1011111	5Fh	11.9	1101101	6Dh	13.3	1111011	7Bh	14.7
1100000	60h	12	1101110	6Eh	13.4	1111100	7Ch	14.8
1100001	61h	12.1	1101111	6Fh	13.5	1111101	7Dh	14.9
1100010	62h	12.2	1110000	70h	13.6	1111110	7Eh	15
1100011	63h	12.3	1110001	71h	13.7	others		
1100100	64h	12.4	1110010	72h	13.8			

Note:
1.VSH>VSHR

Restriction

8.2.3 R02H (POF): Power OFF Command

R02H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
POF	W	0	0	0	0	0	0	0	1	0	02H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ● After power off command, driver will power off base on power off sequence. ● After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N singal will rise from low to high. ● Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. ● SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.
Restriction	This command only active when BUSY_N = "1".

8.2.4 R03H (PFS): Power off Sequence Setting Register

R03H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PFS	W	0	0	0	0	0	0	0	1	1	03H
1st Parameter	W	1	-	-	T_VDS_OFF [1]	T_VDS_OFF [0]			-	-	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : 1st Parameter:

Bit	Name	Description
5-4	T_VDS_OFF	00: 1 frame (default) 01: 2 frame 10: 3 frame 11: 4 frame

Restriction	

8.2.5 R04H (PON): Power ON Command

R04H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PON	W	0	0	0	0	0	0	1	0	0	04H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ● After power on command, driver will power on base on power on sequence. ● After power on command, BUSY_N signal will drop from high to low. When finishing the power on sequence, BUSY_N signal will rise from low to high.
Restriction	This command only active when BUSY_N = "1".

8.2.6 R05H (PMES): Power ON Measure Command

R05H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PMES	W	0	0	0	0	0	0	1	0	1	05H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■ If user wants to read temperature sensor or detect low power in power off mode, user has to send this command. After power on measure command, driver will switch on relevant commend with Low Power detection (R51H) and temperature measurement. (R40H).
Restriction	This command only active when BUSY_N = "1".

8.2.7 R06H (BTST): Booster Soft Start Command

R06H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
BTST	W	0	0	0	0	0	0	1	1	0	06H
1st Parameter	W	1	BT_PHA[7]	BT_PHA[6]	BT_PHA[5]	BT_PHA[4]	BT_PHA[3]	BT_PHA[2]	BT_PHA[1]	BT_PHA[0]	17h
2nd Parameter	W	1	BT_PHB[7]	BT_PHB[6]	BT_PHB[5]	BT_PHB[4]	BT_PHB[3]	BT_PHB[2]	BT_PHB[1]	BT_PHB[0]	17h
3rd Parameter	W	1	-	-	BT_PHC[5]	BT_PHC[4]	BT_PHC[3]	BT_PHC[2]	BT_PHC[1]	BT_PHC[0]	17h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command define as follows:

1st Parameter:

Bit	Name	Description
2-0	**Driving strength of phase A**	000: period 1 001: period 2 010: period 3 011: period 4 100: period 5 101: period 6 110: period 7 111: period 8 (default)
5-3		000: Strength 1 001: Strength 2 010: Strength 3 (default) 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8
7-6	**Soft start period of phase A**	00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS

2nd Parameter:

Bit	Name	Description
2-0	**Driving strength of phase B**	000: period 1 001: period 2 010: period 3 011: period 4 100: period 5 101: period 6 110: period 7 111: period 8 (default)
5-3		000: Strength 1 001: Strength 2 010: Strength 3 (default) 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8
7-6	**Soft start period of phase B**	00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS

<table>
<tr><td>Description</td><td>3rd Parameter:
<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>2-0</td><td>Minimum OFF time setting of GDR in phase C</td><td>000: period 1
001: period 2
010: period 3
011: period 4
100: period 5
101: period 6
110: period 7
111: period 8 (default)</td></tr>
<tr><td>5-3</td><td>Driving strength of phase C</td><td>000: Strength 1
001: Strength 2
010: Strength 3 (default)
011: Strength 4
100: Strength 5
101: Strength 6
110: Strength 7
111: Strength 8</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td>--This command only active when BUSY_N = “1”.</td></tr>
</table>

8.2.8 R07H (DSLP): Deep Sleep Command

R07H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSLP	W	0	0	0	0	0	0	1	1	1	07H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset. The only one parameter is a check code, the command would be excited if check code = 0xA5.
Restriction	This command only active when BUSY_N = "1".

8.2.9 R10H (DTM1): Data Start transmission 1 Register

R10H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM1	W	0	0	0	0	1	0	0	0	0	10H
1st Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
2nd Parameter	W	1									00h
…	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "OLD" data to SRAM. In B/W/Red mode, this command writes "B/W" data to SRAM. In Program mode, this command writes "OTP" data to SRAM for programming.
Restriction	

8.2.10 R11H (DSP): Data Stop Command

R11H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSP	W	0	0	0	0	1	0	0	0	1	11H
1st Parameter	R	1	Data_flag	-	-	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■While finished the data transmitting, user must send this command to driver and read Data_flag information. 1st Parameter: Bit / Name / Description 7 / -- / 0: Driver didn't receive all the data. 1: Driver has already received all of the one frame data. After "Data Start" (10h) or "Data Stop" (11h) commands and when data_flag=1, BUSY_N signal will become "0" and the refreshing of panel starts.
Restriction	This command only actives when BUSY_N = "1".

8.2.11 R12H (DRF): Display Refresh Command

R12H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DRF	W	0	0	0	0	1	0	0	1	0	12H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■While users send this command, driver will refresh display (data/VCOM) base on SRAM data and LUT. After display refresh command, BUSY_N signal will become "0".
Restriction	This command only actives when BUSY_N = "1"

8.2.12 R13H (DTM2): Data Start transmission 2 Register

R13H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM2	W	0	0	0	0	1	0	0	1	1	13H
1st Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
2nd Parameter	W	1									00h
…	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "NEW" data to SRAM. In B/W/Red mode, this command writes "RED" data to SRAM.
Restriction	

8.2.13 R17H (AUTO): Auto Sequence

R17H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Auto Sequence	W	0	0	0	0	1	0	1	1	1	17H
1st Parameter	W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	A5h

Description	The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP. AUTO (0x17) + Code(0xA5) = (PON→DRF→POF) AUTO (0x17) + Code(0xA7) = (PON→DRF→POF→DSLP)
Restriction	This command only actives when BUSY_N = "1"

8.2.14 R18H (BIST): BIST mode Command

R07H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
BIST	W	0	0	0	0	1	1	0	0	0	18H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h
2nd Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command define as follows:

This command use only BWR mode.

- 1st Parameter: (BIST once)

This parameter is a check code.

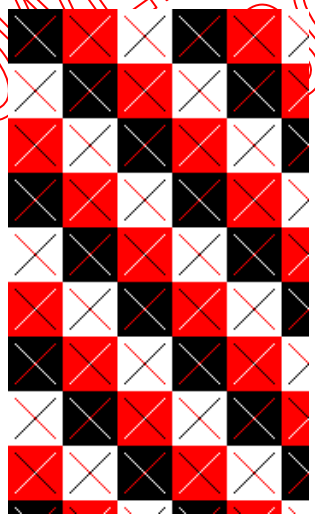
After this parameter is transmitted, the chip would enter the BIST mode, and display build-in pattern which could be decided by user in R19H (BIST_PS) command.

The command would be excited if check code = 0xA5.

While finished the BIST flow, the check code will be clear to 0x00.

The flow as below:

PON→DTM→DSP→POFF



• BIST pattern

- 2nd Parameter: (BIST auto run)

This parameter is a check code.

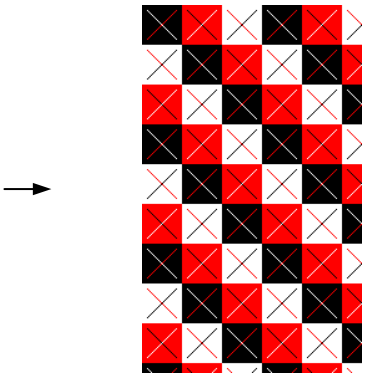
After this parameter is transmitted, the chip would enter the BIST mode, and display build-in pattern auto run.

The command would be excited if check code = 0xA5.

The BIST auto run flow will be stop when the check code =0x00.

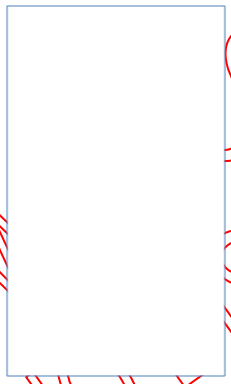
The flow as below:

PON→DTM→DSP→DTM→DSP→…→DTM→DSP→POFF (check code =0x00)

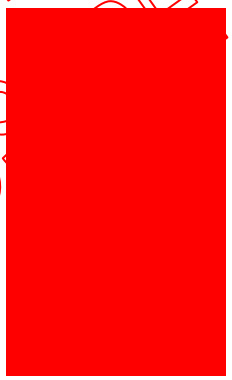


Check pattern

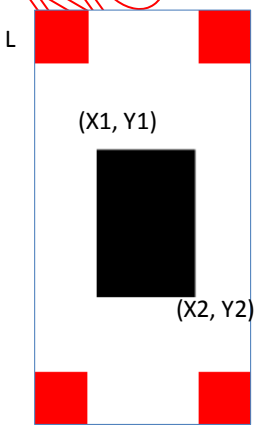
Black pattern



White pattern



Red pattern



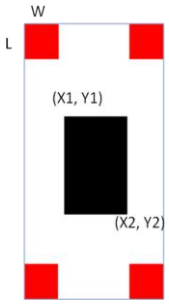
check pattern 2

- BIST pattern (repeat)

Restriction	-This command only actives after hardware reset. - The BUSY flag would change state from 0 to 1 while the command is completed - The DEBUG[6] pin is HW pin control(only auto run)

8.2.15 R19H (BIST_PS): Pattern Selection in BIST

R19H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Auto Sequence	W	0	0	0	0	1	1	0	0	1	19H
1st Parameter	W	1	-	-	-	-	-	BSIT_PS[2:0]			00h
2nd Parameter	W	1	W [7:3]					-			00h
3rd Parameter	W	1	L[7:0]								00h
4th Parameter	W	1	X1[7:3]					0	0	0	00h
5th Parameter	W	1	Y1[7:0]								00h
6th Parameter	W	1	X2[7:3]					1	1	1	00h
7th Parameter	W	1	Y2[7:0]								00h

Description	The command can decide which BIST pattern you would like to show. 1st Parameter 000: check pattern 001: Black pattern 010: White pattern 011: Red pattern 100: check pattern 2 Note: R19 should be determined before R18. 2nd ~7th Parameter : check pattern 2 setting W[7:3]: Red block width L[7:0]: Red block Length X1[7:3]: Black block X star point Y1[7:0]: Black block Y star point X2[7:3]: Black block X end point Y2[7:0]: Black block Y end point  Note: 1.W > H/2 → W = W/4 2.L > V/2 → L = V/4 3.X2 > X1 4.Y2 > Y
Restriction	This command only actives when BUSY_N = “1”.

8.2.16 R20H (LUTC): LUT for Vcom

R20H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTC	W	0	0	0	1	0	0	0	0	0	20H
1st Parameter	W	1	Group repeat times[7:0]								00h
2nd Parameter	W	1	level selection1-1 [1:0]		Frame Number1-1 [5:0]						00h
3rd Parameter	W	1	level selection1-2 [1:0]		Frame Number1-2 [5:0]						00h
4th Parameter	W	1	level selection2-1 [1:0]		Frame Number2-1 [5:0]						00h
5th Parameter	W	1	level selection2-2 [1:0]		Frame Number2-2 [5:0]						00h
6th Parameter	W	1	State 1 repeat times[7:0]								00h
7th Parameter	W	1	State 2 repeat times[7:0]								00h
8th~14th Parameter	W	1	2nd group								00h
15th~21th Parameter	W	1	3rd group								00h
…	W	1	4th~7th group								00h
50th~56th Parameter	W	1	8th group								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-This command builds up VCOM Look-Up Table (LUT). This LUT includes 8 kinds of groups; each group is of 7 bytes, as above. Each Group is divided to 2 states and "Group Repeat Number". Each state made up 2 phases. And each phase is combined with "Repeat Number", "Level selection", and "Frame Number". Byte 2: Group repeat times. Byte 3-6: [D7:D6]: Level selection of each phase. [D5:D0]: Frame number of each phase (state1 & state 2) Bytes 7~8: state repeat times (state1 & state 2) Bytes 2,9,16,23,30,…: Group repeat times 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 times Bytes 3~6,10~13,17~20, 24~27, 31~ 34 Level Selection. [D7:D6]: Level Selection. 00b:-VCM_DC 01b:VSH-VCM_DC(VCOMH) 10b:VSL -VCM_DC(VCOML) 11b:Floating [D5:D0]: Number of frames (state1 & state 2) 00 0000b~11 1111b: 0~63 times Bytes 7~8,14~15,21~22,28~29,35~36,…: :repeat times (state1 & state 2) 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 frames If BWR=0(BWR mode),all 8 groups are used. If BWR=1(BW mode),only 6 groups are used.
Restriction	

8.2.17 R21H (LUTWW): W2W LUT

R21H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTWW	W	0	0	0	1	0	0	0	0	1	21H
1st Parameter	W	1	Group repeat times[7:0]								00h
2nd Parameter	W	1	level selection1-1 [1:0]		Frame Number1-1 [5:0]						00h
3rd Parameter	W	1	level selection1-2 [1:0]		Frame Number1-2 [5:0]						00h
4th Parameter	W	1	level selection2-1 [1:0]		Frame Number2-1 [5:0]						00h
5th Parameter	W	1	level selection2-2 [1:0]		Frame Number2-2 [5:0]						00h
6th Parameter	W	1	State 1 repeat times[7:0]								00h
7th Parameter	W	1	State 2 repeat times[7:0]								00h
8th~14th Parameter	W	1	2nd group								00h
15th~21th Parameter	W	1	3rd group								00h
…	W	1	4th~5th group								00h
36th~42th Parameter	W	1	6th group								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-This command builds LUTWW for White-to- White. This LUT includes 6 kinds of groups; each group is of 7 bytes, as above. Each group is divided to 2 states and "Group Repeat Number". Each state made up 2 phases. And each phase is combined with "Repeat Number", "Level selection", and "Frame Number". Byte 2:Group repeat times. Byte 3-6: [D7:D6]: Level selection of each phase. [D5:D0]: Frame number of each phase (state1 & state 2) Bytes 7~8: state repeat times (state1 & state 2) Bytes 2,9,16,23,30,…: Group repeat times 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 times Bytes 3~6,10~13,17~20, 24~27, 31~ 34 Level Selection. [D7:D6]: Level Selection. 00b: GND 01b: VSH 10b: VSL 11b: VSHR [D5:D0]: Number of frames (state1 & state 2) 00 0000b~11 1111b: 0~63 times Bytes 7~8,14~15,21~22,28~29,35~36,…: :repeat times (state1 & state 2) 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 frames If BWR=0(BWR mode), LUTWW is not used. If BWR=1(BW mode), LUTWW is used.
Restriction	

8.2.18 R22H (LUTBW/LUTR): Black to White LUT or Red LUT Register

R22H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTBW/LUTR	W	0	0	0	1	0	0	0	1	0	22H
1st Parameter	W	1	Group repeat times[7:0]								00h
2nd Parameter	W	1	level selection1-1 [1:0]		Frame Number1-1 [5:0]						00h
3rd Parameter	W	1	level selection1-2 [1:0]		Frame Number1-2 [5:0]						00h
4th Parameter	W	1	level selection2-1 [1:0]		Frame Number2-1 [5:0]						00h
5th Parameter	W	1	level selection2-2 [1:0]		Frame Number2-2 [5:0]						00h
6th Parameter	W	1	State 1 repeat times[7:0]								00h
7th Parameter	W	1	State 2 repeat times[7:0]								00h
8tn~14tn Parameter	W	1	2nd group								00h
15tn~21th Parameter	W	1	3rd group								00h
…	W	1	4th~7th group								00h
50tn~56tn Parameter	W	1	8th group								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	- This command builds Look-up Table for LUTBW / LUTR. This LUT includes 8 kinds of groups; each group is of 7 bytes, as above. Each Group is divided to 2 states and "Group Repeat Number". Each state made up 2 phases. And each phase is combined with "Repeat Number", "Level selection", and "Frame Number". Byte 2:Group repeat times. Byte 3-6: [D7:D6]: Level selection of each phase. [D5:D0]: Frame number of each phase (state1 & state 2) Bytes 7~8: state repeat times (state1 & state 2) Bytes 2,9,16,23,30,…: Group repeat times 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 times Bytes 3~6,10~13,17~20, 24~27, 31~ 34 Level Selection. [D7:D6]: Level Selection. 00b: GND 01b: VSH 10b: VSL 11b: VSHR [D5:D0]: Number of frames (state1 & state 2) 00 0000b~11 1111b: 0~63 times Bytes 7~8,14~15,21~22,28~29,35~36,…: :repeat times (state1 & state 2) 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 frames If BWR=0(BWR mode),all 8 groups are used. If BWR=1(BW mode),only 6 groups are used.
Restriction	

8.2.19 R23H (LUTWB/LUTW): White to Black LUT or White LUT Register

R23H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTWB/LUTW	W	0	0	0	1	0	0	0	1	1	23H
1st Parameter	W	1	Group repeat times[7:0]								00h
2nd Parameter	W	1	level selection1-1 [1:0]		Frame Number1-1 [5:0]						00h
3rd Parameter	W	1	level selection1-2 [1:0]		Frame Number1-2 [5:0]						00h
4th Parameter	W	1	level selection2-1 [1:0]		Frame Number2-1 [5:0]						00h
5th Parameter	W	1	level selection2-2 [1:0]		Frame Number2-2 [5:0]						00h
6th Parameter	W	1	State 1 repeat times[7:0]								00h
7th Parameter	W	1	State 2 repeat times[7:0]								00h
8tn~14tn Parameter	W	1	2nd group								00h
15tn~21tn Parameter	W	1	3rd group								00h
…	W	1	4th~7th group								00h
50tn~56tn Parameter	W	1	8th group								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	- This command builds Look-up Table for LUTWB/LUTW. This LUT includes 8 kinds of groups; each group is of 7 bytes, as above. Each Group is divided to 2 states and "Group Repeat Number". Each state made up 2 phases. And each phase is combined with "Repeat Number", "Level selection", and "Frame Number". Byte 2:Group repeat times. Byte 3-6: [D7:D6]: Level selection of each phase. [D5:D0]: Frame number of each phase (state1 & state 2) Bytes 7~8: state repeat times (state1 & state 2) Bytes 2,9,16,23,30,…: Group repeat times 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 times Bytes 3~6,10~13,17~20, 24~27, 31~ 34 Level Selection. [D7:D6]: Level Selection. 00b: GND 01b: VSH 10b: VSL 11b: VSHR [D5:D0]: Number of frames (state1 & state 2) 00 0000b~11 1111b: 0~63 times Bytes 7~8,14~15,21~22,28~29,35~36,…: :repeat times (state1 & state 2) 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 frames If BWR=0(BWR mode),all 8 groups are used. If BWR=1(BW mode),only 6 groups are used.
Restriction	-

8.2.20 R24H (LUTBB/LUTB): Black to Black LUT or Black LUT Register

R24H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTBB/LUTB	W	0	0	0	1	0	0	1	0	0	24H
1st Parameter	W	1	Group repeat times[7:0]								00h
2nd Parameter	W	1	level selection1-1 [1:0]		Frame Number1-1 [5:0]						00h
3rd Parameter	W	1	level selection1-2 [1:0]		Frame Number1-2 [5:0]						00h
4th Parameter	W	1	level selection2-1 [1:0]		Frame Number2-1 [5:0]						00h
5th Parameter	W	1	level selection2-2 [1:0]		Frame Number2-2 [5:0]						00h
6th Parameter	W	1	State 1 repeat times[7:0]								00h
7th Parameter	W	1	State 2 repeat times[7:0]								00h
8tn~14tn Parameter	W	1	2nd group								00h
15tn~21th Parameter	W	1	3rd group								00h
…	W	1	4th~7th group								00h
50tn~56tn Parameter	W	1	8th group								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	- This command builds Look-up Table for LUTBB/LUTB. This LUT includes 8 kinds of groups; each group is of 7 bytes, as above. Each Group is divided to 2 states and "Group Repeat Number". Each state made up 2 phases. And each phase is combined with "Repeat Number", "Level selection", and "Frame Number". Byte 2: Group repeat times. Byte 3-6: [D7:D6]: Level selection of each phase. [D5:D0]: Frame number of each phase (state1 & state 2) Bytes 7~8: state repeat times (state1 & state 2) Bytes 2,9,16,23,30,…: Group repeat times 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 times Bytes 3~6,10~13,17~20, 24~27, 31~ 34 Level Selection. [D7:D6]: Level Selection. 00b: GND 01b: VSH 10b: VSL 11b: VSHR [D5:D0]: Number of frames (state1 & state 2) 00 0000b~11 1111b: 0~63 times Bytes 7~8,14~15,21~22,28~29,35~36,…: :repeat times (state1 & state 2) 0000 0000b: No repeat 0000 0001b~1111 1111b: 1~255 frames If BWR=0(BWR mode),all 8 groups are used. If BWR=1(BW mode),only 6 groups are used.
Restriction	

Note: All LUTs are independent of each other and could be deal with separately. If waveform time is different for each LUT, IC would select longest LUT as refresh time and fill 0 (GND) to remaining refresh time for other LUT.

8.2.21 R25H (GROUP Frame rate): Set LUT each group frame rate

R25H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
SET_ GROUP	W	0	0	0	1	0	0	1	0	1	25H
1st Parameter	W	1	-	-	Group1 M[2:0]			Group1 N[2:0]			3ch
2nd Parameter	W	1			Group2 M[2:0]			Group2 N[2:0]			3ch
3rd Parameter	W	1			Group3 M[2:0]			Group3 N[2:0]			3ch
4th Parameter	W	1			Group4 M[2:0]			Group4 N[2:0]			3ch
5th Parameter	W	1			Group5 M[2:0]			Group5 N[2:0]			3ch
6th Parameter	W	1			Group6 M[2:0]			Group6 N[2:0]			3ch
7th Parameter	W	1			Group7 M[2:0]			Group7 N[2:0]			3ch
8th Parameter	W	1			Group8 M[2:0]			Group8 N[2:0]			3ch

Description

This command is used to set LUT states

The command controls the LUT frequency. The PLL structure must support the following frame rates:

M	N	Frame rate	M	N	Frame rate	M	N	Frame rate	M	N	Frame rate
1	1	29HZ	3	1	86HZ	5	1	150HZ	7	1	200HZ
	2	14HZ		2	43HZ		2	72HZ		2	100HZ
	3	10HZ		3	29HZ		3	48HZ		3	67HZ
	4	7HZ		4	21HZ		4	36HZ		4	50HZ
	5	6HZ		5	17HZ		5	29HZ		5	40HZ
	6	5HZ		6	14HZ		6	24HZ		6	33HZ
	7	4HZ		7	12HZ		7	20HZ		7	29HZ
2	1	57HZ	4	1	114HZ	6	1	171HZ			
	2	29HZ		2	57HZ		2	86HZ			
	3	19HZ		3	38HZ		3	57HZ			
	4	14HZ		4	29HZ		4	43HZ			
	5	11HZ		5	23HZ		5	34HZ			
	6	10HZ		6	19HZ		6	29HZ			
	7	8HZ		7	16HZ		7	24HZ			

Restriction

8.2.22 R26H (SET_GROUP): Set LUT States

R26H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
SET_ GROUP	W	0	0	0	1	0	0	1	1	0	26H
1st Parameter	W	1	-	-	-	-	-	-	group_sel[1:0]		00h

Description	This command is used to set LUT states Function of group_sel [1:0] are shown below B/W/Red mode(BWR=0)

Value	Group
00	8
01	7
10	6
11	5

B/W mode (BWR=1)

Value	Group
00	6
01	5
10	4
11	3

Restriction	

8.2.23 R2AH (LUTOPT): LUT Option Register

R2AH	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUT Option	W	0	0	0	1	0	1	0	1	0	2AH
1st Parameter	W	1	EOPT	-	-	-	-	-	-	-	00h
2nd Parameter	W	1	STATE_XON[7:0]								00h
3rd Parameter	W	1	STATE_XON[15:8]								00h

Description

- This command sets XON and ending options of source output STATE_XON[15:0]:

  All Gate ON (Each bit controls one sub-state, STATE_XON [0] for state-1, STATE_XON [1] for state-2 …..)
  0000 0000 0000 0000b: no All-Gate-ON
  0000 0000 0000 0001b: State1 All-Gate-ON
  0000 0000 0000 0011b: State1 and State2 All-Gate-ON
  …

EOPT:
Option for LUT ending

1st Parameter:

Bit	Name	Description
7	EOPT	0: Normal.(Default) 1: Source output level keep previous output before power off

Restriction

8.2.24 R30H (PLL): PLL Control Register

R30H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PLL	W	0	0	0	1	1	0	0	0	0	30H
1st Parameter	W	1	-	-	M[2:0]			N[2:0]			3Ch

NOTE: "-" Don't care, can be set to VDD or GND level

Description

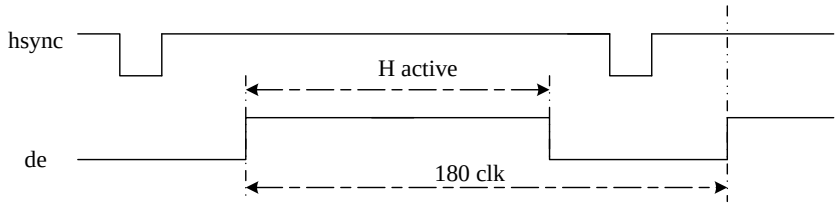
-The command defines as:

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

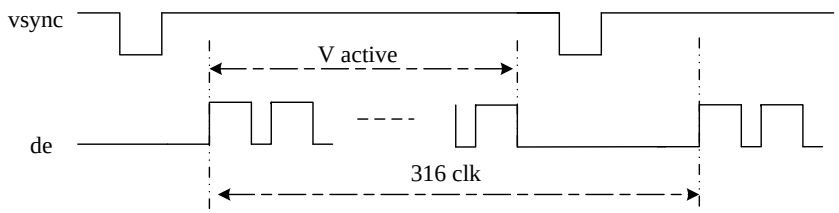
M	N	Frame rate	M	N	Frame rate	M	N	Frame rate	M	N	Frame rate
1	1	29HZ	3	1	86HZ	5	1	150HZ	7	1	200HZ
	2	14HZ		2	43HZ		2	72HZ		2	100HZ
	3	10HZ		3	29HZ		3	48HZ		3	67HZ
	4	7HZ		4	21HZ		4	36HZ		4	50HZ
	5	6HZ		5	17HZ		5	29HZ		5	40HZ
	6	5HZ		6	14HZ		6	24HZ		6	33HZ
	7	4HZ		7	12HZ		7	20HZ		7	29HZ
2	1	57HZ	4	1	114HZ	6	1	171HZ			
	2	29HZ		2	57HZ		2	86HZ			
	3	19HZ		3	38HZ		3	57HZ			
	4	14HZ		4	29HZ		4	43HZ			
	5	11HZ		5	23HZ		5	34HZ			
	6	10HZ		6	19HZ		6	29HZ			
	7	8HZ		7	16HZ		7	24HZ			

remark

-Horizental



-Vertical



Restriction

8.2.25 R31H (PLL mode selection):

R30H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PLL	W	0	0	0	1	1	0	0	0	0	30H
1st Parameter	W	1	-	-	-	-	-	-	-	PLL option	01h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: The command controls the R30H (PLL)& R25H (group frame rate) selection. If PLL option sets to 0, R25H (group frame rate) was decided. If PLL option sets to 1, R30H (PLL) was decided.
remark	
Restriction	

8.2.26 R40H (TSC): Temperature Sensor Command

R40H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	0	0	40H
1st Parameter	R	1	D10/TS[9]	D9/TS[8]	D8/TS[7]	D7/TS[6]	D6/TS[5]	D5/TS[4]	D4/TS[3]	D3/TS[2]	-
2nd Parameter	R	1	D2/TS[1]	D1/ TS[0]	D0	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

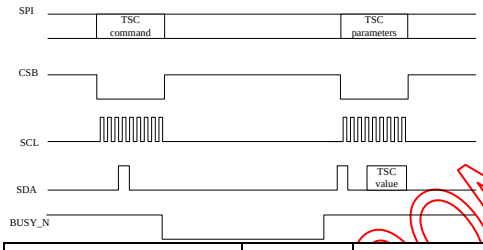
Description

-The command define as follows:

This command indicates the temperature value.

If R41H(TSE) bit7 set to 0, this command reads internal temperature sensor value.

If R41H(TSE) bit7 set to 1, this command reads external (LM75) temperature sensor value



TS[9:2]/D[10:3]	T (℃)	TS[9:2]/D[10:3]	T (℃)	TS[9:2]/D[10:3]	T (℃)
11100111	-25	00000000	0	00011001	25
11101000	-24	00000001	1	00011010	26
11101001	-23	00000010	2	00011011	27
11101010	-22	00000011	3	00011100	28
11101011	-21	00000100	4	00011101	29
11101100	-20	00000101	5	00011110	30
11101101	-19	00000110	6	00011111	31
11101110	-18	00000111	7	00100000	32
11101111	-17	00001000	8	00100001	33
11110000	-16	00001001	9	00100010	34
11110001	-15	00001010	10	00100011	35
11110010	-14	00001011	11	00100100	36
11110011	-13	00001100	12	00100101	37
11110100	-12	00001101	13	00100110	38
11110101	-11	00001110	14	00100111	39
11110110	-10	00001111	15	00101000	40
11110111	-9	00010000	16	00101001	41
11111000	-8	00010001	17	00101010	42
11111001	-7	00010010	18	00101011	43
11111010	-6	00010011	19	00101100	44
11111011	-5	00010100	20	00101101	45
11111100	-4	00010101	21	00101110	46
11111101	-3	00010110	22	00101111	47
11111110	-2	00010111	23	00110000	48
11111111	-1	00011000	24	00110001	49

TS[1:0]	T (℃)
00	+0
01	+0.25
10	+0.5
11	+0.75

Restriction

This command only actives when BUSY_N = "1".

8.2.27 R41H (TSE): Temperature Sensor Calibration Register

R41H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSE	W	0	0	1	0	0	0	0	0	1	41H
1st Parameter	W	1	TSE	-	TO[5]	TO[4]	TO[3]	TO[2]	TO[1]	TO[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the driver IC temperature sensor enable and calibration function.

Reserve one temperature offset TO[3:0] for calibration
1. TO[3]: mean '+' or '-' , while 0 is '+' ; 1 is '-'
2. TO[2:0]: mean temperature offset value

Bit	Description
3-0	Temperature level: 0000: +0℃ (default) 0001: +1℃ 0010: +2℃ 0011: +3℃ 0100: +4℃ 0101: +5℃ 0110: +6℃ 0111: +7℃ 1000: -8℃ 1001: -7℃ 1010: -6℃ 1011: -5℃ 1100: -4℃ 1101: -3℃ 1110: -2℃ 1111: -1℃
5-4	00: +0.0℃ (default) 01: +0.25℃ 10: +0.5℃ 11: +0.75℃
7	Internal temperature sensor enable 0: Internal temperature sensor enable.(default) 1: Internal temperature sensor disable, using external temperature sensor.

Restriction

This command only actives after R04H(PON) or R05H(PMES)

8.2.28 R42H (TSW): Temperature Sensor Write Register

R42H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSW	W	0	0	1	0	0	0	0	1	0	42H
1st Parameter	W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
2nd Parameter	W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
3rd Parameter	W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

This command writes the temperature.

1st Parameter:

Bit	temperature
2-0	Pointer setting
5-3	User-defined address bits (A2, A1, A0)
7-6	I2C Write Byte Number 00: 1 byte (head byte only) 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1st parameter) 11: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

2nd Parameter:

Bit	temperature
7-0	MSByte of write-data to external temperature sensor

3nd Parameter:

Bit	temperature
7-0	LSByte of write-data to external temperature sensor

Restriction

This command only actives after R04H(PON) or R05H(PMES)

8.2.29 R43H (TSR): Temperature Sensor Read Register

R43H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	1	1	43H
1st Parameter	R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	-
2nd Parameter	R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

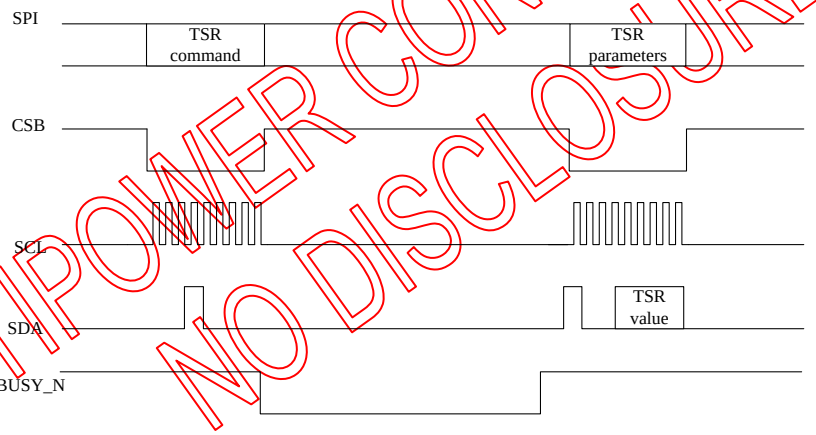
This command reads the temperature sensed by the temperature sensor.

1st Parameter:

Bit	temperature
7-0	MSByte of read-data from external temperature sensor

2nd Parameter:

Bit	temperature
7-0	LSByte of write-data from external temperature sensor



Restriction

This command only actives after R04H(PON) or R05H(PMES)

8.2.30 R44H (PBC): Panel Glass Check Register

R44H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PBC	W	0	0	1	0	0	0	1	0	0	44H
1st Parameter	R	1	-	-	-	-	-	-		PSTA	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	- This command is used to enable panel check, and to disable after reading result. Bit 0 / Name PSTA / Description: 0 : Panel check fail (panel broken); 1 : Panel check pass
Restriction	This command only actives when BUSY_N = "1".

8.2.31 R50H (CDI): VCOM and DATA interval setting Register

R50H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CDI	W	0	0	1	0	1	0	0	0	0	50H
1st Parameter	W	1	VBD[1]	VBD[0]	DDX[1]	DDX[0]	CDI[3]	CDI[2]	CDI[1]	CDI[0]	D7h

NOTE: "-" Don't care, can be set to VDD or GND level

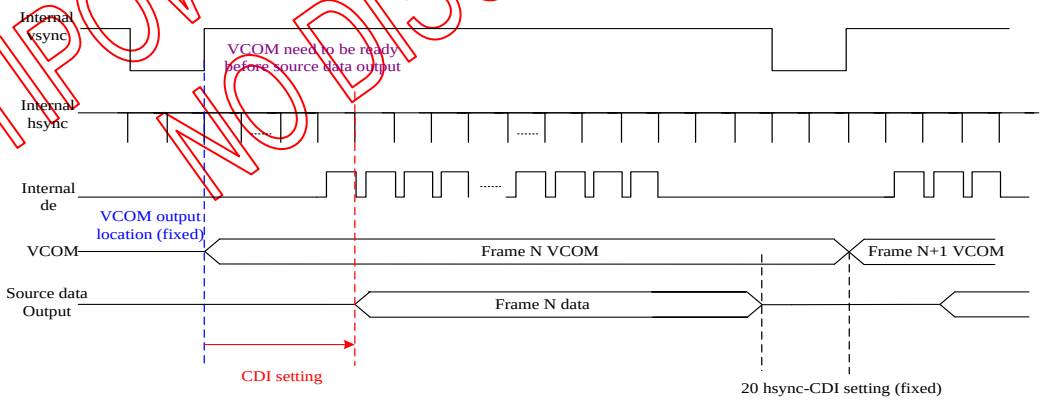
Description

-The command defines as:

1st Parameter:

CDI[1:0]: This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be keep (20hsync).

Bit	
3-0	Vcom and data interval 0000: 17 hsync 0001:16 hsync 0010:15 hsync 0011:14 hsync 0100:13 hsync 0101:12 hsync 0110:11 hsync 0111:10 hsync 1000:9 hsync 1001:8 hsync 1010:7 hsync 1011:6 hsync 1100:5 hsync 1101:4 hsync 1110:3 hsync 1111:2 hsync



VBD[1:0]: Border data selection.

B/W/Red mode(BWR=0)

Bit 4	Bit7-6	Description
DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTR
	10	LUTW
	11	LUTB
1 (default)	00	LUTB
	01	LUTW
	10	LUTR
	11 (default)	Floating

B/W mode (BWR=1)

Bit 4	Bit7-6	description
DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTBW (1->0)
	10	LUTWB (0->1)
	11	Floating
1 (default)	00	Floating
	01	LUTWB (0->1)
	10	LUTBW (1->0)
	11	Floating

Border output voltage level: The level selection is based on mapping LUT data.
Level Selection:
00b: VCOM
01b: VSH
10b: VSL
11b: VSHR

DDX[1:0]: Data polarity
1. DDX[1] for RED data, DDX[0] for BW data in the B/W/Red mode
2. DDX[0] for B/W mode

B/W/Red mode(BWR=0)
DDX[1] is for RED data
DDX[0] is for B/W data

Bit 5-4	Description	
DDX[1:0]	Data (Red/B/W)	LUT
00	00	LUTW
	01	LUTB
	10	LUTR
	11	LUTR
01 (default)	00	LUTB
	01	LUTW
	10	LUTR
	11	LUTR
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTB
11	00	LUTR
	01	LUTR
	10	LUTB
	11	LUTW

B/W mode (BWR=1)

DDX[1]=0 is for BW mode with NEW/OLD

Bit 5-4	Description	
DDX[1:0]	Data (B/W)	LUT
00	00	LUTWW (0->0)
	01	LUTBW(1->0)
	10	LUTWB(0->1)
	11	LUTBB(1->1)
01 (default)	00	LUTBB(0->0)
	01	LUTWB(1->0)
	10	LUTBW(0->1)
	11	LUTWW(1->1)

DDX[1]=1 is for BW mode without NEW/OLD

Bit 5-4	Description	
DDX[1:0]	Data (B/W)	LUT
10	0	LUTBW(1->0)
	1	LUTWB(0->1)
11	0	LUTWB(0->1)
	1	LUTBW(1->0)

Restriction	

8.2.32 R51H (LPD): Lower Power Detection Register

R51H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LPD	W	0	0	1	0	1	0	0	0	1	51H
1st Parameter	R	1	GHD	SHD	SLD	SHRD -	-	-	-	LPD	--

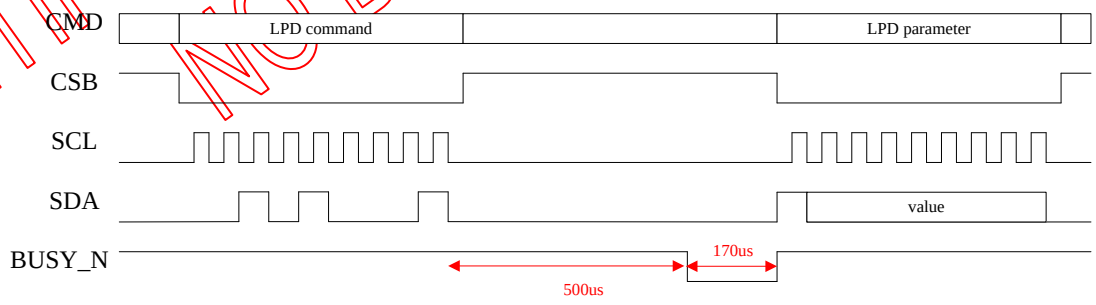
NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the input power condition. Host can read this data to understand the battery's condition.
When LPD="1", system input power is normal.
When LPD="0", system input power is lower (VDD<2.5v, which could be select in RE4H (LVSEL)).

1st Parameter:

Bit	Name	Description
0	LPD	0: Low power input 1: Normal status
4	SHRD	0: Detect voltage < 90%VSHR 1: Normal status
5	SLD	0: Detect voltage < 95%VSL 1: Normal status
6	SHD	0: Detect voltage < 95%VSH 1: Normal status
7	GHD	0: Detect voltage < 95%VGH 1: Normal status



Restriction

- This command only actives when BUSY_N = "1".
- This command only actives after R04H(PON) /R05H(PMES)

8.2.33 R60H (TCON): TCON setting

R60H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TCON	W	0	0	1	1	0	0	0	0	0	60H
1st Parameter	W	1	S2G[3]	S2G[2]	S2G[1]-	S2G[0]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	22h

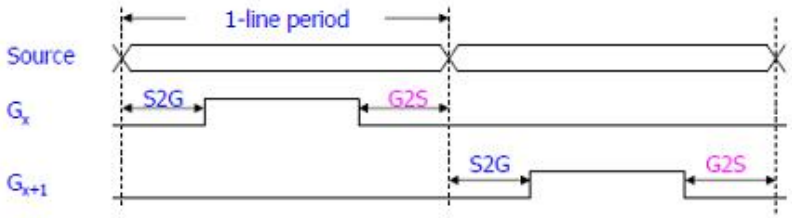
NOTE: "-" Don't care, can be set to VDD or GND level

Description

- The command define Non-overlap period of gate and source as below:
  1st Parameter:

Bit	Period
S2G[3:0]/G2S[3:0]	0000: 4 clock 0001: 8 clock 0010: 12 clock (default) 0011:16 clock 0100: 20 clock 0101: 24 clock 0110: 28 clock 0111: 32 clock 1000: 36 clock 1001: 40 clock 1010: 44 clock 1011: 48 clock 1100: 52 clock 1101: 56 clock 1110: 60 clock 1111: 64 clock

Period=660ns



Restriction

8.2.34 R61H (TRES): Resolution setting

R61H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TRES	W	0	0	1	1	0	0	0	0	1	61H
1st Parameter	W	1	HRES[7]	HRES[6]	HRES[5]	HRES[4]	HRES[3]	-	-	-	00h
2nd Parameter	W	1	Reserved byte								00h
3th Parameter	W	1	VRES[7]	VRES[6]	VRES[5]	VRES[4]	VRES[3]	VRES[2]	VRES[1]	VRES[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: When using register: Horizontal display resolution(source) = HRES Vertical display resolution(gate) = VRES Channel disable calculation: GD : First G active = G0; LAST active GD= first active +VRES[8:0] -1 SD : First active channel: =S0 ; LAST active SD= first active +HRES[7:3]*8-1 EX :128X272 GD: First G active = G0 LAST active GD= 0+272-1= 271; (G271) SD : First active channel: =S0 LAST active SD=0+16*8-1=127; (S127)
Restriction	

8.2.35 R65H (GSST): Gate/Source Start Setting Register

R65H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
GSST	W	0	0	1	1	0	0	1	0	1	65H
1st Parameter	W	1	S_start[7]	S_start[6]	S_start[5]	S_start[4]	S_start[3]	--	--	--	00h
2nd Parameter	W	1	-	-	-	gscan	-	-	-	-	00h
3rd Parameter	W	1	G_start[7]	G_start[6]	G_start[6]	G_start[4]	G_start[3]	G_start[2]	G_start[1]	G_start[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: 1.S_Start [8:3] describe which source output line is the first date line 2.G_Start[8:0] describe which gate line is the first scan line 3. gscan :Gate scan select 0: Normal scan 1: Cascade type 2 scan
Restriction	S_Start should be the multiple of 8

8.2.36 R68H (internal VOTP):

R68H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
REV	W	0	0	1	1	0	1	0	0	0	68H
1st Parameter	W	1	Internal VOTP[7:0]								

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: - The command can selective external/external VOTP Cmd.(0x68) + Parameter(0x00) : External VOTP (default) Cmd.(0x68) + Parameter(0xA7) : Internal VOTP
Restriction	

8.2.37 R70H (REV): REVISION register

R70H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
REV	W	0	0	1	1	1	0	0	0	0	70H
1st Parameter	R	1	REV[7]	REV[6]	REV[5]	REV[4]	REV[3]	REV[2]	REV[1]	REV[0]	FFh
2nd Parameter	R	1	REV[15]	REV[14]	REV[13]	REV[12]	REV[11]	REV[10]	REV[9]	REV[8]	FFh
3rd Parameter	R	1	Vendor ID				CHIP_REV				-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: The LUT_REV is read from: OTP Bank0 address =0xB4C~0xB4D OTP Bank1 address =0x174C~0x174D 3rd Parameter:

Bit	Description
3-0	CHIP_REV
7-4	Vendor ID: 'F'

Restriction	

8.2.38 R71H (FLG): Status register

R71H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
FLG	W	0	0	1	1	1	0	0	0	1	71H
1st Parameter	R	1	Con_fb	PTL_flag	I2C_ERR	II2C_ BUSYN	Data_flag	PON	POF	BUSY_N	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the IC status. Host can read this data to understand the IC status.

1st Parameter:

Bit	Function
7	Connector status feedback (high: connection failed), use DEBUG[5] & DEBUG[7]
6	Partial display status (high: partial mode)
5	I2C master error status
4	I2C master busy status (low active)
3	Driver has already received one frame data
2	PON 0: Not in PON mode 1: In PON mode
1	POF 0: Not in POF mode(default) 1: In POF mode
0	Driver busy status(low active)

Restriction

User can send this command in any time. It doesn't have restriction of BUSY_N.
The DEBUG[5] & DEBUG[7] is connector detect pin

8.2.39 R7FH(RRB):Read Reserved Bytes

R71H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
RBU	W	0	0	1	1	1	1	1	1	1	7FH
1st Parameter	R	1	User reserved byte0								-
2nd Parameter	R	1	User reserved byte1								
3rd~15th Parameter			User reserved byte2~14								
16th Parameter	R	1	User reserved byte15								

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: OTP reserved 16 bytes space which user could record more information such as lot number, LUT version….etc. And the address is 0xB80~0xB8F in bank 0 and 0x1780 ~0x178F in bank1 This command could read these information directly.
Restriction	

8.2.40 R80H (AMV): Auto Measure VCOM register

R80H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
AMV	W	0	1	0	0	0	0	0	0	0	80H
1st Parameter	W	1	-	-	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	10h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the IC status. Host can read this data to understand the IC status.

1st Parameter:

Bit	Function
0	AMVE: Auto Measure Vcom Setting 0: Auto measure VCOM disable (default) 1: Auto measure VCOM enable
1	AMV: Analog signal 0:Get Vcom value from R81h(default) 1:Get Vcom value in analog signal
2	AMVS: setting for Source output at AMV 0: Source output 0V during Auto Measure VCOM period. (default) 1: Source output VSHR during Auto Measure VCOM period.
3	XON: setting for all Gate ON of AMV 0: Gate normally scan during Auto Measure VCOM period. (default) 1: All Gate ON during Auto Measure VCOM period.
5-4	The sensing time of VCOM detection 00: 3s 01: 5s (default) 10: 8s 11: 10s

Restriction

This command only actives when BUSY_N = "1".

8.2.41 R81H (VV): VCOM Value register

R81H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VV	W	0	1	0	0	0	0	0	0	1	81H
1st Parameter	R	1	-	-	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	--

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command could get the VCOM value

1st Parameter:

Bit	Function
5-0	**Vcom value**

VCOM[5:0]		Voltage(V)	VCOM[5:0]		Voltage(V)	VCOM[5:0]		Voltage(V)
000000	00h	-0.1	010100	14h	-1.1	101000	28h	-2.1
000001	01h	-0.15	010101	15h	-1.15	101001	29h	-2.15
000010	02h	-0.2	010110	16h	-1.2	101010	2Ah	-2.2
000011	03h	-0.25	010111	17h	-1.25	101011	2Bh	-2.25
000100	04h	-0.3	011000	18h	-1.3	101100	2Ch	-2.3
000101	05h	-0.35	011001	19h	-1.35	101101	2Dh	-2.35
000110	06h	-0.4	011010	1Ah	-1.4	101110	2Eh	-2.4
000111	07h	-0.45	011011	1Bh	-1.45	101111	2Fh	-2.45
001000	08h	-0.5	011100	1Ch	-1.5	110000	30h	-2.5
001001	09h	-0.55	011101	1Dh	-1.55	110001	31h	-2.55
001010	0Ah	-0.6	011110	1Eh	-1.6	110010	32h	-2.6
001011	0Bh	-0.65	011111	1Fh	-1.65	110011	33h	-2.65
001100	0Ch	-0.7	100000	20h	-1.7	110100	34h	-2.7
001101	0Dh	-0.75	100001	21h	-1.75	110101	35h	-2.75
001110	0Eh	-0.8	100010	22h	-1.8	110110	36h	-2.8
001111	0Fh	-0.85	100011	23h	-1.85	110111	37h	-2.85
010000	10h	-0.9	100100	24h	-1.9	111000	38h	-2.9
010001	11h	-0.95	100101	25h	-1.95	111001	39h	-2.95
010010	12h	-1	100110	26h	-2	111010	3Ah	-3
010011	13h	-1.05	100111	27h	-2.05			

Restriction

8.2.42 R82H (VDCS): VCOM_DC Setting Register

R82H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VDCS	W	0	1	0	0	0	0	0	1	0	82H
1st Parameter	W	1	-	-	VDCS[5]	VDCS [4]	VDCS [3]	VDCS [2]	VDCS [1]	VDCS [0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command set the VCOM DC value. Driver will base on this value for VCM_DC.

1st Parameter:

Bit	Function
5-0	**VCOM value**

VCOM[5:0]		Voltage(V)	VCOM[5:0]		Voltage(V)	VCOM[5:0]		Voltage(V)
000000	00h	-0.1	010100	14h	-1.1	101000	28h	-2.1
000001	01h	-0.15	010101	15h	-1.15	101001	29h	-2.15
000010	02h	-0.2	010110	16h	-1.2	101010	2Ah	-2.2
000011	03h	-0.25	010111	17h	-1.25	101011	2Bh	-2.25
000100	04h	-0.3	011000	18h	-1.3	101100	2Ch	-2.3
000101	05h	-0.35	011001	19h	-1.35	101101	2Dh	-2.35
000110	06h	-0.4	011010	1Ah	-1.4	101110	2Eh	-2.4
000111	07h	-0.45	011011	1Bh	-1.45	101111	2Fh	-2.45
001000	08h	-0.5	011100	1Ch	-1.5	110000	30h	-2.5
001001	09h	-0.55	011101	1Dh	-1.55	110001	31h	-2.55
001010	0Ah	-0.6	011110	1Eh	-1.6	110010	32h	-2.6
001011	0Bh	-0.65	011111	1Fh	-1.65	110011	33h	-2.65
001100	0Ch	-0.7	100000	20h	-1.7	110100	34h	-2.7
001101	0Dh	-0.75	100001	21h	-1.75	110101	35h	-2.75
001110	0Eh	-0.8	100010	22h	-1.8	110110	36h	-2.8
001111	0Fh	-0.85	100011	23h	-1.85	110111	37h	-2.85
010000	10h	-0.9	100100	24h	-1.9	111000	38h	-2.9
010001	11h	-0.95	100101	25h	-1.95	111001	39h	-2.95
010010	12h	-1	100110	26h	-2	111010	3Ah	-3
010011	13h	-1.05	100111	27h	-2.05			

Restriction

8.2.43 R90H (PTL): Partial Window Register

R90H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTL	W	0	1	0	0	1	0	0	0	0	90H
1st Parameter	W	1	HRST[7:3]					0	0	0	00h
2nd Parameter	W	1	HRED[7:3]					1	1	1	00h
3rd Parameter	W	1	Reserved byte								00h
4th Parameter	W	1	VRST[7:0]								00h
5th Parameter	W	1	Reserved byte								00h
6th Parameter	W	1	VRED[7:0]								00h
7th Parameter	W	1	-	-	-	-		-	-	PT_SCAN	00h

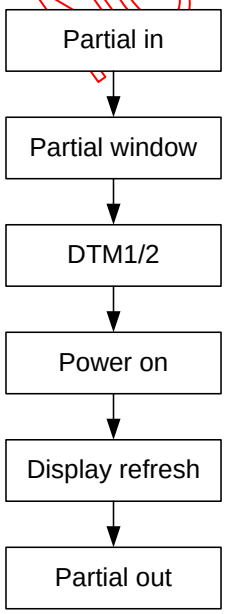
NOTE: "-" Don't care, can be set to VDD or GND level

Description

-This command sets partial window.

Name	Description
HRST[7:3]	Horizontal start channel bank. (value 00h~13h)
HRED[7:3]	Horizontal end channel bank. (value 00h~13h). HRED must be greater than HRST.
VRST[7:0]	Vertical start line. (value 000h~127h)
VRED[7:0]	Vertical end line. (value 000h~127h). VRED must be greater than VRST.
PT_SCAN	0: Gates scan only inside of the partial window. 1: Gates scan both inside and outside of the partial window. (default)

Partial display flow:



Restriction

8.2.44 R91H (PTIN): Partial In Register

R91H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTIN	W	0	1	0	0	1	0	0	0	1	91H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: This command makes the display enter partial mode.
Restriction	

8.2.45 R92H (PTOUT): Partial Out Register

R92H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTOUT	W	0	1	0	0	1	0	0	1	0	92H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: This command makes the display exit partial mode and enter normal mode.
Restriction	

8.2.46 R94H (CRCS): CRC Calculation in SRAM

R94H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CRCS	W	0	1	0	0	1	0	1	0	0	94H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: Start to calculate data which already be sent to SRAM. The data are included OTP Bank 0 (3K bytes)or OTP Bank 1 (3K bytes) information
Restriction	

8.2.47 R95H (CRCO): CRC Calculation in OTP

R95H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CRCO	W	0	1	0	0	1	0	1	0	1	95H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: Start to Calculate data which already be programmed in OTP.
Restriction	

8.2.48 R96H (CRCR): CRC status read

R96H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CRCR	R	0	1	0	0	1	0	1	1	0	96H
1st Parameter	R	1	CRC_MSB[7:0]								-
2nd Parameter	R	1	CRC_LSB[7:0]								-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: This command is used to read the CRC calculation result.
Restriction	

8.2.49 R97H (OTP key): Write OTP key

R97H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
OTP key	W	0	1	0	0	1	0	1	1	1	97H
1st Parameter	W	1	OTP Key_MSB[7:0]								-
2nd Parameter	W	1	OTP Key_LSB [7:0]								-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: This command is used to unlock the OTP read function. The key must be same with the key (in 0xB76, 0xB77 OTP. And the OTP key could be decided by customer.
Restriction	

8.2.50 RA0H (PGM): Program Mode

RA0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTIN	W	0	1	0	1	0	0	0	0	0	A0H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is issued, the chip would enter the program mode. The mode would return to standby by hardware reset.
Restriction	This command only actives when BUSY_N = "1".

8.2.51 RA1H (APG): Active Program

RA1H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
APG	W	0	1	0	1	0	0	0	0	1	A1H

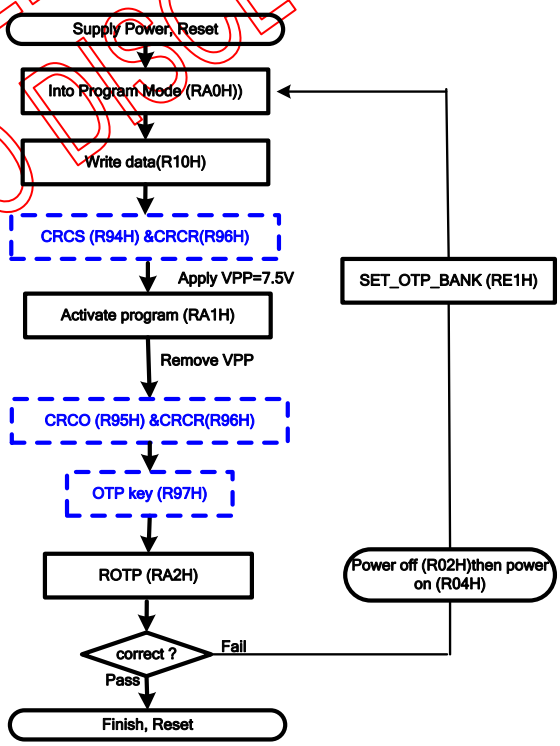
NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is transmitted, the programming state machine would be activated.
Restriction	The BUSY flag would change state from 0 to 1 while the programming is completed.

8.2.52 RA2H (ROTP): Read OTP Data

RA2H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
ROTP	W	0	1	0	1	0	0	0	1	0	A2H
1st Parameter	R	1	Dummy								-
2nd Parameter	R	1	The data of address 0x000 in the OTP								-
3rd Parameter	R	1	The data of address 0x001 in the OTP								-
4th Parameter	R	1	:								-
5th Parameter	R	1	The data of address (n-1) in the OTP								-
6th~(m-1)th Parameter	R	1	…..								-
mth Parameter	R	1	The data of address (n) in the OTP								-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: The command is used for reading the content of OTP for checking the data of programming. The value of (n) is depending on the amount of programmed data, the max address = 0xFFF. OTP flow  The sequence of programming OTP
Restriction	This command only actives when BUSY_N = "1".

8.2.53 RE0H (CCSET): Cascade Setting

RE0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CCSET	W	0	1	1	1	0	0	0	0	0	E0H
1st Parameter	W	1	-	-	-	-	-	-	TSFIX	CCEIN	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

This command is used for cascade.

1st Parameter:

Bit	Name	Description
0	CCEIN	Output clock enable/disable. 0: Output 0V at CL pin. (default) 1: Output clock at CL pin for slave chip.
1	TSFIX	Let the value of slave's temperature is same as the master's. 0: Temperature value is defined by internal temperature sensor/external LM75. (default) 1: Temperature value is defined by TS_SET [7:0] registers.

Restriction

8.2.54 RE1H (SET_OTP_BANK): Set OTP program bank

RE1H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
SET_OTP_BANK	W	0	1	1	1	0	0	0	0	1	E1H
1st Parameter	W	1	-	-	-	-	-	-	LUT_bank0	reg_bank0	03h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-This command is used to set program bank for registers and LUTs

OTP bank 0 (3K Bytes)		OTP bank 1 (3K Bytes)	
Address(Hex)	Content	Address(Hex)	Content
0x000~0x00B	Temp. segment	0xC00~0xC0B	Temp. segment
0x00C	Vcom DC voltage	0xC0C	Vcom DC voltage
0x00D~0x0BFF	LUTs / Reserved	0xC0D~0x17FF	LUTs / Reserved

1st Parameter:

Bit	Name	Description
0	reg_bank0	0: Program "Temp. segment" and "Default Setting" in bank 1 1: Program "Temp. segment" and "Default Setting" in bank 0
1	LUT_bank0	0: Program "LUTs" in bank 1 1: Program "LUTs" in bank 0

After this command is transmitted, the programming state machine would be activated.

Restriction

The BUSY flag would change state from 0 to 1 while the programming is completed

8.2.55 RE3H (PWS): Power Saving Register

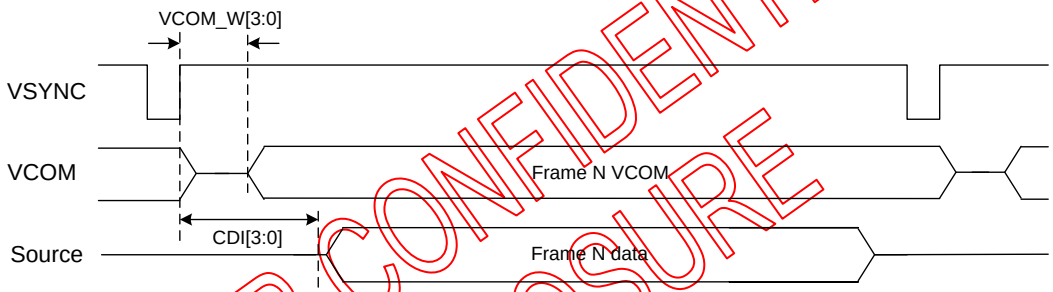
RE3H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWS	W	0	1	1	1	0	0	0	1	1	E3H
1st Parameter	W	1	VCOM_W[3:0]				SD_W[3:0]				00h

NOTE: "-" Don't care, can be set to VDD or GND level

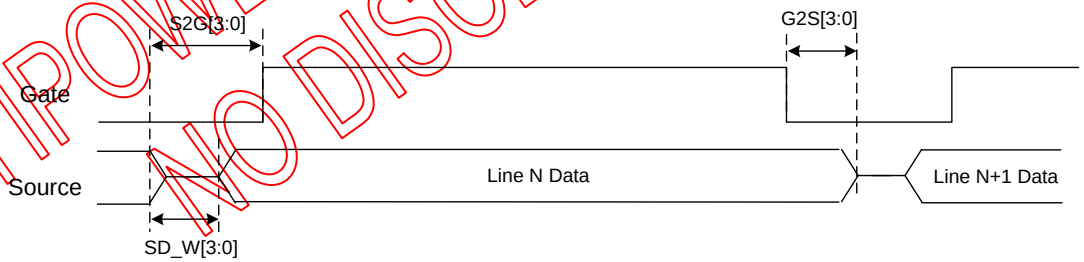
Description

- This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W: VCOM power saving width (unit = line period)



SD_W: Source power saving width (unit = 660nS)



Restriction

8.2.56 RE4H (LVSEL): LVD Voltage Select Register

RE4H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LVSEL	W	0	1	1	1	0	0	1	0	0	E4H
1st Parameter	W	1	-	-	-	-	-	-	LVD_SEL[1:0]		03h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	LVD_SEL[1:0]: Low Power Voltage selection
Restriction	

Bit 0-1	Description
LVD_SEL[1:0]	LVD value
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5 V

8.2.57 RE5H (TSSET): Force Temperature

RE5H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSSET	W	0	1	1	1	0	0	1	0	1	E5H
1st Parameter	W	1	TS_SET[7]	TS_SET[6]	TS_SET[5]	TS_SET[4]	TS_SET[3]	TS_SET[2]	TS_SET[1]	TS_SET[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: This command is used to fix the temperature value of master and slave chip in cascade
Restriction	

8.3 Register Restriction

Following table will indicate the register restriction:

Register	Refresh restriction	BUSY_N flag
R00H(PSR)	X	No action
R01H(PWR)	X	No action
R02H(POF)	X	Flag
R03H(PFS)	X	No action
R04H(PON)	X	Flag
R05H(PMES)	X	No action
R06H(BTST)	X	No action
R07H(DSLP)	X	Flag
R10H(DTM1)	X	No action
R11H(DSP)	Valid only read	Flag
R12H(DRF)	X	Flag
R13H(DTM2)	X	No action
R17H(AUTO)	Valid in standby	Flag
R20H(LUTC)	X	No action
R21H(LUTWW)	X	No action
R22H(LUTBW/LUTR)	X	No action
R23H(LUTWB/LUTW)	X	No action
R24H(LUTBB/LUTB)	X	No action
R26H(SET_GROUP)	X	No action
R2AH(LUTOPT)	X	No action
R30H(PLL)	X	No action
R40H(TSC)	Valid only read	Flag
R41H(TSE)	X	No action
R42H(TSW)	X	Flag
R43H(TSR)	Valid only read	Flag
R44H(PBC)	Valid only read	Flag
R50H(CDI)	X	No action
R51H(LPD)	Valid only read	Flag
R60H(TCON)	X	No action
R61H(TRES)	X	No action
R65H(TSGS)	X	No action
R70H(REV)	Valid only read	No action
R71H(FLG)	Valid only read	No action
R80H(AMV)	X	Flag
R81H(VV)	Valid	No action
R82H(VDCS)	X	No action
R90H(PTL)	X	No action
R91H(PTIN)	X	No action
R92H(PTOUT)	X	No action
RA0H(PGM)	X	No action
RA1H(APG)	X	Flag
RA2H(ROTP)	X	Flag
RE0H(CCSET)	X	No action
RE3H(PWS)	X	No action
RE1H(SET_OTP_BANK)	X	No action
RE4H(LVSEL)	X	No action
RE5H(TSSET)	X	No action

9. FUNCTION DESCRIPTION

9.1 Power On/Off and DSLP Sequence

In order to prevent IC fail in power on resetting, the power sequence must be followed as below.

Power on Sequence

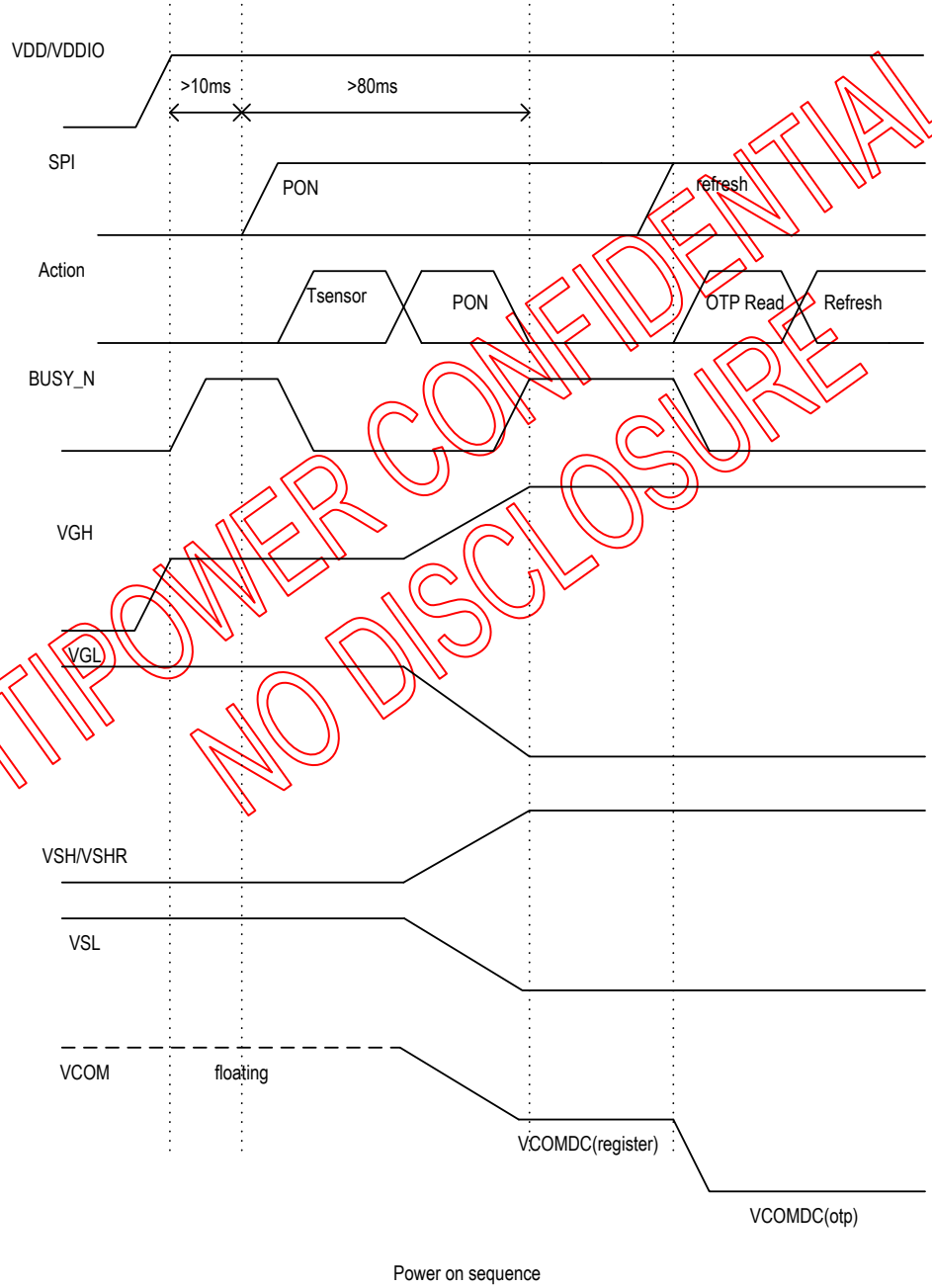


Figure 1: Power on sequence

Power off Sequence

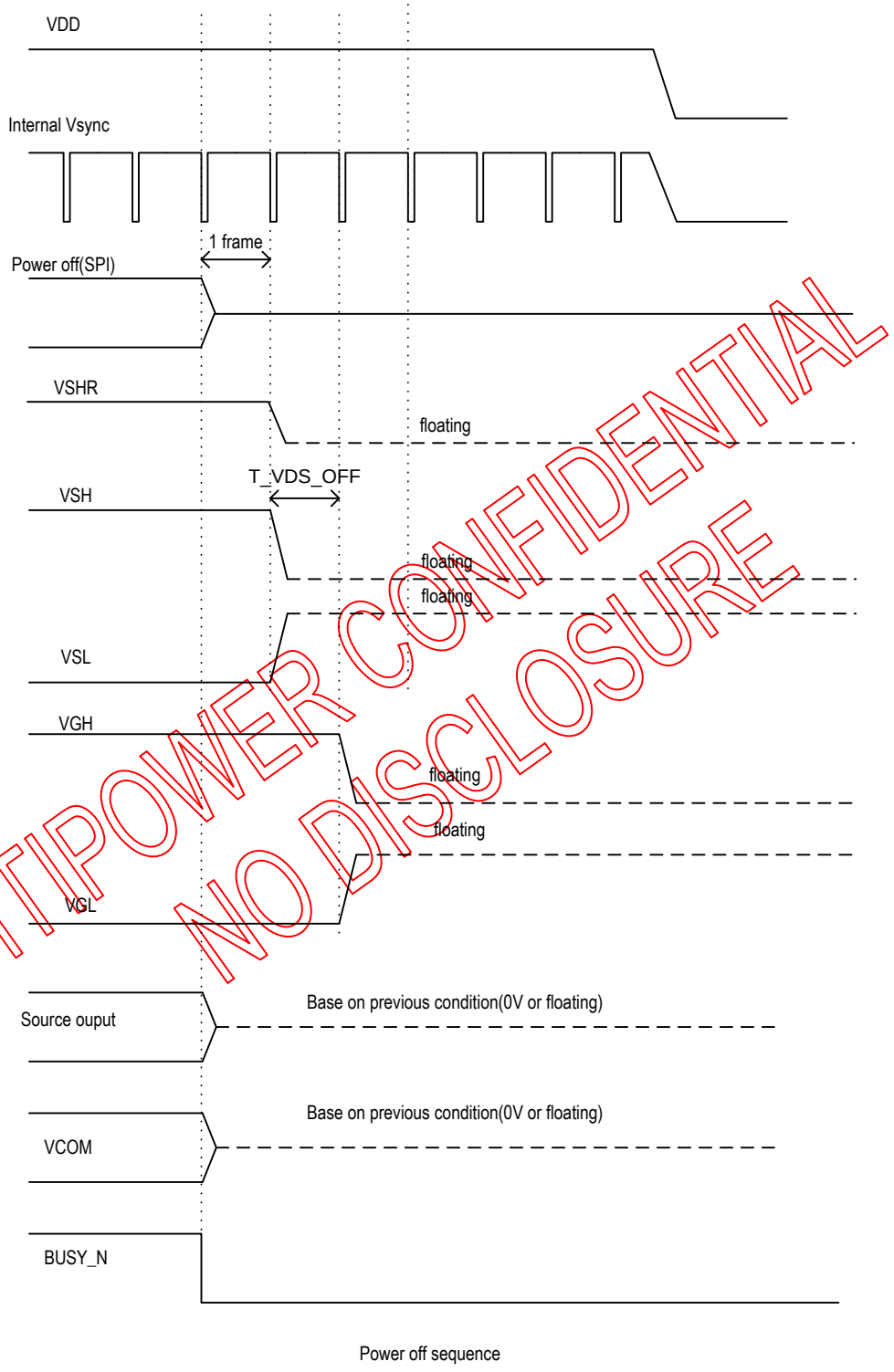


Figure 2: Power off sequence

DSLP sequence

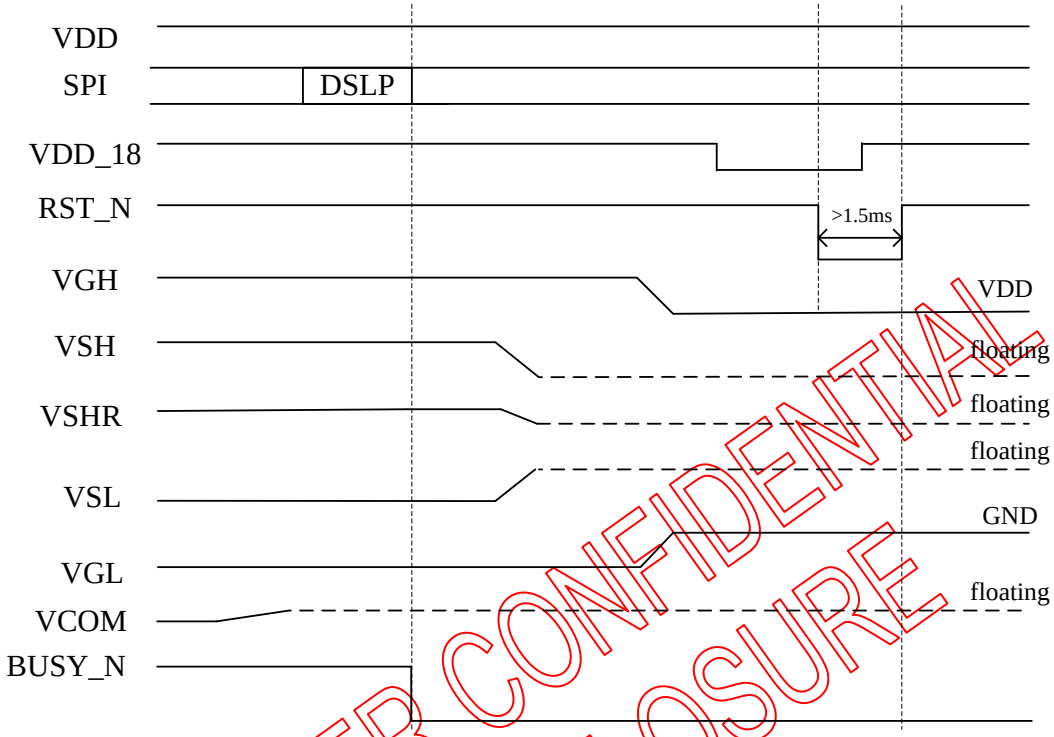


Figure 3: DSLP sequence

9.2 OTP LUT Definition

The OTP size would be 6144 Byte included temperature segment setting and 12 set waveform (maximum).

If TEMP ≦ Boundary0, use TR0 WF

If Boundary0 < TEMP ≦Boundary1, use TR1

If Boundary1 < TEMP ≦ Boundary2, use TR2

……

OTP bank 0 (3K bytes)		OTP bank 1 (3K bytes)	
Address(Hex)	Content	Address(Hex)	Content
0x000	Check code (0xA5)	0xC00	Check code (0xA5)
0x001	Temp. Boundary 0	0xC01	Temp. Boundary 0
0x002	Temp. Boundary 1	0xC02	Temp. Boundary 1
0x003	Temp. Boundary 2	0xC03	Temp. Boundary 2
0x004	Temp. Boundary 3	0xC04	Temp. Boundary 3
0x005	Temp. Boundary 4	0xC05	Temp. Boundary 4
0x006	Temp. Boundary 5	0xC06	Temp. Boundary 5
0x007	Temp. Boundary 6	0xC07	Temp. Boundary 6
0x008	Temp. Boundary 7	0xC08	Temp. Boundary 7
0x009	Temp. Boundary 8	0xC09	Temp. Boundary 8
0x00A	Temp. Boundary 9	0xC0A	Temp. Boundary 9
0x00B	Temp. Boundary 10	0xC0B	Temp. Boundary 10
0x00C~0x0FB	TR0 WF	0xC0C~CFB	TR0 WF
0x0FC~0x1EB	TR1 WF	0xCFC~0xDEB	TR1 WF
0x1EC~0x2DB	TR2 WF	0xDEC~0xEDB	TR2 WF
0x2DC~0x3CB	TR3 WF	0xEDC~0xFCB	TR3 WF
0x3CC~0x4BB	TR4 WF	0xFCC~0x10BB	TR4 WF
0x4BC~0x5AB	TR5 WF	0x10BC ~0x11AB	TR5 WF
0x5AC~0x69B	TR6 WF	0x11AC~0x129B	TR6 WF
0x69C~0x78B	TR7 WF	0x129C~0x138B	TR7 WF
0x78C~0x87B	TR8 WF	0x138C~0x147B	TR8 WF
0x87C~0x96B	TR9 WF	0x147C~0x156B	TR9 WF
0x96C~0xA5B	TR10 WF	0x156C~0x165B	TR10 WF
0xA5C~0xB4B	TR11 WF	0x165C~0x174B	TR11 WF
0xB4C~0xB4D	LUT version	0x174C~0x174D	LUT version
0xB4E~0XB4F	Reserved	0x174E~0x174F	Reserved
0xB50~0xB7D	Default setting	0x1750~0x177D	Default setting
0xB7E~0xB7F	Reserved	0x177E~0x177F	Reserved
0xB80~0xB8F	User reserved 0~15	0x1780~0x178F	User reserved 0~15

9.2.1 LUT Format in OTP

There are 12 TRs (temperature range) in a bank. Each TR has independent frame rate, voltage, XON settings and LUTs. The format of LUT is different in different mode. In BWR mode, there are only 4 LUTs including LUTC, LUTR, LUTW and LUTB in TRs. All LUT have 8 groups in BWR mode. And the extra options, EOPT is imported to define the end state of source output level. In BW mode, there are 5 LUTs including LUTC, LUTWW, LUTBW, LUTWB and LUTBB in TRs. All LUT have 6 groups in BW mode.

	BWR Mode (BWR=0)		BW Mode (BWR=1)	
	Address(Hex)	Content	Address(Hex)	Content
TR0	0x00C	VDCS	0x00C	VDCS
	0x00D	VGH/L voltage	0x00D	VGH/L voltage
	0x00E	VSH voltage	0x00E	VSH voltage
	0x00F	VSL voltage	0x00F	VSL voltage
	0x010	VSHR voltage	0x010	VSHR voltage
	0x011	EOPT	0x011	EOPT
	0x012	STATE XON[7:0]	0x012	STATE XON[7:0]
	0x013	STATE XON[15:8]	0x013	STATE XON[15:8]
	0x014~0x01B	8 Groups frame rate	0x014~0x019	6 Groups frame rate
	0x01C~0x053	LUTC (8 groups)	0x01A~0x043	LUTC (6 groups)
	0x054~0x08B	LUTR (8 groups)	0x044~0x06D	LUTWW (6 groups)
			0x06E~0x097	LUTBW (6 groups)
	0x08C~0x0C3	LUTW (8 groups)	0x098~0x0C1	LUTWB (6 groups)
			0x0C2~0x0EB	LUTBB (6 groups)
	0x0C4~0x0FB	LUTB (8 groups)	0x0EC~0x0FB	reserved

9.2.2 Default Setting Format in OTP

	Addr.(dec)	Addr.(hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	2896	B50	Enable OTP Setting (0xA5)							
R00H-1	2897	B51	RES[1:0]		REG_EN	BWR	UD	SHL	SHD_N	RST_N
R01H	2898	B52	-	-	-	-	-	-	VDS_EN	VDG_EN
	2899	B53		-	-	VCOM_HV	VGHL_LV[3:0]			
	2900	B54	-	-	VSH[5:0]					
	2901	B55	-	-	VSL[5:0]					
	2902	B56	OPTEN	VSHR[6:0]						
R03H	2903	B57	-	-	T_VDS_OFF[1:0]		T_VSHR_OFF[1:0]		-	-
R06H	2904	B58	BT_PHA[7:0]							
	2905	B59	BT_PHB[7:0]							
	2906	B5A	-	-	BT_PHC[5:0]					
RE4H	2909	B5D	-	-	-	-	-	-	LVD_SEL[1:0]	
RE3H	2910	B5E	VCOM_W[3:0]				SD_W[3:0]			
--	2911	B5F	Reserved							
R00H-2	2912	B60	-	-	-	VCMZ	TS_AUTO	VGLTIEG	NORG	VC_LUTZ
R31H	2913	B61								PLL option
R26H	2914	B62	-		-	-		-	GROUP_SEL[1:0]	
R30H	2915	B63	-	-	M[2:0]			N[2:0]		
R41H	2916	B64	TSE	-	TO[5:0]					
R42H	2917	B65	WATTR[7:0]							
	2918	B66	WMSB[7:0]							
	2919	B67	WLSB[7:0]							
R50H	2920	B68	VBD[1:0]		DDX[1:0]		CDI[3:0]			
R60H	2921	B69	S2G[3:0]				G2S[3:0]			
--	2922	B6A	Reserved							
R61H	2923	B6B	HRES[7:3]					-	-	-
	2924	B6C		-	-	-	-	-	-	VRES[8]
	2925	B6D	VRES[7:0]							
R80H	2926	B6E			AMVT[1:0]		XON	AMVS	AMV	AMVE
	2927	B6F	Reserved							
RE0H	2928	B70	-	-	-	-	-	-	TSFIX	CCEIN
RE5H	2929	B71	TS_SET[7:0]							
R68H	2930	B72	reserved							
R65H	2931	B73	S_start[7:3]					-	-	-
	2932	B74				gscan				G_start[8]
	2933	B75	G_start[7:0]							
	2934	B76	OTP Key_MSB[7:0]							
	2935	B77	OTP Key_LSB[7:0]							
RE1H	2936	B78	-	-	-	-	-	-	LUT_bank0	REG_bank0
Slave										
R00H	2937	B79	slv_res[1:0]		slv_reg_en	slv_bwr	slv_ud	slv_shl	slv_shd_n	slv_rst_n
	2938	B7A	-	-	-	slv_vcmz	slv_ts_auto	slv_vgltieg	slv_norg	slv_vc_lutz
R62H	2939	B7B	slv_sstart[7:3]					-	-	-
	2940	B7C	-	-	-	slv_gscan	-	-	-	slv_gstart[8]
	2941	B7D	slv_gstart[7:0]							
--	2942~2943	B7E~B7F	Reserved							

	2944~2959	B80~B8F	User reserved byte 0~15

9.3 Data transmission waveform

Example1: LUT all states complete or phase number=0, the driver will send 2 frame VCOM and data to 0 v.

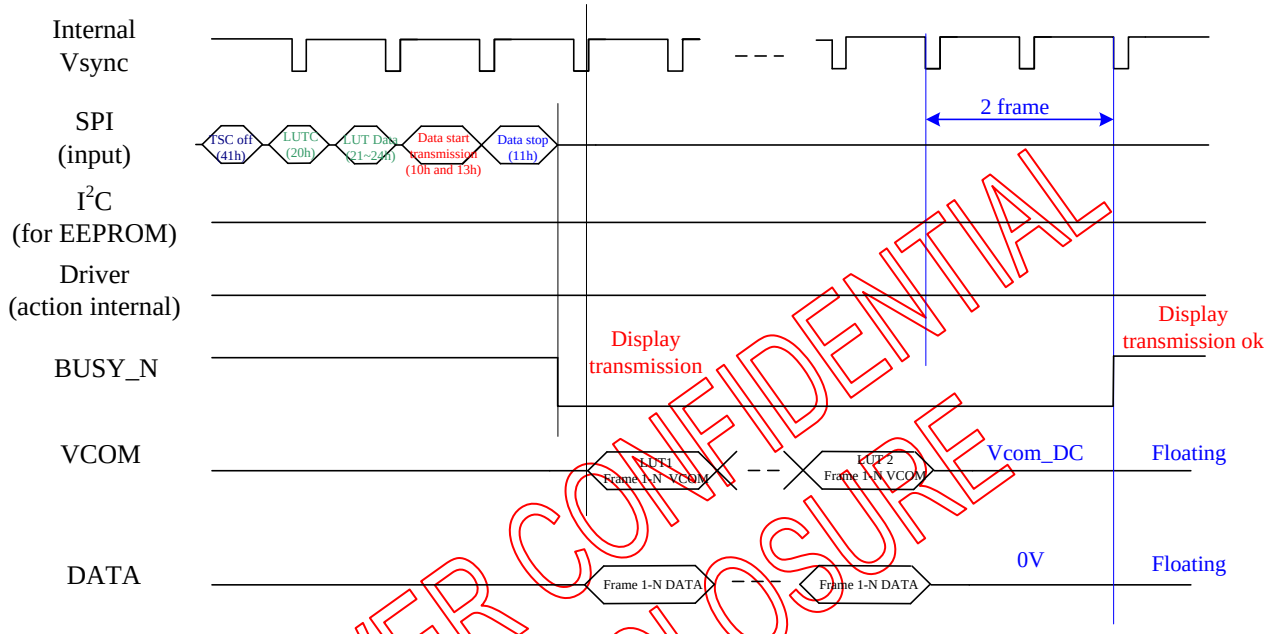


Figure 3: Data transmission example1 waveform

Example2: While level selection in LUT is “11”, the driver will float VCOM and data. (EOPT=0)

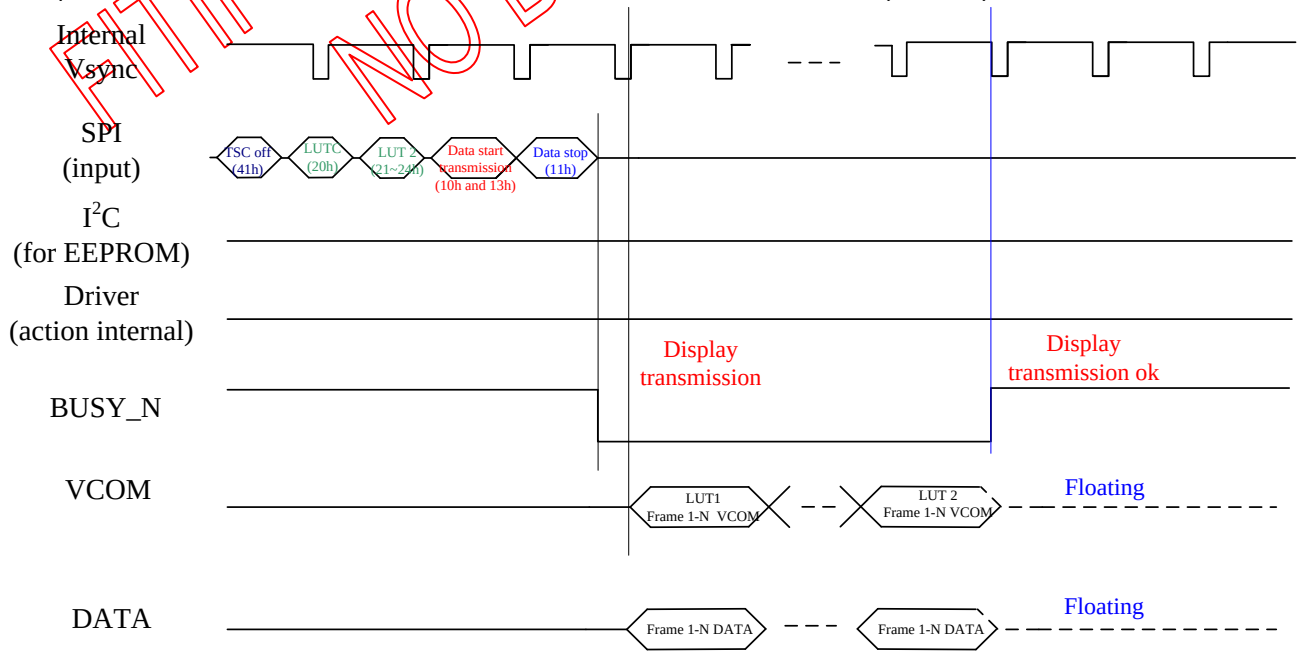


Figure 4: Data transmission example2 waveform

Example3: While level selection in LUT is “11”, the driver will float VCOM and keep last frame data. (EOPT=1)

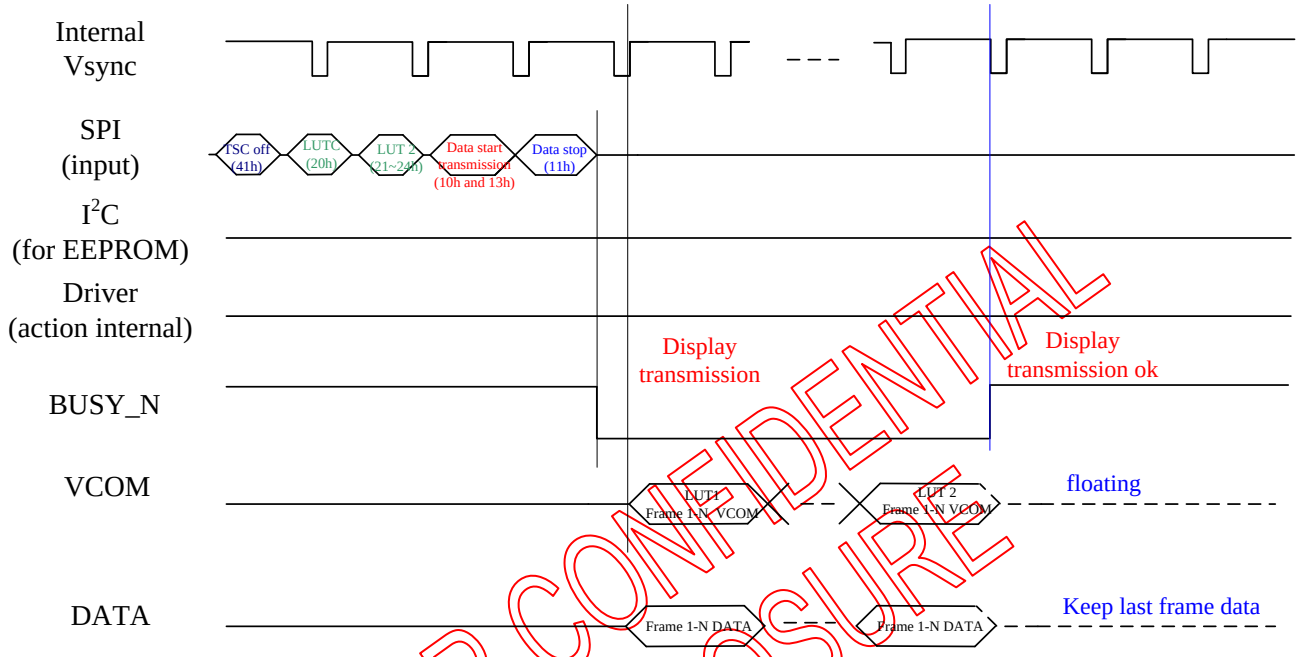


Figure 5: Data transmission example3 waveform

9.5 Display refresh waveform

Example1: LUT all states complete or phase number=0, the driver will send 2 frame VCOM and data to 0 v.

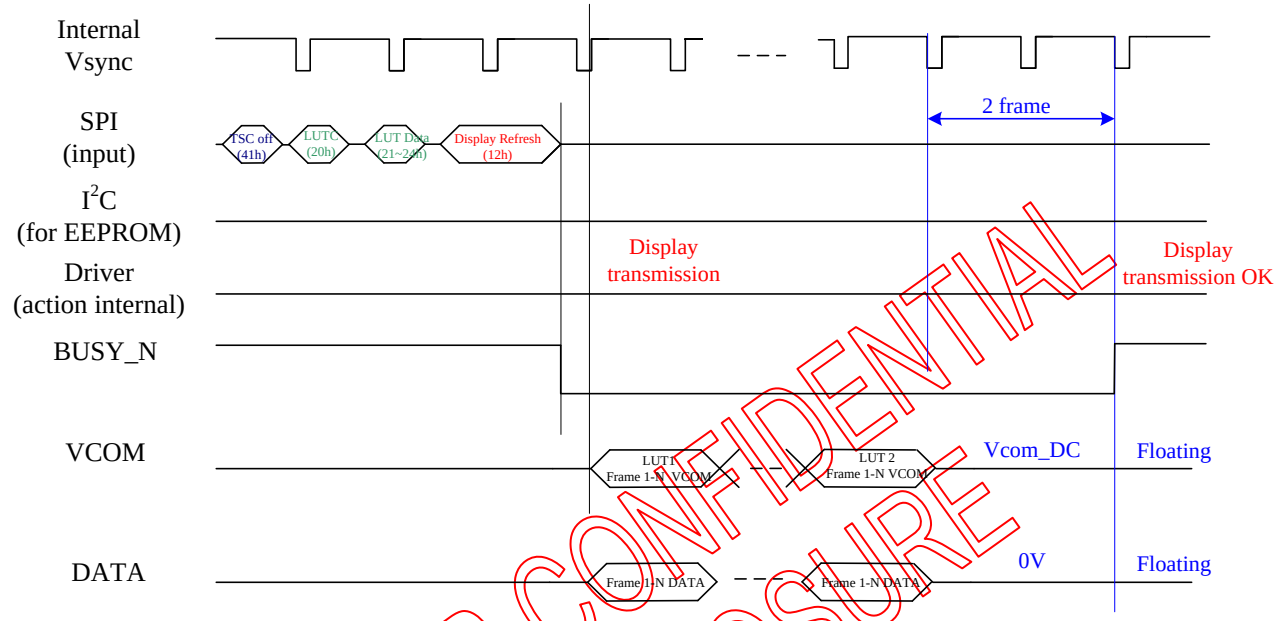


Figure 6: Display refresh example1 waveform

Example2: While level selection in LUT is “11”, the driver will float VCOM and data. (EOPT=0)

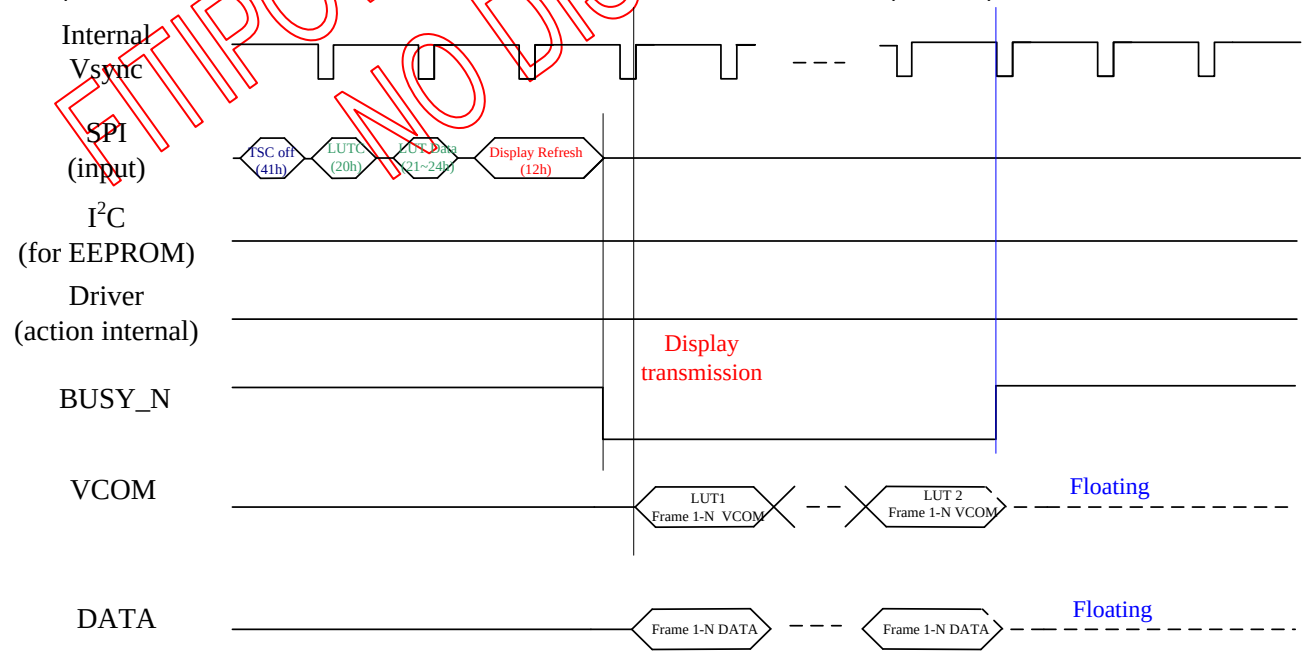


Figure 7: Display refresh example2 waveform

Example3: While level selection in LUT is “11”, the driver will float VCOM and keep last frame data. (EOPT=1)

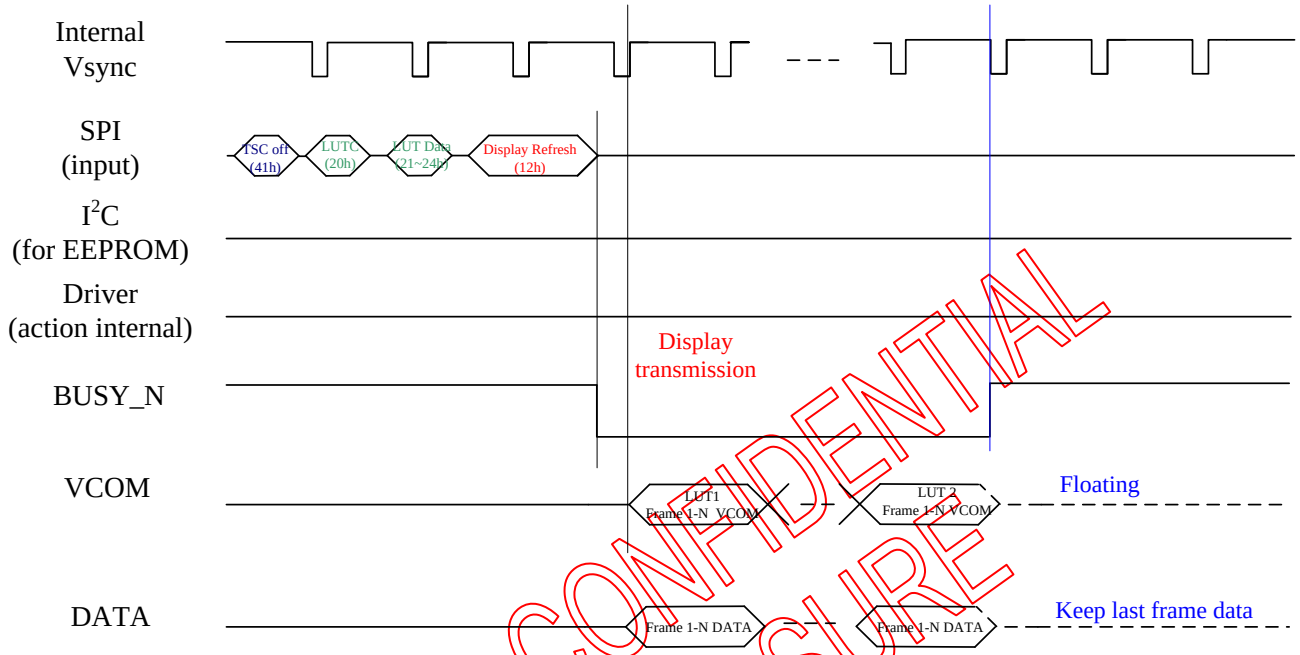


Figure 8: Display refresh example3 waveform

10. ELECTRICAL SPECIFICATIONS

10.1 Absolute Maximum Rating

Parameter	Symbol	Min.	Max.	Unit
Logic supply voltage	VDD, AVDD,VDDIO, VDD1,VPP	-0.3	+6.0	V
Digital input voltage	VI	-0.3	VDDIO+0.3	V
Supply range	VGH-VGL	VGL-0.3	VGH+0.3	V
Analog supply	VSH	+6.4	+15	V
Analog supply	VSL	-15	-6.4	V
Analog supply	VSHR	2.4	+15	
Supply voltage	VGH	+15	+20	V
Supply voltage	VGL	-20	-15	V
Storage temperature	T_{STG}	-55	125	℃

Note:
Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied.
Exposing device to the absolute maximum ratings in a long period of time may degrade the device and affect its reliability.

10.2 Digital DC Characteristic

DC electrical characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
IO Supply Voltage	VDDIO	2.3	3.3	3.6	V	
Digital/Analog supply voltage	VDD	2.3	3.3	3.6	V	
DCDC power input voltage	AVDD	2.3	3.3	3.6	V	
1.8V output voltage	VDD_18	1.62	1.8	1.98		
1.8V input voltage	VDD_18	1.62	1.8	1.98		
OTP program power	VOTP	7.25	7.5	7.75		
Digital ground	VSS		0			
DCDC ground	VSSP		0			
Low Level Input Voltage	Vil	GND	-	0.3xVDD	V	Digital input pins
High Level Input Voltage	Vih	0.7xVIO	-	VIO	V	Digital input pins
High Level Output Voltage	Voh	VIO-0.4	-	-	V	Digital output pins; IOH = 400μA
High Level Output Voltage	Vohd	VDD1-0.4	-	-	V	Digital output pins; IOH = 400μA DRVD, DRVU
Low Level Output Voltage	Vol	GND	-	GND+0.4	V	Digital output pins; IOL = -400μA
Input Leakage Current	Iin	-1.0	-	+1.0	uA	Digital input pins, except pull-up, pull-down pin
Pull-up/down impedance	Rin	-	200K		ohm	
Digital Stand-by Current (power off mode)	IstVDD*	-	0	1	uA	All stopped
Digital Operating Current	IVDD*	-	0.5	2.0	mA	
IO Stand-by Current (power off mode)	IstVDDIO*	-	0.4	1.0	uA	All stopped
IO Operating Current	IVDDIO*	-	-	0.2	mA	No load
Operating Current	IVDD1*	-	-	TBD	mA	
Operating temperature	T_{op}	-30	-	85	℃	

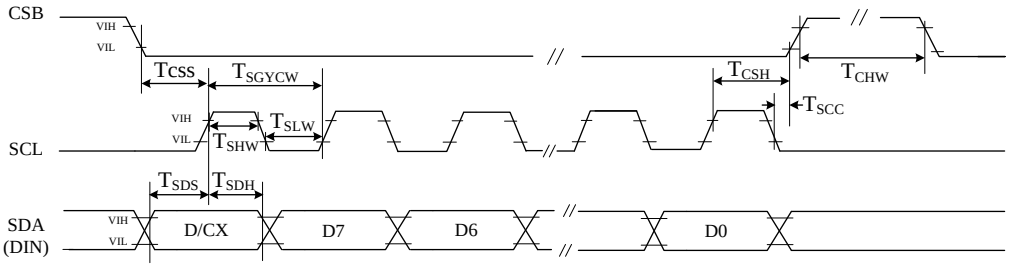
NOTE: typ. and max. values to be confirmed by design

10.3 Analog DC Characteristics

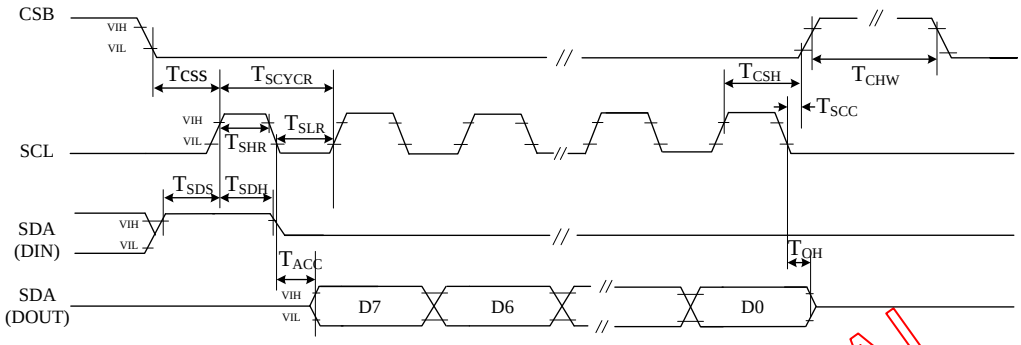
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Positive Source voltage	VSH		15		V	For source driver/VCOM
Positive Source voltage dev	dVSH	-200	0	+200	mV	
Negative Source voltage	VSL		-15		V	For source driver/VCOM
Negative Source voltage dev	dVSL	-200	-	+200	mV	
Positive Source voltage for Red dev.	dVSHR	-200	-	+200	mV	
VCOM voltage dev.	dVCOM	-200	-	+200	mV	
Dynamic Range of Output	Vdr	0.1	-	VSH-0.1	V	
Voltage Range of VGH - VGL	VGH-VGL	-	-	40	V	
Negative Gate voltage	VGL	-15	-	-20	V	For gate driver
Positive Gate voltage	VGH	15		20	V	For gate driver
Positive HV Stand-by Current (power off mode)	IstVGH*	-	0	0.2	uA	Include VSH power With load
Positive HV Operating Current	IVGH*	-	0.7	1.1	mA	Include VSH power With load all SD=L VCOM external resistor divider not included
Positive HV Operating Current	IVGH*	-	0.8	1.2	mA	Include VSH power With load all SD=H VCOM external resistor divider not included
Negative HV Stand-by Current (power off mode)	IstVGL*	-	0	0.2	µA	Include VSH power With load
Negative HV Operating Current	IVGL*	-	0.8	1.2	mA	Include VSL power With load all SD=L
Negative HV Operating Current	IVGL*	-	0.9-	1.3	mA	Include VSL power With load all SD=H
VINT1 Stand-by Current (power off mode)	IstVINT1*		0	0.01	µA	
VINT1 Operating Current	IVINT1*			0.3	mA	
Voltage	IVINT1*			0.3	mA	

10.4 AC Characteristics

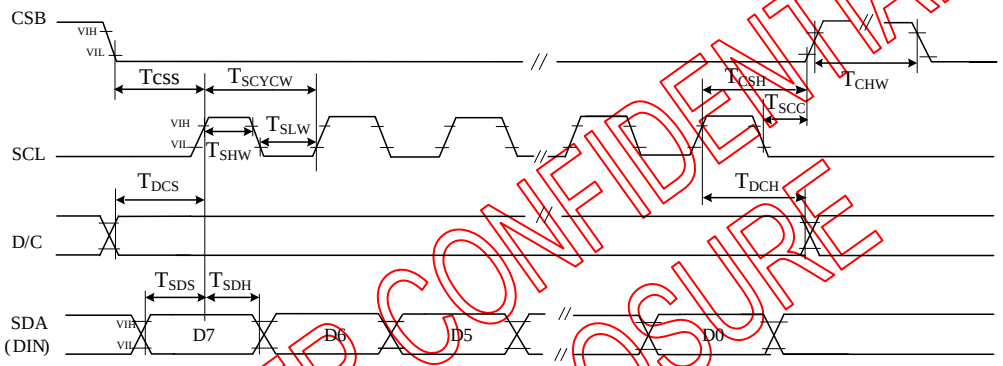
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
SERIAL COMMUNICATION						
CSB	T_{CSS}	60			ns	Chip select setup time
	T_{CSH}	65			ns	Chip select hold time
	T_{SCC}	20			ns	Chip select CSB setup time
	T_{CHW}	40			ns	Chip select setup time
SCL	T_{SCYCW}	100			ns	Serial clock cycle (Write)
	T_{SHW}	35			ns	SCL “H” pulse width (Write)
	T_{SLW}	35			ns	SCL “L” pulse width (Write)
	T_{SCYCR}	150			ns	Serial clock cycle (Read)
	T_{SHR}	60			ns	SCL “H” pulse width (Read)
	T_{SLR}	60			ns	SCL “L” pulse width (Read)
SDA (DIN) (DOUT)	T_{SDS}	30			ns	Data setup time
	T_{SDH}	30			ns	Data hold time
	T_{ACC}			50	ns	Access time
	T_{OH}	15			ns	Output disable time
D/C	T_{DCS}	20			ns	DC setup time
	T_{DCH}	20			ns	DC hold time
RC loading						
Source driver output loading	RL_S		1.96k		Ω	
	CL_S		31.11		pf	
Gate driver output loading	RL_S		2.78k		Ω	
	CL_S		27.68		pf	
VCOM output loading	RL_com		61.26		Ω	
	CL_com		3365.7		pf	



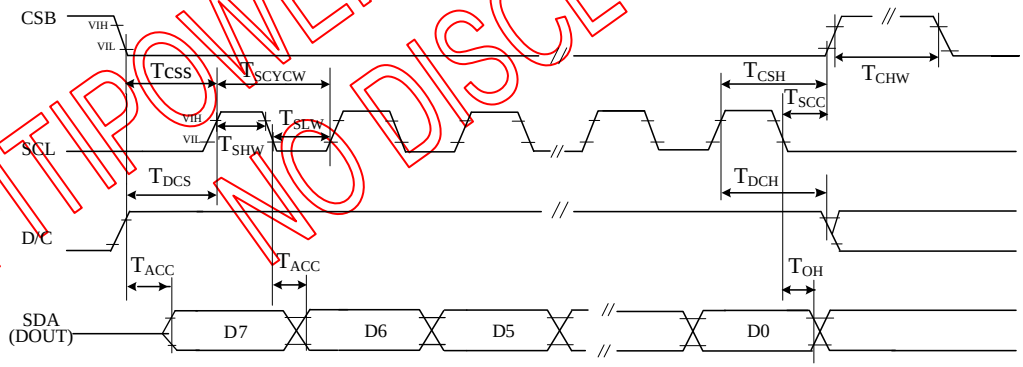
3 pin serial interface characteristics (write mode)



3 pin serial interface characteristics (read mode)



4 pin serial interface characteristics(write mode)



4 pin serial interface characteristics(read mode)

Figure 8: SPI interface timing

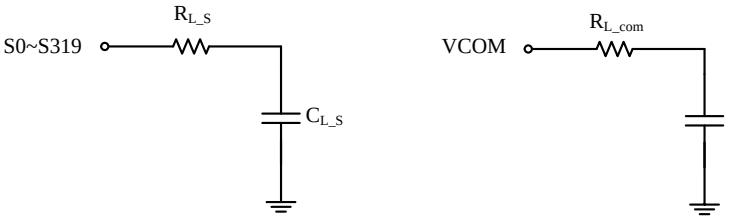
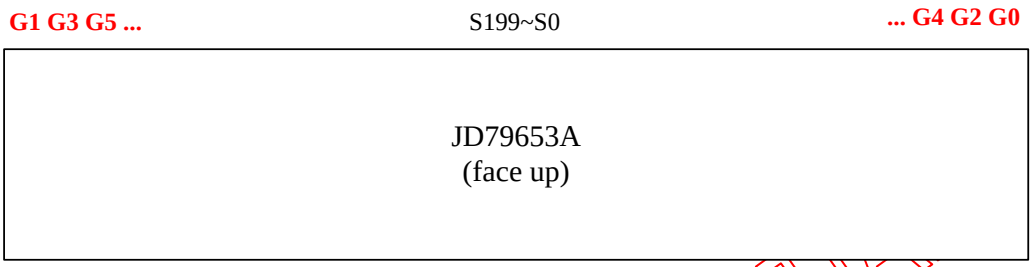


Figure 9: RC loading

11. CHIP OUTLINE DIMENSIONS

11.1 Circuit/Bump View



Die Size:	**9910um * 1028um**
Die Thickness:	230 μm ± 20μm (Polish)
Die TTV:	(D_{MAX} – D_{MIN}) within die ≤ 2μm
Bump Height:	12 μm ± 2μm
	(H_{MAX} – H_{MIN}) within die ≤ 2μm
Hardness:	75 Hv ±25Hv
Coordinate origin:	Chip center

12. REVISION HISTORY

Revision	Content	Page	Date
0.01	new issue	-	2019/05/06