SSD1607

Product Preview

Active Matrix EPD 200 x 300
Display Driver with Controller

Appendix: IC Revision history of SSD1607 Specification

Revision	Change Items	Effective Date
0.10	Product Preview Release	06-Sep-12
0.20	Revised Command Table	12-Sep-12

CONTENTS

TABLES

FIGURES

1 GENERAL DESCRIPTION

The SSD1607 is a CMOS active matrix bistable display driver with controller. It consists of 200 source outputs, 300 gate outputs, 1 VCOM and 1 VBD for border that can support a maximum display resolution 200x300 for single chip application. In addition, the SSD1607 has a cascade mode that can support higher display resolution.

The SSD1607 embeds booster, regulators and oscillator. Data/Commands are sent from general MCU through the hardware selectable 6800-/8080-series compatible Parallel Interface or Serial Peripheral Interface.

2 FEATURES

- Design for dot matrix type active matrix EPD display
- Resolution: 200 source outputs; 300 gate outputs; 1 VCOM; 1VBD for border
- Power supply
  - VCI: 2.4 to 3.7V
  - VDDIO: Connect to VCI
  - VDD: 1.8V, regulate from VCI supply

- Gate driving output voltage:
  - 2 levels output (VGH, VGL)
  - Max 42Vp-p
  - VGH: 15V to 22V;
  - VGL: -20V to -15V
  - Voltage adjustment in steps of 500mV.

- Source / VBD driving output voltage:
  - 3 levels output (VSH, VSS, VSL)
  - VSH: 10V to 17V
  - VSL: -10V to -17V
  - Voltage adjustment in steps of 500mV

- VCOM output voltage
  - -4V to 0.2V in 20mV resolution
  - 8 bits Non-volatile memory (OTP) for VCOM adjustment

- Source and gate scan direction control
- Low current deep sleep mode
- On chip display RAM with double display buffer [200x300 / 8 * 2 = 15000Byte]
- Waveform settings can be programmed and stored in On-chip OTP
- Programmable output waveform allowing flexibility for different applications / environments.
- Built in VCOM sensing
- On-chip oscillator.
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage.
- Cascade mode to support higher display resolution.
- I2C Single Master Interface to read external temperature sensor reading
- 8-bits Parallel (6800 & 8080), Serial peripheral interface available
- Available in COG package

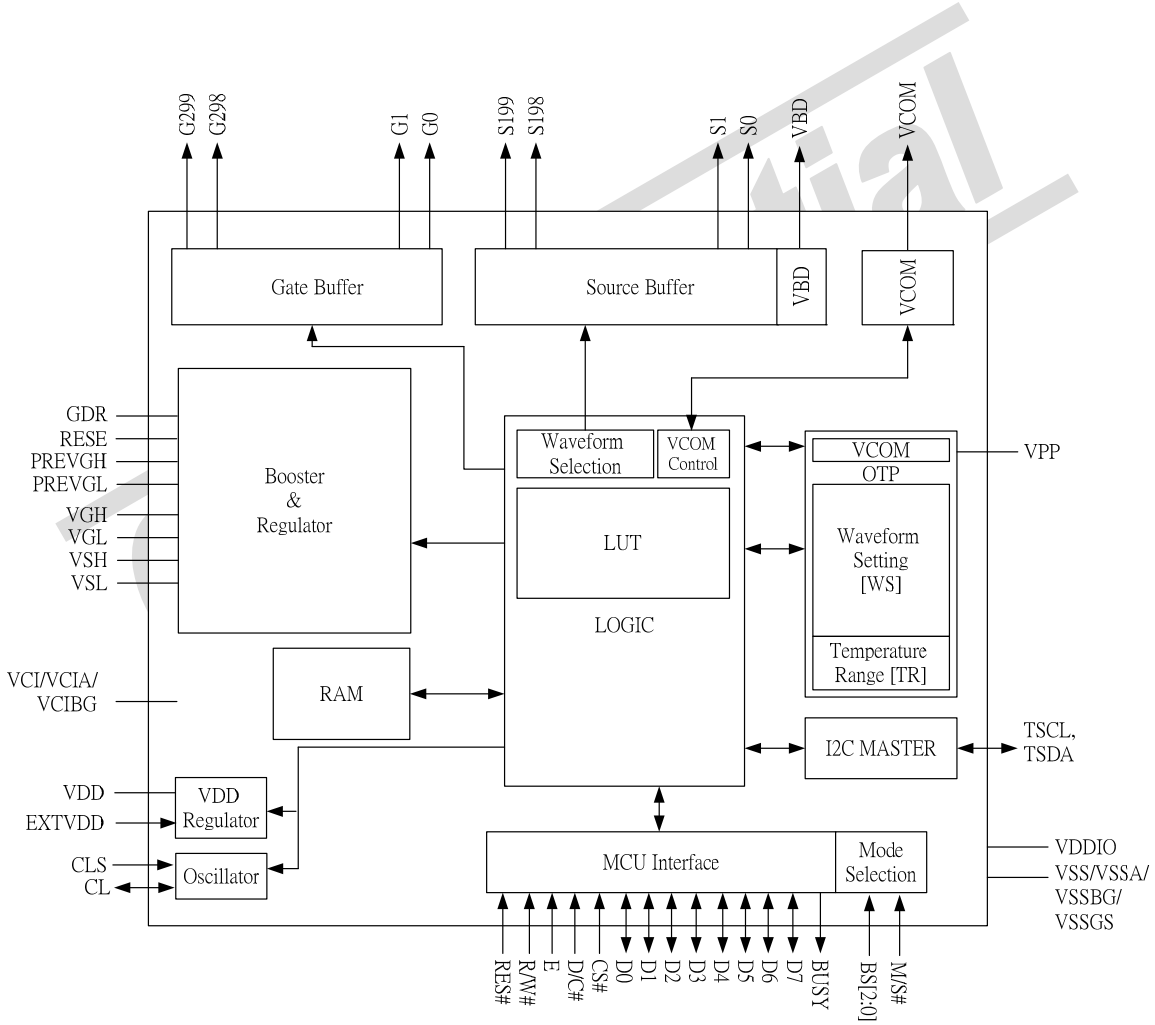
3 ORDERING INFORMATION

Table 3-1 : Ordering Information

Ordering Part Number	Package Form
SSD1607Z	Gold bump die

4 BLOCK DIAGRAM

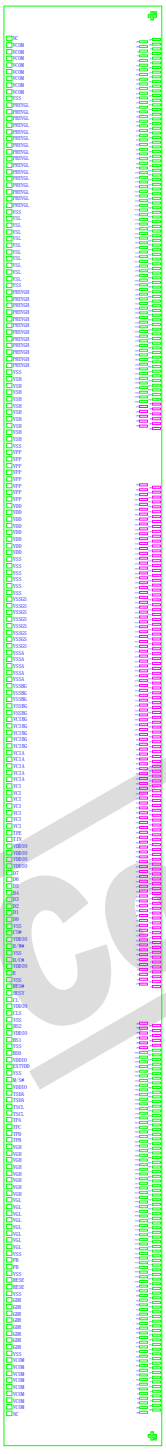
Figure 4-1 : SSD1607 Block Diagram



5 DIE PAD FLOOR PLAN

Figure 5-1 - SSD1607Z Die Floor Plan (Bump face up)

Pin1



Pin747

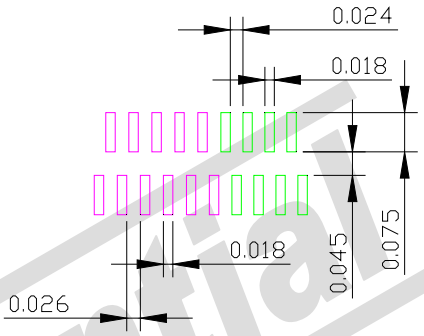
Pin207

Pin208

Die Information:

Die Size: [After sawing]
X = 12.97 +/- 0.1 mm
Y = 1.49 +/- 0.1 mm
Die Height: 300 um +/- 25 um
Bump Height: 12 um
Output pad: 18X75 = 1350 um^2
I/O pad: 40x50 = 2000 um^2

Output Pad Pitch:



Alignment Marks:

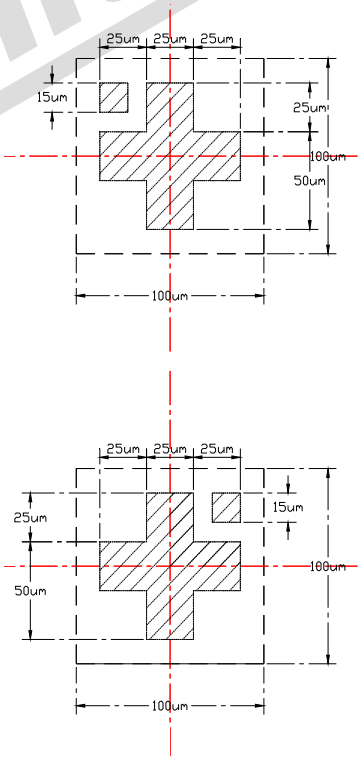


Table 5-1 : SSD1607Z Bump Die Pad Coordinates

Pin #	Pin Name	X	Y
1	NC	-6180	-680
2	VCOM	-6120	-680
3	VCOM	-6060	-680
4	VCOM	-6000	-680
5	VCOM	-5940	-680
6	VCOM	-5880	-680
7	VCOM	-5820	-680
8	VCOM	-5760	-680
9	VCOM	-5700	-680
10	VSS	-5640	-680
11	PREVGL	-5580	-680
12	PREVGL	-5520	-680
13	PREVGL	-5460	-680
14	PREVGL	-5400	-680
15	PREVGL	-5340	-680
16	PREVGL	-5280	-680
17	PREVGL	-5220	-680
18	PREVGL	-5160	-680
19	PREVGL	-5100	-680
20	PREVGL	-5040	-680
21	PREVGL	-4980	-680
22	PREVGL	-4920	-680
23	PREVGL	-4860	-680
24	PREVGL	-4800	-680
25	PREVGL	-4740	-680
26	PREVGL	-4680	-680
27	VSS	-4620	-680
28	VSL	-4560	-680
29	VSL	-4500	-680
30	VSL	-4440	-680
31	VSL	-4380	-680
32	VSL	-4320	-680
33	VSL	-4260	-680
34	VSL	-4200	-680
35	VSL	-4140	-680
36	VSL	-4080	-680
37	VSL	-4020	-680
38	VSS	-3960	-680
39	PREVGH	-3900	-680
40	PREVGH	-3840	-680
41	PREVGH	-3780	-680
42	PREVGH	-3720	-680
43	PREVGH	-3660	-680
44	PREVGH	-3600	-680
45	PREVGH	-3540	-680
46	PREVGH	-3480	-680
47	PREVGH	-3420	-680
48	PREVGH	-3360	-680
49	PREVGH	-3300	-680
50	PREVGH	-3240	-680
51	VSS	-3180	-680
52	VSH	-3120	-680
53	VSH	-3060	-680
54	VSH	-3000	-680
55	VSH	-2940	-680
56	VSH	-2880	-680
57	VSH	-2820	-680
58	VSH	-2760	-680
59	VSH	-2700	-680
60	VSH	-2640	-680
61	VSH	-2580	-680
62	VSS	-2520	-680
63	VPP	-2460	-680
64	VPP	-2400	-680
65	VPP	-2340	-680
66	VPP	-2280	-680
67	VPP	-2220	-680
68	VPP	-2160	-680
69	VPP	-2100	-680
70	VPP	-2040	-680
71	VDD	-1980	-680
72	VDD	-1920	-680
73	VDD	-1860	-680
74	VDD	-1800	-680
75	VDD	-1740	-680
76	VDD	-1680	-680
77	VDD	-1620	-680
78	VDD	-1560	-680
79	VSS	-1500	-680
80	VSS	-1440	-680
81	VSS	-1380	-680
82	VSS	-1320	-680
83	VSS	-1260	-680
84	VSS	-1200	-680
85	VSSGS	-1140	-680
86	VSSGS	-1080	-680
87	VSSGS	-1020	-680
88	VSSGS	-960	-680
89	VSSGS	-900	-680
90	VSSGS	-840	-680
91	VSSGS	-780	-680
92	VSSGS	-720	-680
93	VSSA	-660	-680
94	VSSA	-600	-680
95	VSSA	-540	-680
96	VSSA	-480	-680
97	VSSA	-420	-680
98	VSSBG	-360	-680
99	VSSBG	-300	-680
100	VSSBG	-240	-680
101	VSSBG	-180	-680
102	VSSBG	-120	-680
103	VCIBG	-60	-680
104	VCIBG	0	-680
105	VCIBG	60	-680
106	VCIBG	120	-680
107	VCIBG	180	-680
108	VCIA	240	-680
109	VCIA	300	-680
110	VCIA	360	-680
111	VCIA	420	-680
112	VCIA	480	-680
113	VCI	540	-680
114	VCI	600	-680
115	VCI	660	-680
116	VCI	720	-680
117	VCI	780	-680
118	VCI	840	-680
119	VCI	900	-680
120	TPE	960	-680
121	TIN	1020	-680
122	VDDIO	1080	-680
123	VDDIO	1140	-680
124	VDDIO	1200	-680
125	VDDIO	1260	-680
126	D7	1320	-680
127	D6	1380	-680
128	D5	1440	-680
129	D4	1500	-680
130	D3	1560	-680
131	D2	1620	-680
132	D1	1680	-680
133	D0	1740	-680
134	VSS	1800	-680
135	CS#	1860	-680
136	VDDIO	1920	-680
137	R/W#	1980	-680
138	VSS	2040	-680
139	D/C#	2100	-680
140	VDDIO	2160	-680
141	E	2220	-680
142	VSS	2280	-680
143	RES#	2340	-680
144	BUSY	2400	-680
145	CL	2460	-680
146	VDDIO	2520	-680
147	CLS	2580	-680
148	VSS	2640	-680
149	BS2	2700	-680
150	VDDIO	2760	-680
151	BS1	2820	-680
152	VSS	2880	-680
153	BS0	2940	-680
154	VDDIO	3000	-680
155	EXTVDD	3060	-680
156	VSS	3120	-680
157	M/S#	3180	-680
158	VDDIO	3240	-680
159	TSDA	3300	-680
160	TSDA	3360	-680
161	TSCL	3420	-680
162	TSCL	3480	-680
163	TPA	3540	-680
164	TPC	3600	-680
165	TPD	3660	-680
166	TPB	3720	-680
167	VGH	3780	-680
168	VGH	3840	-680
169	VGH	3900	-680
170	VGH	3960	-680
171	VGH	4020	-680
172	VGH	4080	-680
173	VGH	4140	-680
174	VGH	4200	-680
175	VGL	4260	-680
176	VGL	4320	-680
177	VGL	4380	-680
178	VGL	4440	-680
179	VGL	4500	-680
180	VGL	4560	-680
181	VGL	4620	-680
182	VGL	4680	-680
183	VSS	4740	-680
184	FB	4800	-680
185	FB	4860	-680
186	VSS	4920	-680
187	RESE	4980	-680
188	RESE	5040	-680
189	VSS	5100	-680
190	GDR	5160	-680
191	GDR	5220	-680
192	GDR	5280	-680
193	GDR	5340	-680
194	GDR	5400	-680
195	GDR	5460	-680
196	GDR	5520	-680
197	GDR	5580	-680
198	VSS	5640	-680
199	VCOM	5700	-680
200	VCOM	5760	-680
201	VCOM	5820	-680
202	VCOM	5880	-680
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204	VCOM	6000	-680
205	VCOM	6060	-680
206	VCOM	6120	-680
207	NC	6180	-680
208	NC	6170	561.5
209	NC	6149	681.5
210	NC	6128	561.5
211	NC	6107	681.5
212	NC	6086	561.5
213	NC	6065	681.5
214	G0	6044	561.5
215	G2	6023	681.5
216	G4	6002	561.5
217	G6	5981	681.5
218	G8	5960	561.5
219	G10	5939	681.5
220	G12	5918	561.5
221	G14	5897	681.5
222	G16	5876	561.5
223	G18	5855	681.5
224	G20	5834	561.5
225	G22	5813	681.5
226	G24	5792	561.5
227	G26	5771	681.5
228	G28	5750	561.5
229	G30	5729	681.5
230	G32	5708	561.5
231	G34	5687	681.5
232	G36	5666	561.5
233	G38	5645	681.5
234	G40	5624	561.5
235	G42	5603	681.5
236	G44	5582	561.5
237	G46	5561	681.5
238	G48	5540	561.5
239	G50	5519	681.5
240	G52	5498	561.5
241	G54	5477	681.5
242	G56	5456	561.5
243	G58	5435	681.5
244	G60	5414	561.5
245	G62	5393	681.5
246	G64	5372	561.5
247	G66	5351	681.5
248	G68	5330	561.5
249	G70	5309	681.5
250	G72	5288	561.5
251	G74	5267	681.5
252	G76	5246	561.5
253	G78	5225	681.5
254	G80	5204	561.5
255	G82	5183	681.5
256	G84	5162	561.5
257	G86	5141	681.5
258	G88	5120	561.5
259	G90	5099	681.5
260	G92	5078	561.5
261	G94	5057	681.5
262	G96	5036	561.5
263	G98	5015	681.5
264	G100	4994	561.5
265	G102	4973	681.5
266	G104	4952	561.5
267	G106	4931	681.5
268	G108	4910	561.5
269	G110	4889	681.5
270	G112	4868	561.5
271	G114	4847	681.5
272	G116	4826	561.5
273	G118	4805	681.5
274	G120	4784	561.5
275	G122	4763	681.5
276	G124	4742	561.5
277	G126	4721	681.5
278	G128	4700	561.5
279	G130	4679	681.5
280	G132	4658	561.5
281	G134	4637	681.5
282	G136	4616	561.5
283	G138	4595	681.5
284	G140	4574	561.5
285	G142	4553	681.5
286	G144	4532	561.5
287	G146	4511	681.5
288	G148	4490	561.5
289	G150	4469	681.5
290	G152	4448	561.5
291	G154	4427	681.5
292	G156	4406	561.5
293	G158	4385	681.5
294	G160	4364	561.5
295	G162	4343	681.5
296	G164	4322	561.5
297	G166	4301	681.5
298	G168	4280	561.5
299	G170	4259	681.5
300	G172	4238	561.5
301	G174	4217	681.5
302	G176	4196	561.5
303	G178	4175	681.5
304	G180	4154	561.5
305	G182	4133	681.5
306	G184	4112	561.5
307	G186	4091	681.5
308	G188	4070	561.5
309	G190	4049	681.5
310	G192	4028	561.5
311	G194	4007	681.5
312	G196	3986	561.5
313	G198	3965	681.5
314	G200	3944	561.5
315	G202	3923	681.5
316	G204	3902	561.5
317	G206	3881	681.5
318	G208	3860	561.5
319	G210	3839	681.5
320	G212	3818	561.5

Pin #	Pin Name	X	Y
321	G214	3797	681.5
322	G216	3776	561.5
323	G218	3755	681.5
324	G220	3734	561.5
325	G222	3713	681.5
326	G224	3692	561.5
327	G226	3671	681.5
328	G228	3650	561.5
329	G230	3629	681.5
330	G232	3608	561.5
331	G234	3587	681.5
332	G236	3566	561.5
333	G238	3545	681.5
334	G240	3524	561.5
335	G242	3503	681.5
336	G244	3482	561.5
337	G246	3461	681.5
338	G248	3440	561.5
339	G250	3419	681.5
340	G252	3398	561.5
341	G254	3377	681.5
342	G256	3356	561.5
343	G258	3335	681.5
344	G260	3314	561.5
345	G262	3293	681.5
346	G264	3272	561.5
347	G266	3251	681.5
348	G268	3230	561.5
349	G270	3209	681.5
350	G272	3188	561.5
351	G274	3167	681.5
352	G276	3146	561.5
353	G278	3125	681.5
354	G280	3104	561.5
355	G282	3083	681.5
356	G284	3062	561.5
357	G286	3041	681.5
358	G288	3020	561.5
359	G290	2999	681.5
360	G292	2978	561.5
361	G294	2957	681.5
362	G296	2936	561.5
363	G298	2915	681.5
364	NC	2893	561.5
365	NC	2871	681.5
366	NC	2849	561.5
367	NC	2827	681.5
368	NC	2805	561.5
369	NC	2783	681.5
370	NC	2761	561.5
371	NC	2739	681.5
372	NC	2717	561.5
373	NC	2695	681.5
374	NC	2673	561.5
375	NC	2343	681.5
376	NC	2321	561.5
377	VBD	2299	681.5
378	S0	2277	561.5
379	S1	2255	681.5
380	S2	2233	561.5
381	S3	2211	681.5
382	S4	2189	561.5
383	S5	2167	681.5
384	S6	2145	561.5
385	S7	2123	681.5
386	S8	2101	561.5
387	S9	2079	681.5
388	S10	2057	561.5
389	S11	2035	681.5
390	S12	2013	561.5
391	S13	1991	681.5
392	S14	1969	561.5
393	S15	1947	681.5
394	S16	1925	561.5
395	S17	1903	681.5
396	S18	1881	561.5
397	S19	1859	681.5
398	S20	1837	561.5
399	S21	1815	681.5
400	S22	1793	561.5

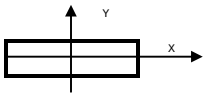
Pin #	Pin Name	X	Y
401	S23	1771	681.5
402	S24	1749	561.5
403	S25	1727	681.5
404	S26	1705	561.5
405	S27	1683	681.5
406	S28	1661	561.5
407	S29	1639	681.5
408	S30	1617	561.5
409	S31	1595	681.5
410	S32	1573	561.5
411	S33	1551	681.5
412	S34	1529	561.5
413	S35	1507	681.5
414	S36	1485	561.5
415	S37	1463	681.5
416	S38	1441	561.5
417	S39	1419	681.5
418	S40	1397	561.5
419	S41	1375	681.5
420	S42	1353	561.5
421	S43	1331	681.5
422	S44	1309	561.5
423	S45	1287	681.5
424	S46	1265	561.5
425	S47	1243	681.5
426	S48	1221	561.5
427	S49	1199	681.5
428	S50	1177	561.5
429	S51	1155	681.5
430	S52	1133	561.5
431	S53	1111	681.5
432	S54	1089	561.5
433	S55	1067	681.5
434	S56	1045	561.5
435	S57	1023	681.5
436	S58	1001	561.5
437	S59	979	681.5
438	S60	957	561.5
439	S61	935	681.5
440	S62	913	561.5
441	S63	891	681.5
442	S64	869	561.5
443	S65	847	681.5
444	S66	825	561.5
445	S67	803	681.5
446	S68	781	561.5
447	S69	759	681.5
448	S70	737	561.5
449	S71	715	681.5
450	S72	693	561.5
451	S73	671	681.5
452	S74	649	561.5
453	S75	627	681.5
454	S76	605	561.5
455	S77	583	681.5
456	S78	561	561.5
457	S79	539	681.5
458	S80	517	561.5
459	S81	495	681.5
460	S82	473	561.5
461	S83	451	681.5
462	S84	429	561.5
463	S85	407	681.5
464	S86	385	561.5
465	S87	363	681.5
466	S88	341	561.5
467	S89	319	681.5
468	S90	297	561.5
469	S91	275	681.5
470	S92	253	561.5
471	S93	231	681.5
472	S94	209	561.5
473	S95	187	681.5
474	S96	165	561.5
475	S97	143	681.5
476	S98	121	561.5
477	S99	99	681.5
478	S100	77	561.5
479	S101	55	681.5
480	S102	33	561.5

Pin #	Pin Name	X	Y
481	S103	11	681.5
482	S104	-11	561.5
483	S105	-33	681.5
484	S106	-55	561.5
485	S107	-77	681.5
486	S108	-99	561.5
487	S109	-121	681.5
488	S110	-143	561.5
489	S111	-165	681.5
490	S112	-187	561.5
491	S113	-209	681.5
492	S114	-231	561.5
493	S115	-253	681.5
494	S116	-275	561.5
495	S117	-297	681.5
496	S118	-319	561.5
497	S119	-341	681.5
498	S120	-363	561.5
499	S121	-385	681.5
500	S122	-407	561.5
501	S123	-429	681.5
502	S124	-451	561.5
503	S125	-473	681.5
504	S126	-495	561.5
505	S127	-517	681.5
506	S128	-539	561.5
507	S129	-561	681.5
508	S130	-583	561.5
509	S131	-605	681.5
510	S132	-627	561.5
511	S133	-649	681.5
512	S134	-671	561.5
513	S135	-693	681.5
514	S136	-715	561.5
515	S137	-737	681.5
516	S138	-759	561.5
517	S139	-781	681.5
518	S140	-803	561.5
519	S141	-825	681.5
520	S142	-847	561.5
521	S143	-869	681.5
522	S144	-891	561.5
523	S145	-913	681.5
524	S146	-935	561.5
525	S147	-957	681.5
526	S148	-979	561.5
527	S149	-1001	681.5
528	S150	-1023	561.5
529	S151	-1045	681.5
530	S152	-1067	561.5
531	S153	-1089	681.5
532	S154	-1111	561.5
533	S155	-1133	681.5
534	S156	-1155	561.5
535	S157	-1177	681.5
536	S158	-1199	561.5
537	S159	-1221	681.5
538	S160	-1243	561.5
539	S161	-1265	681.5
540	S162	-1287	561.5
541	S163	-1309	681.5
542	S164	-1331	561.5
543	S165	-1353	681.5
544	S166	-1375	561.5
545	S167	-1397	681.5
546	S168	-1419	561.5
547	S169	-1441	681.5
548	S170	-1463	561.5
549	S171	-1485	681.5
550	S172	-1507	561.5
551	S173	-1529	681.5
552	S174	-1551	561.5
553	S175	-1573	681.5
554	S176	-1595	561.5
555	S177	-1617	681.5
556	S178	-1639	561.5
557	S179	-1661	681.5
558	S180	-1683	561.5
559	S181	-1705	681.5
560	S182	-1727	561.5

Pin #	Pin Name	X	Y
561	S183	-1749	681.5
562	S184	-1771	561.5
563	S185	-1793	681.5
564	S186	-1815	561.5
565	S187	-1837	681.5
566	S188	-1859	561.5
567	S189	-1881	681.5
568	S190	-1903	561.5
569	S191	-1925	681.5
570	S192	-1947	561.5
571	S193	-1969	681.5
572	S194	-1991	561.5
573	S195	-2013	681.5
574	S196	-2035	561.5
575	S197	-2057	681.5
576	S198	-2079	561.5
577	S199	-2101	681.5
578	VBD	-2123	561.5
579	NC	-2145	681.5
580	NC	-2167	561.5
581	NC	-2673	681.5
582	NC	-2695	561.5
583	NC	-2717	681.5
584	NC	-2739	561.5
585	NC	-2761	681.5
586	NC	-2783	561.5
587	NC	-2805	681.5
588	NC	-2827	561.5
589	NC	-2849	681.5
590	NC	-2871	561.5
591	NC	-2893	681.5
592	G299	-2915	561.5
593	G297	-2936	681.5
594	G295	-2957	561.5
595	G293	-2978	681.5
596	G291	-2999	561.5
597	G289	-3020	681.5
598	G287	-3041	561.5
599	G285	-3062	681.5
600	G283	-3083	561.5
601	G281	-3104	681.5
602	G279	-3125	561.5
603	G277	-3146	681.5
604	G275	-3167	561.5
605	G273	-3188	681.5
606	G271	-3209	561.5
607	G269	-3230	681.5
608	G267	-3251	561.5
609	G265	-3272	681.5
610	G263	-3293	561.5
611	G261	-3314	681.5
612	G259	-3335	561.5
613	G257	-3356	681.5
614	G255	-3377	561.5
615	G253	-3398	681.5
616	G251	-3419	561.5
617	G249	-3440	681.5
618	G247	-3461	561.5
619	G245	-3482	681.5
620	G243	-3503	561.5
621	G241	-3524	681.5
622	G239	-3545	561.5
623	G237	-3566	681.5
624	G235	-3587	561.5
625	G233	-3608	681.5
626	G231	-3629	561.5
627	G229	-3650	681.5
628	G227	-3671	561.5
629	G225	-3692	681.5
630	G223	-3713	561.5
631	G221	-3734	681.5
632	G219	-3755	561.5
633	G217	-3776	681.5
634	G215	-3797	561.5
635	G213	-3818	681.5
636	G211	-3839	561.5
637	G209	-3860	681.5
638	G207	-3881	561.5
639	G205	-3902	681.5
640	G203	-3923	561.5

Pin #	Pin Name	X	Y
641	G201	-3944	681.5
642	G199	-3965	561.5
643	G197	-3986	681.5
644	G195	-4007	561.5
645	G193	-4028	681.5
646	G191	-4049	561.5
647	G189	-4070	681.5
648	G187	-4091	561.5
649	G185	-4112	681.5
650	G183	-4133	561.5
651	G181	-4154	681.5
652	G179	-4175	561.5
653	G177	-4196	681.5
654	G175	-4217	561.5
655	G173	-4238	681.5
656	G171	-4259	561.5
657	G169	-4280	681.5
658	G167	-4301	561.5
659	G165	-4322	681.5
660	G163	-4343	561.5
661	G161	-4364	681.5
662	G159	-4385	561.5
663	G157	-4406	681.5
664	G155	-4427	561.5
665	G153	-4448	681.5
666	G151	-4469	561.5
667	G149	-4490	681.5
668	G147	-4511	561.5
669	G145	-4532	681.5
670	G143	-4553	561.5
671	G141	-4574	681.5
672	G139	-4595	561.5
673	G137	-4616	681.5
674	G135	-4637	561.5
675	G133	-4658	681.5
676	G131	-4679	561.5
677	G129	-4700	681.5
678	G127	-4721	561.5
679	G125	-4742	681.5
680	G123	-4763	561.5
681	G121	-4784	681.5
682	G119	-4805	561.5
683	G117	-4826	681.5
684	G115	-4847	561.5
685	G113	-4868	681.5
686	G111	-4889	561.5
687	G109	-4910	681.5
688	G107	-4931	561.5
689	G105	-4952	681.5
690	G103	-4973	561.5
691	G101	-4994	681.5
692	G99	-5015	561.5
693	G97	-5036	681.5
694	G95	-5057	561.5
695	G93	-5078	681.5
696	G91	-5099	561.5
697	G89	-5120	681.5
698	G87	-5141	561.5
699	G85	-5162	681.5
700	G83	-5183	561.5
701	G81	-5204	681.5
702	G79	-5225	561.5
703	G77	-5246	681.5
704	G75	-5267	561.5
705	G73	-5288	681.5
706	G71	-5309	561.5
707	G69	-5330	681.5
708	G67	-5351	561.5
709	G65	-5372	681.5
710	G63	-5393	561.5
711	G61	-5414	681.5
712	G59	-5435	561.5
713	G57	-5456	681.5
714	G55	-5477	561.5
715	G53	-5498	681.5
716	G51	-5519	561.5
717	G49	-5540	681.5
718	G47	-5561	561.5
719	G45	-5582	681.5
720	G43	-5603	561.5

Pin #	Pin Name	X	Y
721	G41	-5624	681.5
722	G39	-5645	561.5
723	G37	-5666	681.5
724	G35	-5687	561.5
725	G33	-5708	681.5
726	G31	-5729	561.5
727	G29	-5750	681.5
728	G27	-5771	561.5
729	G25	-5792	681.5
730	G23	-5813	561.5
731	G21	-5834	681.5
732	G19	-5855	561.5
733	G17	-5876	681.5
734	G15	-5897	561.5
735	G13	-5918	681.5
736	G11	-5939	561.5
737	G9	-5960	681.5
738	G7	-5981	561.5
739	G5	-6002	681.5
740	G3	-6023	561.5
741	G1	-6044	681.5
742	NC	-6065	561.5
743	NC	-6086	681.5
744	NC	-6107	561.5
745	NC	-6128	681.5
746	NC	-6149	561.5
747	NC	-6170	681.5



Pad 1,2,3,…>> 207
Gold Bumps face up

Unit in um			
Die height		300	
Bump height		12	
Bump size		X	Y
Pad	1-207	40	50
Pad	208-747	18	75
Alignment mark		X	Y
	'+ shape	-6382	642
	+' shape	6382	642

6 PIN DESCRIPTION

Key: I = Input, O =Output, IO = Bi-directional (input/output), P = Power pin, C = Capacitor Pin
NC = Not Connected, Pull L =connect to V_{SS}, Pull H = connect to V_{DDIO}

Pin name	Type	Connect to	Function	Description	When not in use
Input power					
VCI	P	Power Supply	Power Supply	Power Supply for the chip	-
VCIA	P	Power Supply	Power Supply	Power input for the chip, Connected with VCI	-
VCIBG	P	Power Supply	Power Supply	Power input for the chip (Reference), Connected with VCI	-
VDDIO	P	Power Supply	Power for interface logic pins	Power Supply for the Interface It should be connected with VCI	-
VDD	P	Capacitor	Regulator output	Core logic power pin VDD can be regulated internally from VCI. - For the single chip application, a capacitor should be connected between VDD and VSS under all circumstances. - For the cascade mode application, a capacitor should be connected between VDD and VSS in the master chip under all circumstances. For the slave chip, the capacitor is not necessary as VDD will be supplied from the cascade master chip externally.	-
EXTVDD	I	VDDIO/VSS	Regulator bypass	This pin is VDD regulator bypass pin. - For the single chip application, EXTVDD should be connected to VSS. - For the cascade mode application, EXTVDD of the master chip should be connected to VSS while EXTVDD of the slave chip should be connected to VDDIO.	-
VSS	P	VSS	GND	Ground (Digital)	-
VSSA	P	VSS	GND	Ground (Analog) It should be connected with VSS.	-
VSSBG	P	VSS	GND	Ground (Reference) Connected with VSS	-
VSSGS	P	VSS	GND	Ground (Output) Connected with VSS	-
VPP	P	Power Supply	OTP power	Power Supply for OTP Programming	Open
Digital I/O					
D [7:0]	I/O	MPU	Data Bus	These pins are bi-directional data bus connecting to the MCU data bus. SPI mode: D0: SCLK D1: SDIN	D[2] : OPEN D[7:3]: VDDIO or VSS
CS#	I	MPU	Logic Control	This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW in parallel interface.	VDDIO or VSS

Pin name	Type	Connect to	Function	Description	When not in use
R/W# (WR#)	I	MPU		This pin is read / write control input pin connecting to the MCU interface. When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin R/W (WR#) can be connected to either VDDIO or VSS.	VDDIO or VSS
D/C#	I	MPU		This pin is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data at D [7:0] will be interpreted as data. When the pin is pulled LOW, the data at D [7:0] will be interpreted as command.	VDDIO or VSS
E (RD#)	I	MPU		This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin E (RD#) should be connected to either VDDIO or VSS	VDDIO or VSS
RES#	I	MPU	System Reset	This pin is reset signal input. Active Low.	-
BUSY	O	MPU	Device Busy Signal	This pin is Busy state output pin When Busy is High, the operation of the chip should not be interrupted, command should not be sent. For example., The chip would put Busy pin High when - Outputting display waveform; or - Programming with OTP - Communicating with digital temperature sensor In the cascade mode, the BUSY pin of the slave chip should be left open.	Open
CLS	I	VDDIO/VSS	Clock Mode Selection	This pin is internal clock enable pin. - For the single chip application, the CLS pin should be connected to VDDIO. - For the cascade mode application, the CLS pin of the master chip should be connected to VDDIO. The CLS pin of the slave chip should be connected to VSS to disable the internal clock as its CL pin should be connected to the CL pin of the master chip.	-
M/S#	I	VDDIO/VSS	Cascade Mode Selection	This pin is Master and Slave selection pin. - For the single chip application, the M/S# pin should be connected to VDDIO. - In the cascade mode: For Master Chip, the M/S# pin should be connected to VDDIO. For Slave Chip, the M/S# pin should be connected to VSS. The oscillator and the booster & regulator circuits of the slave chip will be disabled. The corresponding pins including CL, VDD, VDDIO, PREVGH, PREVGL, VSH, VSL, VGH, VGL and VCOM must be connected to the master chip.	

<table>
<tr><th>Pin name</th><th>Type</th><th>Connect to</th><th>Function</th><th>Description</th><th>When not in use</th></tr>
<tr><td>CL</td><td>I/O</td><td>NC</td><td>Clock signal</td><td>This is the clock signal pin.
When CLS is connected to VDDIO, the internal clock is enable. The clock signal will be detected at CL. Leave the CL pin open when internal clock is enable and used.
When CLS is connected to VSS, the internal clock is disable. An external clock is fed in the CL pin.

In the cascade mode, the CL pin of the slave chip should be connected to the CL pin of the master chip.</td><td></td></tr>
<tr><td>BS [2:0]</td><td>I</td><td>VDDIO/VSS</td><td>MCU Interface Mode Selection</td><td>These pins are for selecting different bus interface.
BS2 should be connected to VSS.
Table 6-1 : MCU interface selection
<table>
<tr><td>BS1</td><td>BS0</td><td>MPU Interface</td></tr>
<tr><td>L</td><td>L</td><td>4-lines serial peripheral interface (SPI)</td></tr>
<tr><td>L</td><td>H</td><td>8-bit 8080 parallel interface</td></tr>
<tr><td>H</td><td>L</td><td>3-lines serial peripheral interface (SPI) – 9 bits SPI</td></tr>
<tr><td>H</td><td>H</td><td>8-bit 6800 parallel interface</td></tr>
</table></td><td>-</td></tr>
<tr><td>TSDA</td><td>I/O</td><td>Temperature sensor SDA</td><td>Interface to Digital Temperature Sensor</td><td>This pin is I^2C Interface to digital temperature sensor Data pin
External pull up resistor is required when connecting to I^2C slave</td><td>Open</td></tr>
<tr><td>TSCL</td><td>O</td><td>Temperature sensor SCL</td><td>Interface to Digital Temperature Sensor</td><td>This pin is I^2C Interface to digital temperature sensor Clock pin
External pull up resistor is required when connecting to I^2C slave</td><td>Open</td></tr>
<tr><td colspan="6">Analog Pin</td></tr>
<tr><td>GDR</td><td>O</td><td>POWER MOSFET Driver Control</td><td>PREVGH & PREVGL Generation</td><td>This pin is N-Channel MOSFET Gate Drive Control.

In the cascade mode, the GDR pin of the slave chip should be left open.</td><td>-</td></tr>
<tr><td>RESE</td><td>I</td><td>Booster Control Input</td><td></td><td>This pin is the Current Sense Input for the Control Loop

In the cascade mode, the RESE pin of the slave chip should be left open.</td><td>-</td></tr>
<tr><td>FB</td><td>I</td><td>NC</td><td></td><td>Keep open.</td><td>Open</td></tr>
<tr><td>PREVGH</td><td>C</td><td>Stabilizing capacitor</td><td></td><td>This pin is the Power Supply pin for VGH and VSH.
A stabilizing capacitor should be connected between PREVGH and VSS.</td><td>-</td></tr>
<tr><td>PREVGL</td><td>C</td><td>Stabilizing capacitor</td><td></td><td>This pin is the Power Supply pin for VCOM, VGL and VSL.
A stabilizing capacitor should be connected between PREVGL and VSS.</td><td>-</td></tr>
<tr><td colspan="6"></td></tr>
<tr><td>VGH</td><td>C</td><td>Stabilizing capacitor</td><td>VGH, VGL Generation</td><td>Positive Gate driving voltage.
A stabilizing capacitor should be connected between VGH and VSS.</td><td>-</td></tr>
<tr><td>VGL</td><td>C</td><td>Stabilizing capacitor</td><td>VGL Generation</td><td>This pin is Negative Gate driving voltage.
A stabilizing capacitor should be connected between VGL and VSS.</td><td>-</td></tr>
</table>

Pin name	Type	Connect to	Function	Description	When not in use
VSH	C	Stabilizing capacitor	VSH, VSL Generation	This pin is Positive Source driving voltage. A stabilizing capacitor should be connected between VSH and VSS.	-
VSL	C	Stabilizing capacitor		This pin is Negative Source driving voltage. A stabilizing capacitor should be connected between VSL and VSS.	-
VCOM	C	Panel/ Stabilizing capacitor	VCOM	This pin is VCOM driving voltage A stabilizing capacitor should be connected between VCOM and VSS.	-
Panel Driving					
S [199:0]	O	Panel	Source driving signal	Source output pin	Open
G [299:0]	O	Panel	Gate driving signal	Gate output pin	Open
VBD	O	Panel	Border driving signal	Border output pin	Open
Others					
NC	NC	NC	Not Connected	Keep open. Don't connect with other NC pins	Open
TPA	NC	NC	Reserved for Testing	Keep open. Don't connect to NC pin or other test pins including TPA, TPB, TPC, TPD and TPE.	Open
TPB	NC	NC	Reserved for Testing	Keep open. Don't connect to NC pin or other test pins including TPA, TPB, TPC, TPD and TPE.	Open
TPC	NC	NC	Reserved for Testing	Keep open. Don't connect to NC pin or other test pins including TPA, TPB, TPC, TPD and TPE.	Open
TPD	NC	NC	Reserved for Testing	Keep open. Don't connect to NC pin or other test pins including TPA, TPB, TPC, TPD and TPE.	Open
TIN	I	NC	Reserved for Testing	Connect to TPE pin.	
TPE	O	NC	Reserved for Testing	Connect to TIN pin.	

7 FUNCTIONAL BLOCK DESCRIPTION

The device can drive an active matrix TFT EPD panel. It composes of 200 source outputs, 300 gate outputs, 1 VBD and 1 VCOM. It contains flexible built-in waveforms to drive the EPD panel.

7.1 MCU Interface

7.1.1 MCU Interface selection

The SSD1607 can support 6800-series/8080-series parallel interface and 3-wire/4-wire serial peripheral Interface. In the SSD1607, the MCU interface is pin selectable by BS0 and BS1 pins shown in Table 7-1

Table 7-1 : MCU interface selection by BS0 and BS1

BS1	BS0	MPU Interface
L	L	4-lines serial peripheral interface (SPI)
L	H	8-bit 8080 parallel interface
H	L	3-lines serial peripheral interface (SPI) – 9 bits SPI
H	H	8-bit 6800 parallel interface

The MCU interface consists of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 7-2.

Table 7-2 : MCU interface assignment under different bus interface mode

Pin Name	Data/Command Interface								Control Signal				
Bus Interface	D7	D6	D5	D4	D3	D2	D1	D0	E (RD#)	R/W# (WR#)	CS#	D/C#	RES#
SPI4	L					NC	SDin	SCLK	L	L	CS#	D/C#	RES#
8-bit 8080	D [7:0]								RD#	WR#	CS#	D/C#	RES#
SPI3	L					NC	SDin	SCLK	L	L	CS#	L	RES#
8-bit 6800	D [7:0]								E	R/W#	CS#	D/C#	RES#

Note
(1) L is connected to V_{SS}
(2) H is connected to V_{DDIO}

7.1.2 MCU 6800-series Parallel Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.
A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

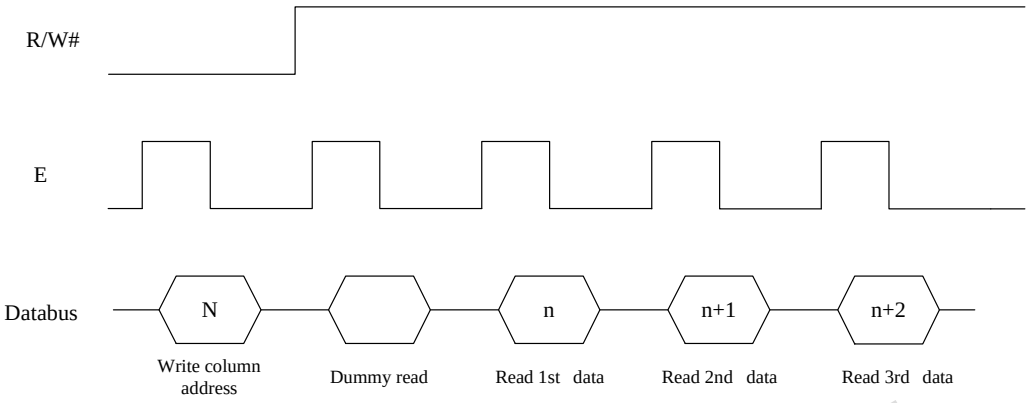
Table 7-3 : Control pins of 6800 interface

Function	E	R/W#	CS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note: ↓ stands for falling edge of signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 7-1.

Figure 7-1 : Data read back procedure - insertion of dummy read



7.1.3 MCU 8080-series Parallel Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 7-2 : Example of Write procedure in 8080 parallel interface mode

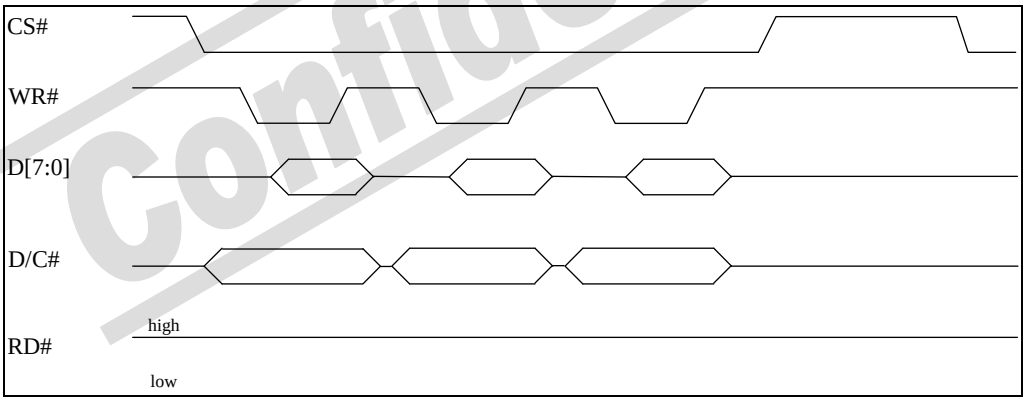


Figure 7-3 : Example of Read procedure in 8080 parallel interface mode

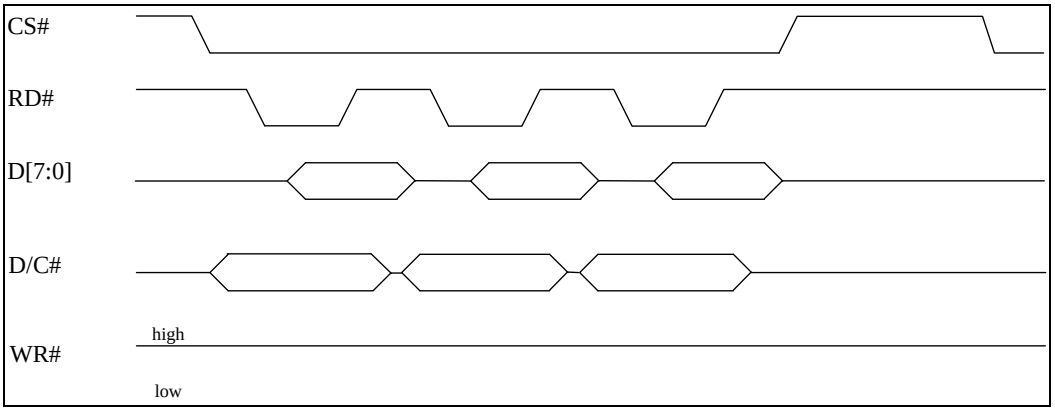


Table 7-4 : Control pins of 8080 interface (Form 1)

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
(1) ↑ stands for rising edge of signal
(2) Refer to Figure 13-2 for Form 1 8080-Series MPU Parallel Interface Timing Characteristics

Alternatively, RD# and WR# can be keep stable while CS# serves as the data/command latch signal.

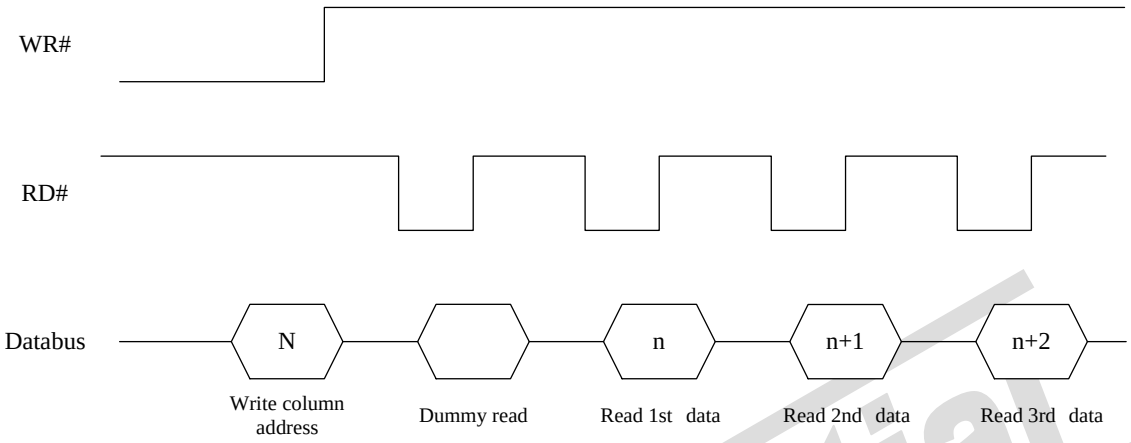
Table 7-5 : Control pins of 8080 interface (Form 2)

Function	RD#	WR#	CS#	D/C#
Write command	H	L	↑	L
Read status	L	H	↑	L
Write data	H	L	↑	H
Read data	L	H	↑	H

Note
(1) ↑ stands for rising edge of signal
(2) Refer to Figure 13-3 for Form 2 8080-Series MPU Parallel Interface Timing Characteristics

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 7-4.

Figure 7-4 : Display data read back procedure - insertion of dummy read



7.1.4 MCU Serial Peripheral Interface (4-wire SPI)

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, E and R/W# can be connected to an external ground.

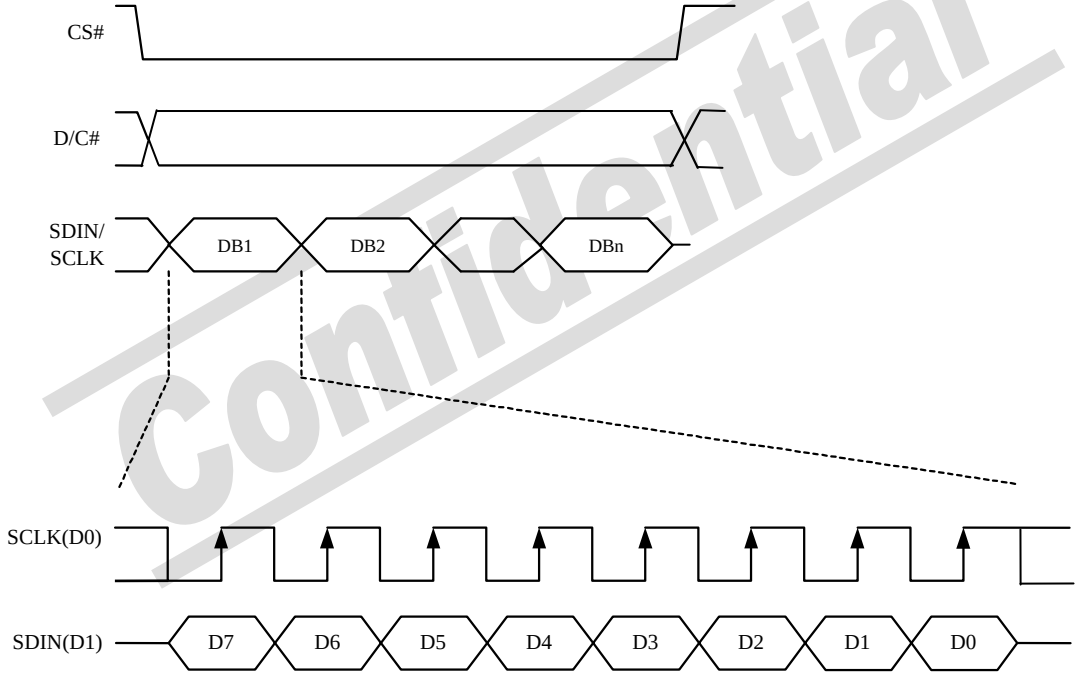
Table 7-6 : Control pins of 4-wire Serial Peripheral interface

Function	E(RD#)	R/W#(WR#)	CS#	D/C#	SCLK
Write command	Tie LOW	Tie LOW	L	L	↑
Write data	Tie LOW	Tie LOW	L	H	↑

Note: ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register in the order of D7, D6, ... D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.

Figure 7-5 : Write procedure in 4-wire Serial Peripheral Interface mode



7.1.5 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.
In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, R/W# (WR#)#, E and D/C# can be connected to an external ground.

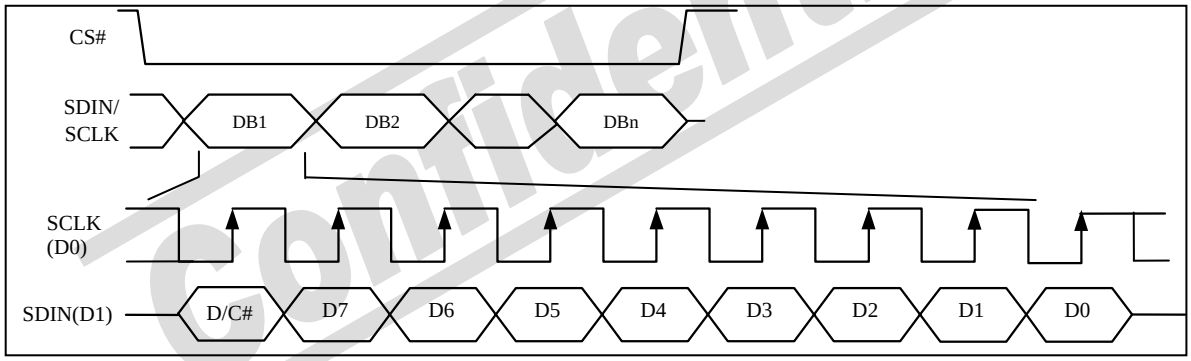
The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

Table 7-7 : Control pins of 3-wire Serial Peripheral interface

Function	E(RD#)	R/W#(WR#)	CS#	D/C#	SCLK
Write command	Tie LOW	Tie LOW	L	Tie LOW	↑
Write data	Tie LOW	Tie LOW	L	Tie LOW	↑

Note: ↑ stands for rising edge of signal

Figure 7-6 : Write procedure in 3-wire Serial Peripheral Interface mode



7.2 RAM

The On chip display RAM is holding the image data. 1 set of RAM is built for historical data and the other set is built for the current image data. The size of each RAM is 200x300 bits.

Table 7-8 shows the RAM map under the following condition:

- Command “Data Entry Mode” R11h is set to:

Address Counter update in X direction	AM=0
X: Increment Y: Increment	ID[1:0] =11

- Command “Driver Output Control” R01h is set to

300 Mux	MUX = 12BFh
Select G0 as 1st gate	GD = 0
Left and Right gate Interlaced	SM = 0
Scan From G0 to G299	TB = 0

- Command “Gate Start Position” R0Fh is set to:

Set the Start Position of Gate = G0	SCN=0

- Data byte sequence: DB0, DB1, DB2 … DB7499

Table 7-8 : RAM address map

		S0	S1	S2	S3	S4	S5	S6	S7	…	…	S192	S193	S194	S195	S196	S197	S198	S199
		00h								…		18h							
G0	00h	DB0 [7]	DB0 [6]	DB0 [5]	DB0 [4]	DB0 [3]	DB0 [2]	DB0 [1]	DB0 [0]	…	…	DB24 [7]	DB24 [6]	DB24 [5]	DB24 [4]	DB24 [3]	DB24 [2]	DB24 [1]	DB24 [0]
G1	01h	DB25 [7]	DB25 [6]	DB25 [5]	DB25 [4]	DB25 [3]	DB25 [2]	DB25 [1]	DB25 [0]	…	…	DB49 [7]	DB49 [6]	DB49 [5]	DB49 [4]	DB49 [3]	DB49 [2]	DB49 [1]	DB49 [0]
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…
G298	12Ah	DB7450 [7]	DB7450 [6]	DB7450 [5]	DB7450 [4]	DB7450 [3]	DB7450 [2]	DB7450 [1]	DB7450 [0]	…	…	DB7474 [7]	DB7474 [6]	DB7474 [5]	DB7474 [4]	DB7474 [3]	DB7474 [2]	DB7474 [1]	DB7474 [0]
G299	12Bh	DB7475 [7]	DB7475 [6]	DB7475 [5]	DB7475 [4]	DB7475 [3]	DB7475 [2]	DB7475 [1]	DB7475 [0]	…	…	DB7499 [7]	DB7999 [6]	DB7999 [5]	DB7999 [4]	DB7999 [3]	DB7999 [2]	DB7999 [1]	DB7999 [0]
GATE	Y-ADDR																		

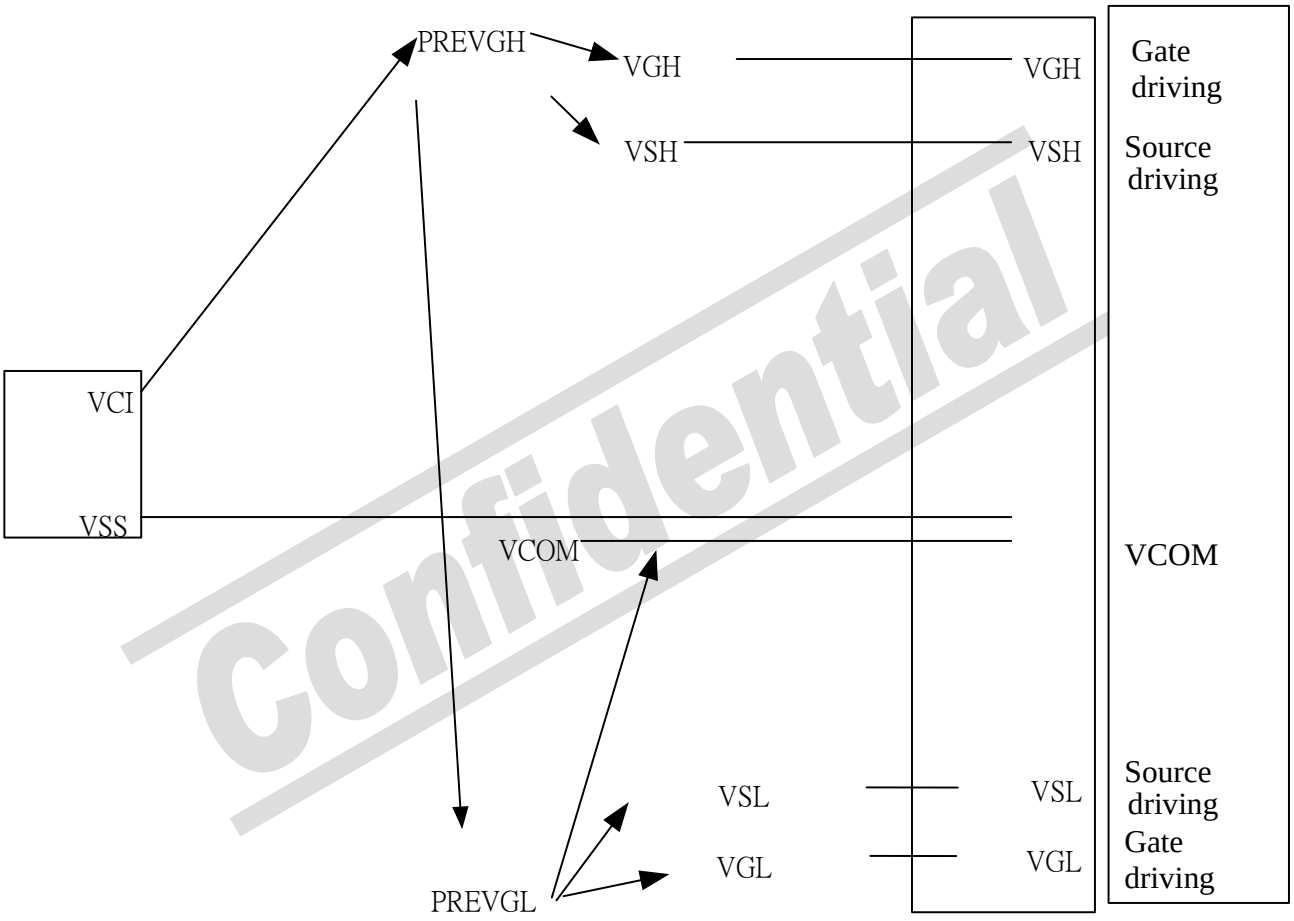
7.3 Oscillator

The on-chip oscillator is included for the use on waveform timing and Booster operations. In order to enable the internal oscillator, the CLS pin must be connected to VDDIO.

7.4 Booster & Regulator

A voltage generation system is included in the SSD1607. It provides all necessary driving voltages required for an AMEPD panel including VGH, VGL, VSH, VSL and VCOM. Figure 7-7 shows the relation of the voltages. External application circuit is needed to make the on-chip booster & regulator circuit work properly.

Figure 7-7 : Input and output voltage relation chart



- Max voltage difference between VGH and VGL is 42V.

7.5 Panel Driving Waveform

The Vpixel is defined as Figure 7-8, and its relations with GATE, SOURCE are shown in Figure 7-9.

Figure 7-8 : Vpixel Definition

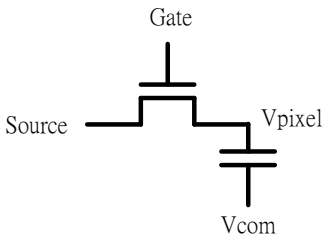
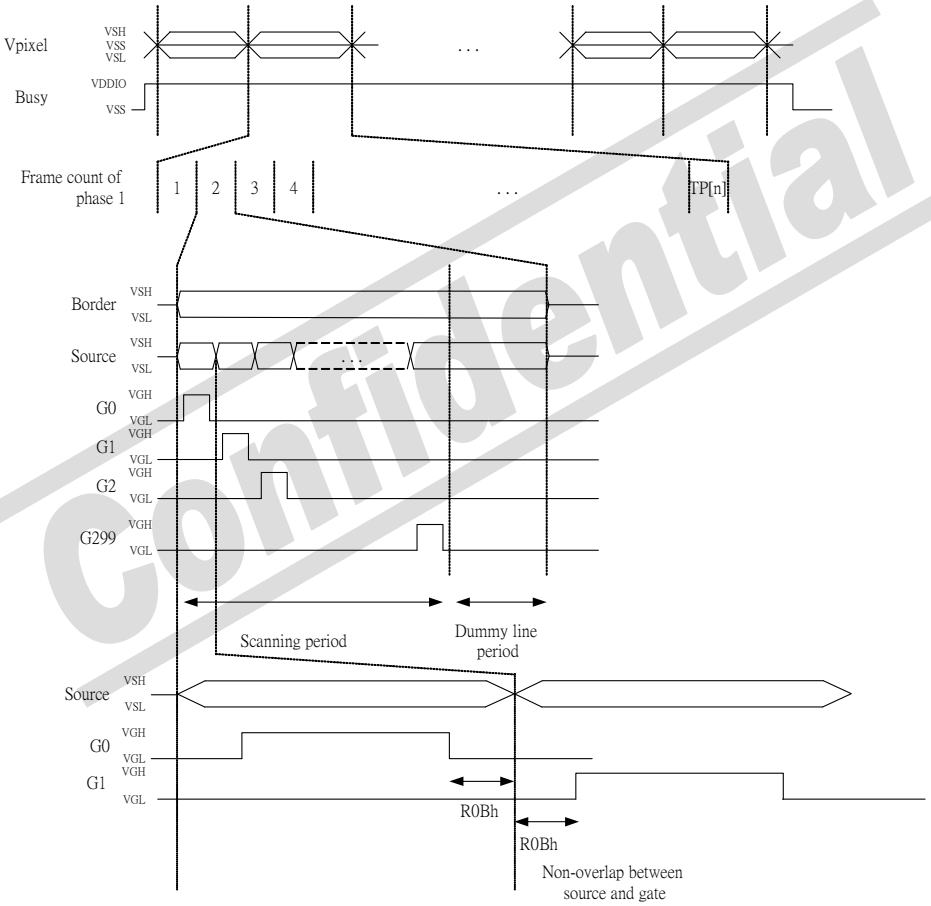


Figure 7-9 : The Relation of Vpixel Waveform with Gate and Source

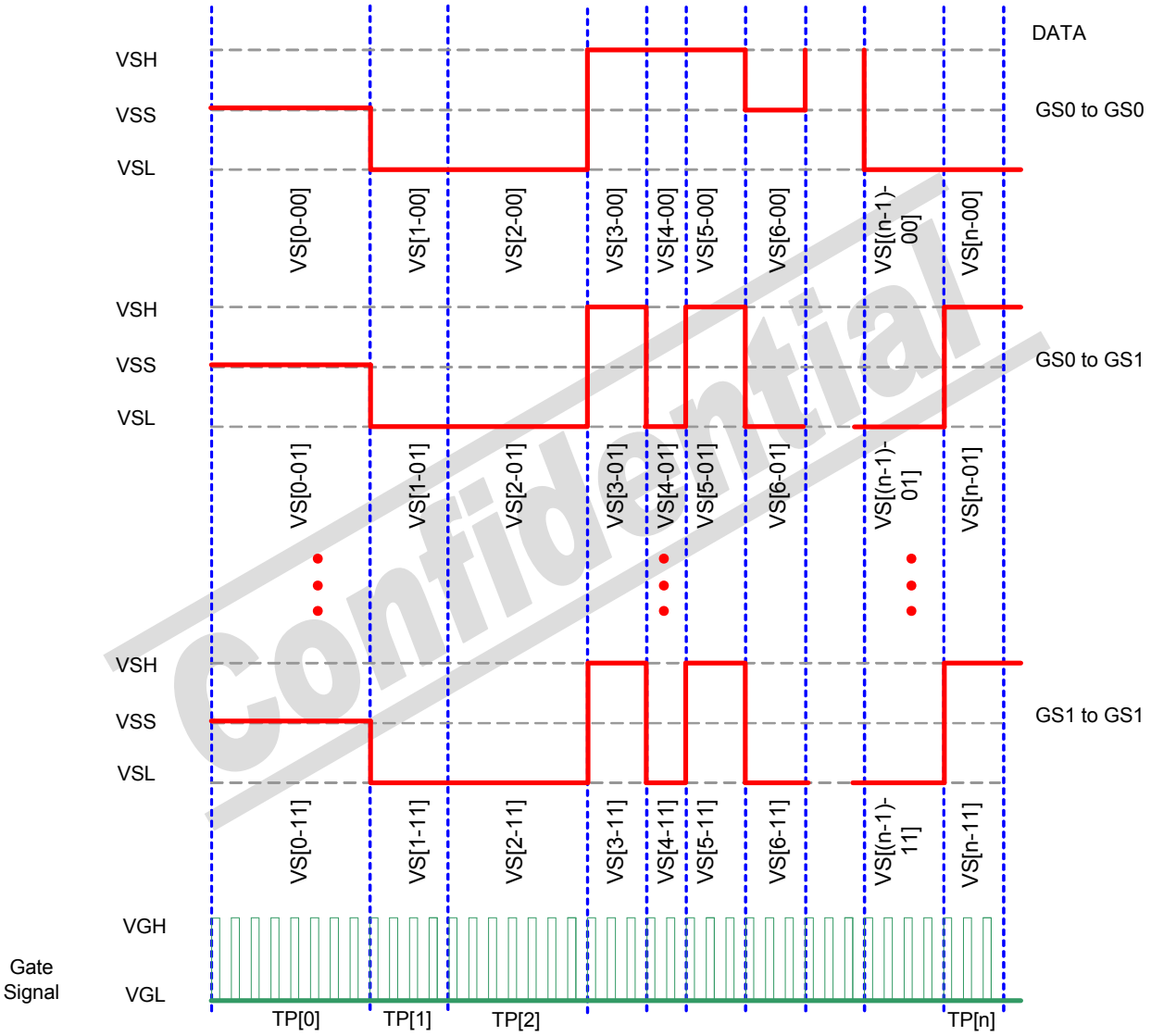


7.6 VCOM Sensing

This functional block provides the scheme to select the optimal VCOM DC level and programmed the setting into OTP.

7.7 Gate and Programmable Source waveform

Figure 7-10 : Programmable Source and Gate waveform illustration



- There are totally 20 phases for programmable Source waveform of different phase length.
- The phase period defined as TP [n] * T_{FRAME}, where TP [n] range from 0 to 15.
- TP [n] = 0 indicates phase skipped
- Source Voltage Level: VS [n-XY] is constant in each phase
- VS [n-XY] indicates the voltage in phase n for transition from GS X to GS Y
  - 00 – VSS
  - 01 – VSH
  - 10 – VSL
  - 11 – NA
- VS [n-XY] and TP[n] are stored in waveform lookup table register [LUT].

7.8 Waveform Look Up Table (LUT)

LUT contains 256 bits, which defines the display driving waveform settings. They are arranged in format shown in Figure 7-11.

Figure 7-11 : VS[n-XY] and TP[n] mapping in LUT

in Decimal	D7	D6	D5	D4	D3	D2	D1	D0
0	VS[0-11]		VS[0-10]		VS[0-01]		VS[0-00]	
1	VS[1-11]		VS[1-10]		VS[1-01]		VS[1-00]	
2	VS[2-11]		VS[2-10]		VS[2-01]		VS[2-00]	
3	VS[3-11]		VS[3-10]		VS[3-01]		VS[3-00]	
4	VS[4-11]		VS[4-10]		VS[4-01]		VS[4-00]	
5	VS[5-11]		VS[5-10]		VS[5-01]		VS[5-00]	
6	VS[6-11]		VS[6-10]		VS[6-01]		VS[6-00]	
7	VS[7-11]		VS[7-10]		VS[7-01]		VS[7-00]	
…	…		…		…		…	
16	VS[16-11]		VS[16-10]		VS[16-01]		VS[16-00]	
17	VS[17-11]		VS[17-10]		VS[17-01]		VS[17-00]	
18	VS[18-11]		VS[18-10]		VS[18-01]		VS[18-00]	
19	VS[19-11]		VS[19-10]		VS[19-01]		VS[19-00]	
20	TP[1]				TP[0]			
21	TP[3]				TP[2]			
…	…				…			
29	TP[19]				TP[18]			
30					VSH/VSL			
31								

7.9 OTP

The OTP is the non-volatile memory and is used to store the information of OTP Selection Option, VCOM value, 7 sets of WAVEFORM SETTING (WS) [256bits x 7] and 6 sets of TEMPERATURE RANGE (TR) [24bits x 6].

The OTP is the non-volatile memory and stored the information of:

- OTP Selection Option
- VCOM value
- Source value
- 7 set of WAVEFORM SETTING (WS) [256bits x 7]
- 6set of TEMPERATURE RANGE (TR) [24bits x 6]

For Programming the WS and TR, Write RAM is required, and the configurations should be

Command: Data Entry mode	C11, D03	Set Address automatic increment setting = X increment and Y increment Set Address counter update in X direction
Command: X RAM address start /end	C44, D00, D18	Set RAM Address for S0 to S199
Command: Y RAM address start /end	C45, D00, D13F	Set RAM Address for G0 to G299
Command: RAM X address counter	C4E, D00	Set RAM X AC as 0
Command: RAM Y address counter	C4F, D000	Set RAM Y AC as 0

The mapping table of OTP is shown in below figure,

Figure 7-12 : OTP Content and Address Mapping

Default OTP ADDRESS	SPARE OTP ADDRESS	WRITE RAM ADDRESS X	WRITE RAM ADDRESS Y	D7	D6	D5	D4	D3	D2	D1	D0
0	256	0	0	VS[0-11]		VS[0-10]		VS[0-01]		VS[0-00]	
1	257	1	0	VS[1-11]		VS[1-10]		VS[1-01]		VS[1-00]	
2	258	2	0	VS[2-11]		VS[2-10]		VS[2-01]		VS[2-00]	
3	259	3	0	VS[3-11]		VS[3-10]		VS[3-01]		VS[3-00]	
4	260	4	0	VS[4-11]		VS[4-10]		VS[4-01]		VS[4-00]	
				…		…		…		…	
18	274	18	0	VS[18-11]		VS[18-10]		VS[18-01]		VS[18-00]	
19	275	19	0	VS[19-11]		VS[19-10]		VS[19-01]		VS[19-00]	
20	276	20	0	TP[1]				TP[0]			
21	277	21	0	TP[3]				TP[2]			
				…				…			
29	285	4	1	TP[19]				TP[18]			
30	286	5	1	Dummy				VSH/VSL			
31	287	6	1	DUMMY							
32	288	7	1	WS[1]							
63	319	13	2								
				…							
192	448	17	7	WS[6]							
223	479	23	8								
224	480	24	8	TEMP[1L][11:0]							
225	481	0	9								
226	482	1	9	TEMP[1-H][11:0]							
227	483	2	9	TEMP[2L][11:0]							
228	484	3	9								
229	485	4	9	TEMP[2-H][11:0]							
				…							
236	492	11	9	TEMP[5L][11:0]							
237	493	12	9								
238	494	13	9	TEMP[5-H][11:0]							
239	495	14	9	TEMP[6L][11:0]							
240	496	15	9								
241	497	16	9	TEMP[6-H][11:0]							

Remark:

- WS [m] means the waveform setting of temperature set m, the configuration are same as the definition in LUT. The corresponding low temperature range of WS[m] defined as TEMP [m-L] and high range defined as TEMP [m-H]
- Load WS [m] from OTP for LUT if Temp [m-L] < Temperature Register <= Temp [m-H]

7.9.1 Temperature Searching Mechanism

Legend:

WS#	Waveform Setting no. #
TR#	Temperature Range no. #
LUT	720 bit register storing the waveform setting (volatile)
Temperature register	12bit Register storing reading from temperature sensor (volatile)
OTP	A non-volatile storing 7 sets of waveform setting and 6 set of temperature range
WS_sel_address	an address pointer indicating the selected WS#

Figure 7-13 : Waveform Setting and Temperature Range # mapping

OTP (non-volatile)

WS0	
WS1	TR1
WS2	TR2
WS3	TR3
WS4	TR4
WS5	TR5
WS6	TR6

IC implementation requirement	
1	Default selection is **WS0**
2	Compare temperature register from **TR1 to TR6**, in sequence. **The last match will be recorded**
	i.e. If the temperature register fall in both TR3 and TR5. WS5 will be selected
3	If none of the range TR1 to TR6 is match, WS0 will be selected.
User application	
1	The default waveform should be programmed as WS0
2	There is no restriction on the sequence of TR1, TR2…. TR6.

7.10 External Temperature Sensor I2C Single Master Interface

The chip provides two I/O lines [TSDA and TSCL] for connecting digital temperature sensor for temperature reading sensing.
TSDA will treat as SDA line and TSCL will treat as SCL line. They are required connecting with external pull-up resistor.

1. If the Temperature value MSByte bit D11 = 0, then
The temperature is positive and value (DegC) = + (Temperature value) / 16
2. If the Temperature value MSByte bit D11 = 1, then
The temperature is negative and value (DegC) = ~ (2's complement of Temperature value) / 16

12-bit binary (2's complement)	Hexadecimal Value	Decimal Value	Value [DegC]
0111 1111 0000	7F0	2032	127
0111 1110 1110	7EE	2030	126.875
0111 1110 0010	7E2	2018	126.125
0111 1101 0000	7D0	2000	125
0001 1001 0000	190	400	25
0000 0000 0010	002	2	0.125
0000 0000 0000	000	0	0
1111 1111 1110	FFE	-2	-0.125
1110 0111 0000	E70	-400	-25
1100 1001 0010	C92	-878	-54.875
1100 1001 0000	C90	-880	-55

7.11 Cascade Mode

The SSD1607 has a cascade mode that can cascade 2 chips to achieve the display resolution up to 400 (sources) x 300 (gates). The pin M/S# is used to configure the chip. When M/S# is connected to VDDIO, the chip is configured as a master chip. When M/S# is connected to VSS, the chip is configured as a slave chip.

When the chip is configured as a master chip, it will be the same as a single chip application, ie, all circuit blocks will be worked as usual. When the chip is configured as a slave chip, its oscillator and booster & regulator circuit will be disabled. The oscillator clock and all booster voltages will be come from the master chip. Therefore, the corresponding pins including CL, VDD, PREVGH, PREVGL, VSH, VSL, VGH, VGL and VCOM must be connected to the master chip.

8 COMMAND TABLE

Table 8-1: Command Table

(D/C#=0, R/W#(WR#) = 0, E(RD#=1) unless specific setting is stated)

Command Table												
R/W#	**D/C#**	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
1	0	-	0	0	0	0	0	A_2	A_1	A_0	Status Read	Read Driver status on • A2: BUSY flag • A1,A0: Chip ID (01 as default)
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting A[8:0]: MUX setting as A[8:0] + 1 POR = 12Bh + 1 MUX B[2]: GD Selects the 1st output Gate GD=0 [POR], G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, … GD=1, G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, … B[1]: SM Change scanning order of gate driver. SM=0 [POR], G0, G1, G2, G3…G299 (left and right gate interlaced) SM=1, G0, G2, G4 …G178, G1, G3, …G299 B[0]: TB TB = 0 [POR], scan from G0 to G299 TB = 1, scan from G299 to G0.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1		0	0	0	0	0	B_2	B_1	B_0		
0	0	02	0	0	0	0	0	0	1	0	Reserve	

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage Control	Set Gate related driving voltage A[7:4]: VGH, 15 to 22V in 0.5V step A[3:0]: VGL, -15 to -20V in 0.5V step VGL default at -20V
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source output voltage magnitude
0	1		0	0	0	0	A_3	A_2	A_1	A_0		A[3:0]: VSH/VSL 10V to 17V in 0.5V step Source setting can be loaded from WS-BYTE31, D[3:0]
0	0	05	0	0	0	0	0	1	0	1	Reserve	
0	0	06	0	0	0	0	0	1	1	0	Reserve	

	VGH	VGL
0000	15	-15
0001	15.5	-15.5
0010	16	-16
0011	16.5	-16.5
0100	17	-17
0101	17.5	-17.5
0110	18	-18
0111	18.5	-18.5
1000	19	-19
1001	19.5	-19.5
1010	20	-20 [POR]
1011	20.5	NA
1100	21	NA
1101	21.5	NA
1110	22 [POR]	NA
1111	NA	NA

	VSH/VSL
0000	10
0001	10.5
0010	11
0011	11.5
0100	12
0101	12.5
0110	13
0111	13.5
1000	14
1001	14.5
1010	15.0 [POR]
1011	15.5
1100	16
1101	16.5
1110	17
1111	N/A

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	07	0	0	0	0	0	1	1	1	Display Control	Display control setting
0	1		0	0	A_5	A_4	0	0	0	0		
0	0	08	0	0	0	0	1	0	0	0	Reserve	
0	0	09	0	0	0	0	1	0	0	1	Reserve	
0	0	0A	0	0	0	0	1	0	1	0	Reserve	
0	0	0B	0	0	0	0	1	0	1	1	Gate and Source non overlap period Control	Set Delay of gate and source non overlap period: - Gate falling edge to source output change - Source change to Gate rising edge Delay Duration in terms of Oscillator clock [$1/F_{OSC}$]
0	1		0	0	0	0	A_3	A_2	A_1	A_0		

A[5]	A[4]	Description
1	1	All Gate output voltage level as VGH
0	1	All Gate output voltage level as VGL
1	0	Selected gate output as VGL, non-selected gate output as VGH
0	0	Selected gate output as VGH, non-selected gate output as VGL [POR]

A [3:0]	Delay Duration
0000	NA
0001	NA
0010	4
…	
0101	10 [POR]
…	
1110	28
1111	NA

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start Control	Booster Enable with Phase 1, Phase 2 and Phase 3 for soft start current setting. A[7:0] -> Soft start setting for Phase1 = 87h [POR] B[7:0] -> Soft start setting for Phase2 = 86h [POR] C[7:0] -> Soft start setting for Phase3 = 85h [POR] Bit Description of each byte:
0	1		1	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		1	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		1	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	0	0D	0	0	0	0	1	1	0	1	Reserve	
0	0	0E	0	0	0	0	1	1	1	0	Reserve	
0	0	0F	0	0	0	0	1	1	1	1	Gate scan start position	Set the scanning start position of the gate driver. The valid range is from 0 to 299. When TB=0: SCN [8:0] = A[8:0] A[8:0] = 000h [POR] When TB=1: SCN [8:0] = 299 - A[8:0] A[8:0] = 000h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		

Bit[6:5]	Duration of Phase
00	10ms
01	20ms
10	30ms
11	40ms

Bit[4:3]	Driving Strength Selection
00	1
01	2
10	3
11	4

Bit[2:0]	Min Off Time Setting of GDR [us]
000	0.27
001	0.34
010	0.4
011	0.54
100	0.8
101	1.54
110	3.34
111	6.58

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control
0	1		0	0	0	0	0	0	0	A_0		A[0] : Description 0 Normal Mode [POR] 1 Enter Deep Sleep Mode
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	A_2	A_1	A_0		
0	0	12	0	0	0	1	0	0	1	0	SWRESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode Note: RAM are unaffected by this command.
0	0	13	0	0	0	1	0	0	1	1	Reserve	
0	0	14	0	0	0	1	0	1	0	0	Reserve	
0	0	15	0	0	0	1	0	1	0	1	Reserve	
0	0	16	0	0	0	1	0	1	1	0	Reserve	
0	0	17	0	0	0	1	0	1	1	1	Reserve	
0	0	18	0	0	0	1	1	0	0	0	Reserve	
0	0	19	0	0	0	1	1	0	0	1	Reserve	
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[7:0] – MSByte 01111111[POR] B[7:0] – LSByte 11110000[POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	0	0	0	0		
0	0	1B	0	0	0	1	1	1	0	1	Temperature Sensor Control (Read from temperature register)	Read from temperature register. X[7:0] – MSByte Y[7:4] – LSByte
1	1		X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0		
1	1		Y_7	Y_6	Y_5	Y_4	0	0	0	0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	1C	0	0	0	1	1	1	0	0	Temperature Sensor Control (Write Command to temperature sensor)	Write Command to temperature sensor A[7:6] – Select no of byte to be sent 00 – Address + pointer 01 – Address + pointer + 1st parameter 10 – Address + pointer + 1st parameter + 2nd pointer 11 – Address A[5:0] – Pointer Setting B[7:0] – 1st parameter C[7:0] – 2nd parameter The command required CLKEN=1.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	0	1D	0	0	0	1	1	1	0	1	Temperature Sensor Control (Load temperature register with temperature sensor reading)	Load temperature register with temperature sensor reading BUSY=H for whole loading period The command required CLKEN=1.
0	0	1E	0	0	0	1	1	1	1	0	Reserve	
0	0	1F	0	0	0	1	1	1	1	1	Reserve	
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h User should not interrupt this operation to avoid corruption of panel images.
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	Option for Display Update Bypass Option used for Pattern Display, which is used for display the RAM content into the Display OLD RAM Bypass option A [7] A[7] = 1: Enable bypass A[7] = 0: Disable bypass [POR] A[4] value will be used as for bypass. A[4] = 0 [POR] A[1:0] Initial Update Option - Source Control
0	1		A_7	0	0	A_4	A_3	A_2	A_1	A_0		

A[1:0]	GSC	GSD
00	GS0	GS0
01 [POR]	GS0	GS1
10	GS1	GS0
11	GS1	GS1

Command Table

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>22</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td rowspan="2">Display Update Control 2</td><td rowspan="2">Display Update Sequence Option:
Enable the stage for Master Activation

<table><tr><th></th><th>Parameter (in Hex)</th></tr><tr><td>Enable Clock Signal,
Then Enable CP
Then Load Temperature value
Then Load LUT
Then INIITIAL DISPLAY
Then PATTERN DISPLAY
Then Disable CP
Then Disable OSC</td><td>FF
[POR]</td></tr><tr><td>Enable Clock Signal,
Then Enable CP
Then Load Temperature value
Then Load LUT
Then PATTERN DISPLAY
Then Disable CP
Then Disable OSC</td><td>F7</td></tr><tr><td>To Enable Clock Signal
(CLKEN=1)</td><td>80</td></tr><tr><td>To Enable Clock Signal,
then Enable CP
(CLKEN=1, CPEN=1)</td><td>C0</td></tr><tr><td>To INITIAL DISPLAY + PATTEN DISPLAY</td><td>0C</td></tr><tr><td>To INITIAL DISPLAY</td><td>08</td></tr><tr><td>To DISPLAY PATTEN</td><td>04</td></tr><tr><td>To Disable CP,
then Disable Clock Signal
(CLKEN=1, CPEN=1)</td><td>03</td></tr><tr><td>To Disable Clock Signal
(CLKEN=1)</td><td>01</td></tr></table>
Remark:
CLKEN=1:
If CLS=VDDIO then Enable OSC
If CLS=VSS then Enable External Clock
CLKEN=0:
If CLS=VDDIO then Disable OSC
AND
INTERNAL CLOCK Signal = VSS,</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>0</td><td>23</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Reserve</td><td></td></tr>
<tr><td>0</td><td>0</td><td>24</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Write RAM</td><td>After this command, data entries will be written into the RAM until another command is written. Address pointers will advance accordingly.</td></tr>
<tr><td>0</td><td>0</td><td>25</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>Read RAM</td><td>After this command, data read on the MCU bus will fetch data from RAM, until another command is written. Address pointers will advance accordingly.</td></tr>
<tr><td>0</td><td>0</td><td>26</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Reserve</td><td></td></tr>
<tr><td>0</td><td>0</td><td>27</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>Reserve</td><td></td></tr>
</table>

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	**Command**	**Description**
0	0	28	0	0	1	0	1	0	0	0	VCOM Sense	Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value. The sensed VCOM voltage is stored in register The command required CLKEN=1.
0	0	29	0	0	1	0	1	0	0	1	VCOM Sense Duration	Stabling time between entering VCOM sensing mode and reading acquired. VCOM sense duration = Setting + 1 Seconds 0x09(10Seconds) [POR]
0	1		0	0	0	0	A_3	A_2	A_1	A_0		
0	0	2A	0	0	1	0	1	0	1	0	Program VCOM OTP	Program VCOM register into OTP
0	0	2B	0	0	1	0	1	0	1	1	Reserve	
0	0	2C	0	0	1	0	1	0	1	1	Write VCOM register	Write VCOM register from MCU interface
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	2D	0	0	1	0	1	1	0	1	Read OTP Registers	Read register reading to MCU A [7:0] Spare OTP Option B [7:0] VCOM Register
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	0	2E	0	0	1	0	1	1	1	0	Reserve	
0	0	2F	0	0	1	0	1	1	1	1	Reserve	
0	0	30	0	0	1	1	0	0	0	0	Program WS OTP	Program OTP of Waveform Setting The contents should be written into RAM before sending this command.
0	0	31	0	0	1	1	0	0	0	1	Reserve	
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU [240 bits], (excluding the VSH/VSL and Dummy bit)
0 0 0 … 0 0	1 1 1 … 1 1		LUT [30 bytes]									
0	0	33	0	0	1	1	0	0	1	1	Read LUT register	Read from LUT register [240 bits] (excluding the VSH/VSL and Dummy bit)
1 1 1 … 1 1	1 1 1 … 1 1		LUT [30 bytes]									

Command Table

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>34</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Reserve</td><td></td></tr>
<tr><td>0</td><td>0</td><td>35</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>Reserve</td><td></td></tr>
<tr><td>0</td><td>0</td><td>36</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Program OTP selection</td><td>Program OTP Selection according to the OTP Selection Control [R37h]</td></tr>
<tr><td>0</td><td>0</td><td>37</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>OTP selection Control</td><td>Write the OTP Selection:
<table><tr><td>A[7]=1</td><td>spare VCOM OTP</td></tr><tr><td>A[6]</td><td>VCOM_Status</td></tr><tr><td>A[5]=1</td><td>spare WS OTP</td></tr><tr><td>A[4]</td><td>WS_Status</td></tr></table>A[3:0] are reserved OTP bit. User can treat the bits as Version Control.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>38</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Reserve</td><td></td></tr>
<tr><td>0</td><td>0</td><td>39</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Reserve</td><td></td></tr>
<tr><td>0</td><td>0</td><td>3A</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Set dummy line period</td><td>Set number of dummy line period

A[6:0]: Number of dummy line period in term of TGate
A[6:0] = 16h [POR]

Available setting 0 to 127.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>3B</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Set Gate line width</td><td>Set Gate line width (TGate)
A[3:0] Line width in us

<table><tr><th>A[3:0]</th><th>TGate</th></tr><tr><td>0000</td><td>30</td></tr><tr><td>0001</td><td>34</td></tr><tr><td>0010</td><td>38</td></tr><tr><td>0011</td><td>40</td></tr><tr><td>0100</td><td>44</td></tr><tr><td>0101</td><td>46</td></tr><tr><td>0110</td><td>52</td></tr><tr><td>0111</td><td>56</td></tr><tr><td>1000</td><td>62 [POR]</td></tr><tr><td>1001</td><td>68</td></tr><tr><td>1010</td><td>78</td></tr><tr><td>1011</td><td>88</td></tr><tr><td>1100</td><td>104</td></tr><tr><td>1101</td><td>125</td></tr><tr><td>1110</td><td>156</td></tr><tr><td>1111</td><td>208</td></tr></table>
Remark: Default value will give 50Hz Frame frequency under 22 dummy line pulse setting.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
</table>

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A [7] Follow Source at Initial Update Display A [7]=0: [POR] A [7]=1: Follow Source at Initial Update Display for VBD, A [6:0] setting are being overridden at Initial Display STAGE. A [6] Select GS Transition/ Fix Level for VBD A [6]=0: Select GS Transition A[3:0] for VBD A [6]=1: Select FIX level Setting A[5:4] for VBD [POR] A [5:4] Fix Level Setting for VBD A[5:4] = 00: VBD level = VSS; 01: VSH; 10: VSL; 11[POR]: HiZ A [1:0] GS transition setting for VBD (Select waveform like data A[3:2] to data A[1:0]) A[1:0] = 00: GSA = GS0, GSB = GS0; 01 [POR]: GS0, GS1; 10: GS1, GS0; 11: GS1, GS1
0	1		A_7	A_6	A_5	A_4	0	0	A_1	A_0		
0	0	3D	0	0	1	1	1	1	0	1	Reserve	
0	0	3E	0	0	1	1	1	1	1	0	Reserve	
0	0	3F	0	0	1	1	1	1	1	1	Reserve	
0	0	40	0	1	0	0	0	0	0	0	Reserve	
0	0	41	0	1	0	0	0	0	0	1	Reserve	
0	0	42	0	1	0	0	0	0	1	0	Reserve	
0	0	43	0	1	0	0	0	0	1	1	Reserve	
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit A[4:0]: XSA[4:0], XStart, POR = 00h B[4:0]: XEA[4:0], XEnd, POR = 18h
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	B_4	B_3	B_2	B_1	B_0		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit A[8:0]: YSA[8:0], YStart, POR = 000h B[8:0]: YEA[8:0], YEnd, POR = 12Bh
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		0	0	0	0	0	0	0	B_8		
0	0	46	0	1	0	0	0	1	1	0	Reserve	
0	0	47	0	1	0	0	0	1	1	1	Reserve	

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	48	0	1	0	0	1	0	0	0	Reserve	
0	0	49	0	1	0	0	1	0	0	1	Reserve	
0	0	4A	0	1	0	0	1	0	1	0	Reserve	
0	0	4B	0	1	0	0	1	0	1	1	Reserve	
0	0	4C	0	1	0	0	1	1	0	0	Reserve	
0	0	4D	0	1	0	0	1	1	0	1	Reserve	
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[4:0]: XAD[4:0], POR is 00h
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: YAD8:0], POR is 000h
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1	FF	1	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read Commands.

9 Command DESCRIPTION

9.1 Driver Output Control (01h)

This double byte command has multiple configurations and each bit setting is described as follows:

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0
POR		0	0	1	0	1	0	1	1
W	1								MUX8
POR									1
W	1						GD	SM	TB
POR							0	0	0

MUX[8:0]: Specify number of lines for the driver: MUX[8:0] + 1. Multiplex ratio (MUX ratio) from 16 MUX to 300MUX.

GD: Selects the 1st output Gate

This bit is made to match the GATE layout connection on the panel. It defines the first scanning line.

SM: Change scanning order of gate driver.

When SM is set to 0, left and right interlaced is performed.

When SM is set to 1, no splitting odd / even of the GATE signal is performed,

Output pin assignment sequence is shown as below (for 300 MUX ratio):

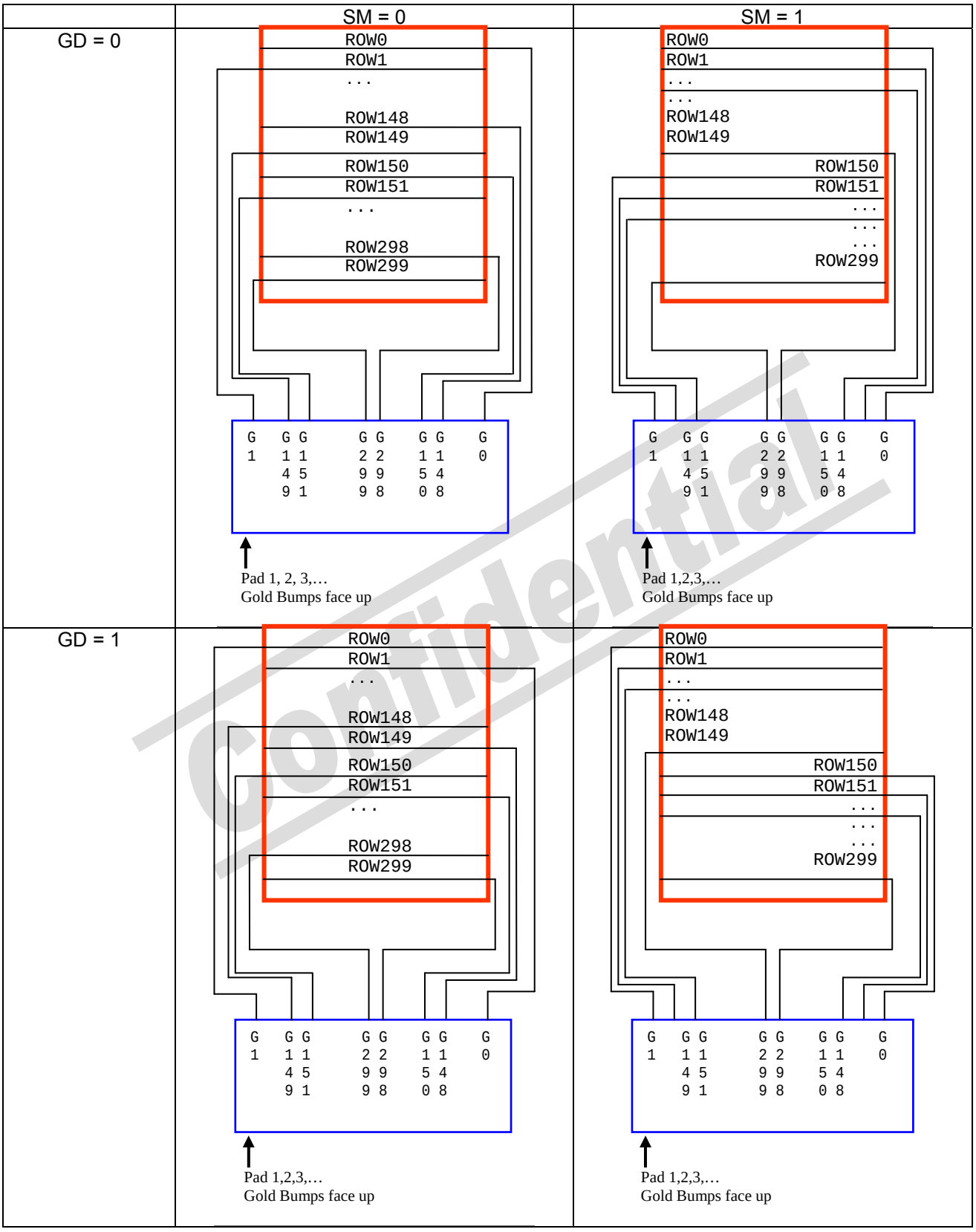
	SM=0	SM=0	SM=1	SM=1
Driver	**GD=0**	**GD=1**	**GD=0**	**GD=1**
G0	ROW0	ROW1	ROW0	ROW150
G1	ROW1	ROW0	ROW150	ROW0
G2	ROW2	ROW3	ROW1	ROW151
G3	ROW3	ROW2	ROW151	ROW1
:	:	:	:	:
G148	ROW148	ROW149	ROW74	ROW224
G149	ROW149	ROW148	ROW224	ROW74
G150	ROW150	ROW151	ROW75	ROW225
G151	ROW151	ROW150	ROW225	ROW75
:	:	:	:	:
G296	ROW296	ROW297	ROW148	ROW298
G297	ROW297	ROW296	ROW298	ROW148
G298	ROW298	ROW299	ROW149	ROW299
G299	ROW299	ROW298	ROW299	ROW149

See “Scan Mode Setting” on next page.

TB: Change scanning direction of gate driver.

This bit defines the scanning direction of the gate for flexible layout of signals in module either from up to down (TB = 0) or from bottom to up (TB = 1).

Figure 9-1: Output pin assignment on different Scan Mode Setting



9.2 Gate Scan Start Position (0Fh)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
POR		0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	0	SCN8
POR		0	0	0	0	0	0	0	0

This command is to set Gate Start Position for determining the starting gate of display RAM by selecting a value from 0 to299. Figure 9-2 shows an example using this command of this command when MUX ratio= 300 and MUX ratio= 150 “ROW” means the graphic display data RAM row.

Figure 9-2: Example of Set Display Start Line with no Remapping

	MUX ratio (01h) = 12Bh	MUX ratio (01h) = 095h	MUX ratio (01h) = 095h
GATE Pin	Gate Start Position (0Fh) = 000h	Gate Start Position (0Fh) = 000h	Gate Start Position (0Fh) = 046h
G0	ROW0	ROW0	-
G1	ROW1	ROW1	-
G2	ROW2	ROW2	-
G3	ROW3	ROW3	-
:	:	:	:
:	:	:	:
G73	:	:	-
G74	:	:	-
G75	:	:	ROW75
G76	:	:	ROW76
:	:	:	:
:	:	:	:
G148	ROW148	ROW148	:
G149	ROW149	ROW149	:
G150	ROW150	-	:
G151	ROW151	-	:
:	:	:	:
	:	:	:
G223	:	:	ROW223
G224	:	:	ROW224
G225	:	:	-
G226	:	:	-
	:	:	:
:	:	:	:
G296	ROW296	-	-
G297	ROW297	-	-
G298	ROW298	-	-
G299	ROW299	-	-
Display Example			

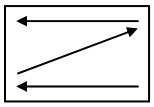
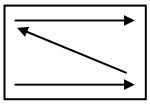
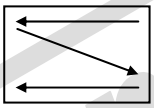
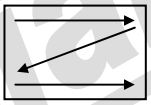
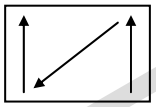
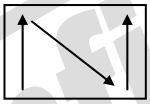
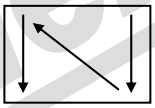
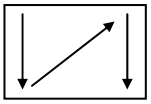
9.3 Data Entry Mode Setting (11h)

This command has multiple configurations and each bit setting is described as follows:

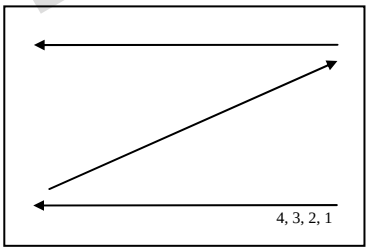
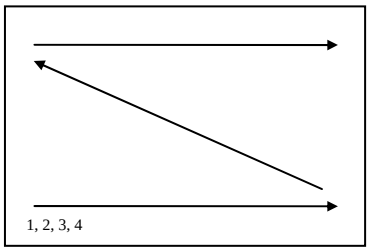
R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1						AM	ID1	ID0
POR		0	0	0	0	0	0	0	0

ID[1:0]: The address counter is automatically incremented by 1, after data is written to the RAM when ID[1:0] = “01”. The address counter is automatically decremented by 1, after data is written to the RAM when ID[1:0] = “00”. The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. The direction of the address when data is written to the RAM is set by AM bits.

AM: Set the direction in which the address counter is updated automatically after data are written to the RAM. When AM = “0”, the address counter is updated in the X direction. When AM = “1”, the address counter is updated in the Y direction. When window addresses are selected, data are written to the RAM area specified by the window addresses in the manner specified with ID[1:0] and AM bits.

	ID [1:0]="00” X: decrement Y: decrement	ID [1:0]="01” X: increment Y: decrement	ID [1:0]="10” X: decrement Y: increment	ID [1:0]="11” X: increment Y: increment
AM="0” X-mode	00,00h  18,1BFh	00,00h  18,1BFh	00,00h  18,1BFh	00,00h  18,1BFh
AM="1” Y-mode	00,00h  18,1BFh	00,00h  18,1BFh	00,00h  18,1BFh	00,00h  18,1BFh

The pixel sequence is defined by the ID [0],

	ID[1:0]="00” X: decrement Y: decrement	ID[1:0]="01” X: increment Y: decrement
AM="0” X-mode	00,00h  4, 3, 2, 1 18,1BFh	00,00h  1, 2, 3, 4 18,1BFh

9.4 Set RAM X - Address Start / End Position (44h)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1				XSA4	XSA3	XSA2	XSA1	XSA0
POR		0	0	0	0	0	0	0	0
W	1				XEA4	XEA3	XEA2	XEA1	XEA0
POR		0	0	0	1	1	1	1	1

XSA[4:0]/XEA[4:0]: Specify the start/end positions of the window address in the X direction by 8 times address unit. Data is written to the RAM within the area determined by the addresses specified by XSA [4:0] and XEA [4:0]. These addresses must be set before the RAM write.
It allows on XEA [4:0] ≤ XSA [4:0]. The settings follow the condition on 00h ≤ XSA [4:0], XEA [4:0] ≤ 18h. The windows is followed by the control setting of Data Entry Setting (R11h)

9.5 Set RAM Y - Address Start / End Position (45h)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	YSA7	YSA6	YSA5	YSA4	YSA3	YSA2	YSA1	YSA0
POR	0	0	0	0	0	0	0	0	
W	1	0	0	0	0	0	0	0	YSA8
POR		0	0	0	0	0	0	0	0
W	1	YEA7	YEA6	YEA5	YEA4	YEA3	YEA2	YEA1	YEA0
POR		1	1	0	1	0	0	1	1
W	1	0	0	0	0	0	0	0	YEA8
POR		1	1	0	1	0	0	1	1

YSA[8:0]/YEA[8:0]: Specify the start/end positions of the window address in the Y direction by an address unit. Data is written to the RAM within the area determined by the addresses specified by YSA [8:0] and YEA [8:0]. These addresses must be set before the RAM write.
It allows YEA [8:0] ≤ YSA [8:0]. The settings follow the condition on 00h ≤ YSA [8:0], YEA [8:0] ≤ 1BFh. The windows is followed by the control setting of Data Entry Setting (R11h)

9.6 Set RAM Address Counter (4Eh-4Fh)

Reg#	R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
4Eh	W	1				XAD4	XAD3	XAD2	XAD1	XAD0
	POR		0	0	0	0	0	0	0	0
4Fh	W	1	YAD7	YAD6	YAD5	YAD4	YAD3	YAD2	YAD1	YAD0
	POR		0	0	0	0	0	0	0	0
4Fh	W	1								YAD8
	POR									0

XAD[4:0]: Make initial settings for the RAM X address in the address counter (AC).
YAD[8:0]: Make initial settings for the RAM Y address in the address counter (AC).

After RAM data is written, the address counter is automatically updated according to the settings with AM, ID bits and setting for a new RAM address is not required in the address counter. Therefore, data is written consecutively without setting an address. The address counter is not automatically updated when data is read out from the RAM. RAM address setting cannot be made during the standby mode. The address setting should be made within the area designated with window addresses which is controlled by the Data Entry Setting (R11h) {AM, ID[1:0]} ; RAM Address XStart / XEnd Position (R44h) and RAM Address Ystart /Yend Position (R45h). Otherwise undesirable image will be displayed on the Panel.

10 Typical Operating Sequence

10.1 Normal Display

Sequence	Action by	Command	Action Description	Remark
1	User	-	Power on (VCI supply);	
2	User	-	HW Reset	
	IC		After HW reset, the IC will have Registers load with POR value Ready for command input VCOM register loaded with OTP value IC enter idle mode	
3		-	Send initial code to driver including setting of	
	User	C 01	Command: Panel configuration (MUX, Source gate scanning direction)	
	User	C 03	Command: VGH, VGL voltage	
	User	C 04	Command: VSH / VSL voltage	
	User	C 3A	Command: Set dummy line pulse period	
	User	C 3B	Command: Set Gate line width	
	User	C 3C	Command: Select Border waveform	
4		-	Data operations	
	User	C 11	Command: Data Entry mode	
	User	C 44	Command: X RAM address start /end	
	User	C 45	Command: Y RAM address start /end	
	User	C 4E	Command: RAM X address counter	
	User	C 4F	Command: RAM Y address counter	
	User	C 24	Command: write display data to RAM	
			Ram Content for Display	
5	User	C 22	Command: Display Update Control 2	
	User	C 20	Command: Master Acitivation	
	IC	-	Booster and regulators turn on	
	IC	-	Load temperature register with sensor reading	
	IC	-	Load LUT register with corresponding waveform setting stored in OTP)	
	IC	-	Send output waveform according initial update option	
	IC	-	Send output waveform according to data	
	IC	-	Booster and Regulators turn off	
	IC	-	Back to idle mode	
6	User	-	IC power off;	

OTP Selection bit:

Set on R37h, and read from R2Dh, A[7:6] used for VCOM and A[5:4] used for OTP

A[7:6] / [5:4]	Description
00	It indicates fresh device, OTP read and program would be made on Default OTP set User required setting and programming the bits into 01.
01	It indicates default OTP programmed device, OTP read would be made on Default OTP set. User require setting and programming the bits into 11
11	It indicates SPARE OTP programmed device, only OTP read would be made on SPARE OTP set. User should stop the OTP programming if 11 is found at OTP checking stage

10.2 VCOM OTP Program

Sequence	Action by	Command	Action Description	Remark
1	User	-	Power on (VCI and VPP supply)	
2	User	-	HW Reset	
3	User	C 2D	Check whether the IC status and determine whether "default" or "spare" OTP should be used	
4	User		If the IC had been OTP twice (both default and spare had been used up). The operation should stop	
5	User	C 37	Proceed OTP sequence. Command: Indicate which OTP location to be use (default or spare)	OTP selection register
	User	C 22 D 80 C 20	Command: CLKEN=1	
	User	-	Wait until BUSY = L	
6	User	C 36	Program OTP selection register	
	User	-	Wait until BUSY = L	
	User	-	Power OFF (VPP supply)	
7		-	Send initial code to driver including setting of (or leave as POR)	VCOM sensing should have same setting during application
	User	C 01	Command: Panel configuration (MUX, Source gate scanning direction)	
	User	C 03	Command: VGH, VGL voltage	
	User	C 04	Command: VSH / VSL voltage	
	User	C 3A	Command: Set dummy line pulse period	
	User	C 32	VCOM sense required full set of LUT for operation, USER required writing LUT in register 32h	
		-	LUT parameter	
	User	C 22 D 40 C 20	Command: Booster on and High voltage ready	
	User	-	Wait until BUSY = L	
8	User	C 28	Command: Enter VCOM sensing mode	
	IC	-	VCOM pin in sensing mode	
	IC	-	All Source cell have VSS output	
			All Gate scanning continuously	
	IC	-	Wait for 10s	According to R29h
	IC	-	Detect VCOM voltage and store in register	
	IC	-	All Gate Stop Scanning.	
	User	-	Wait until BUSY = L	
9	User	C 22 D 02 C 20	Command: Booster and High voltage disable	
	User	-	Wait until BUSY = L	
	User	-	Power On (VPP supply)	
10	User	C 2A	Command: VCOM OTP program	
	User	-	Wait until BUSY = L	
11	User	C 22 D 01 C 20	Command: CLKEN=0	
	User	-	Wait until BUSY = L	
12	User	-	IC power off (VCI and VPP Supply)	

10.3 WS OTP Program

Sequence	Action by	Command	Action Description	Remark
1	User	-	Power on (VCI supply)	
2	User	-	Power on (VPP supply)	
3	User	-	HW Reset	
4	User	C 2D	Check whether the IC status and determine whether "default" or "spare" OTP should be used	
5	User		If the IC had been OTP twice (both default and spare had been used up). The operation should stop	
6	User	C 37	Proceed OTP sequence. Command: Indicate which OTP location to be use (default or spare)	OTP selection register
	User	C 22 D 80 C 20	Command: CLKEN=1	
	User	-	Wait BUSY = L	
7	User	C 36	Program OTP selection register	
	User	-	Wait BUSY = L	
8	User	C 24	Write corresponding data into RAM	
			Following specific format	
			Write into RAM	
			Full LUT (11 entries + Temperature range) must be written at the same time	
	User	C 4E D 00 C 4F D 00	Command: Initial Ram address counter	
9	User	C 30	Waveform Setting OTP programming	
	IC	-	BUSY pin pull H	
	IC	-	Check the OTP Selection	
	IC	-	IC control OTP programming time, and transfer data to selected OTP	
	IC	-	BUSY pin pull L	
	User	-	Wait BUSY = L	
10	User	C 22 D 01 C 20	Command: CLKEN=0	
	User	-	Wait BUSY = L	
11	User	-	IC power off	

11 ABSOLUTE MAXIMUM RATING

Table 11-1: Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CI}	Logic supply voltage	-0.5 to +4.0	V
V_{IN}	Logic Input voltage	-0.5 to V_{DDIO}+0.5	V
V_{OUT}	Logic Output voltage	-0.5 to V_{DDIO}+0.5	V
T_{OPR}	Operation temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-65 to +150	°C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. This device is not radiation protected.

12 ELECTRICAL CHARACTERISTICS

The following specifications apply for: VSS=0V, VCI=3.0V, VDD=1.8V, T_{OPR}=25ºC.

Table 12-1: DC Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
V_{CI}	VCI operation voltage		VCI	2.4	3.0	3.7	V
V_{DD}	VDD operation voltage		VDD	1.7	1.8	1.9	V
V_{COM}	VCOM output voltage		VCOM	-4.0		-0.2	V
V_{GATE}	Gate output voltage		G0-299	-20		+22	V
$V_{GATE(p-p)}$	Gate output peak to peak voltage		G0-299			42	V
V_{SH}	Positive Source output voltage		S0-199	+10		+17	V
V_{SL}	Negative Source output voltage		S0-199		-VSH		V
V_{IH}	High level input voltage		D[7:0], CS#, R/W#, D/C#, E, RES#, CLS, M/S#, CL, BS[2:0], TSDA, TSCL	$0.8V_{DDIO}$			V
V_{IL}	Low level input voltage					$0.2V_{DDIO}$	V
V_{OH}	High level output voltage	IOH = -100uA	D[7:0], BUSY, CL, TSDA, TSCL	$0.9V_{DDIO}$			V
V_{OL}	Low level output voltage	IOL = 100uA				$0.1V_{DDIO}$	V
V_{PP}	OTP Program voltage		VPP		7.5		V
Idslp_VCI	Deep Sleep mode current	VCI=3.7V DC/DC OFF No clock No output load Ram data not retain	V_{CI}		2	5	uA
Islp_VCI	Sleep mode current	VCI=3.7V DC/DC OFF No clock No output load Ram data retain	VCI		35	50	uA
Iopr_VCI	Operating current	VCI=3.0V DC/DC on VGH=22V VGL=-20V VSH=15V VSL=-15V VCOM = -2V No waveform transitions. No loading. No RAM read/write No OTP read /write Osc on Bandgap on	VCI		2000		uA

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
V_{GH}	Operating Mode Output Voltage	VCI=3.0V DC/DC on VGH=22V VGL=-20V VSH=15V VSL=-15V VCOM = -2V No waveform transitions. No loading. Osc on Bandgap on	VGH	21	22	23	V
V_{SH}			VSH	14.5	15	15.5	V
V_{COM}			VCOM	-2.5	-2	-1.5	V
V_{SL}			VSL	-15.5	-15	-14.5	V
V_{GL}			VGL	-21	-20	-19	V

Table 12-2: Regulators Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
IVGH	VGH current	VGH = 22V	VGH			400	uA
IVGL	VGL current	VGL = -20V	VGL			600	uA
IVSH	VSH current	VSH = +15V	VSH			4000	uA
IVSL	VSL current	VSL = -15V	VSL			4000	uA
IVCOM	VCOM current	VCOM = -2V	VCOM			100	uA

13 AC CHARACTERISTICS

13.1 Oscillator frequency

The following specifications apply for: VSS=0V, VCI=3.0V, VDD=1.8V, T_{OPR}=25ºC.

Table 13-1: Oscillator Frequency

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
Fosc	Internal Oscillator frequency	VCI=2.4 to 3.7V	CL	0.95	1	1.05	MHz

13.2 Interface Timing

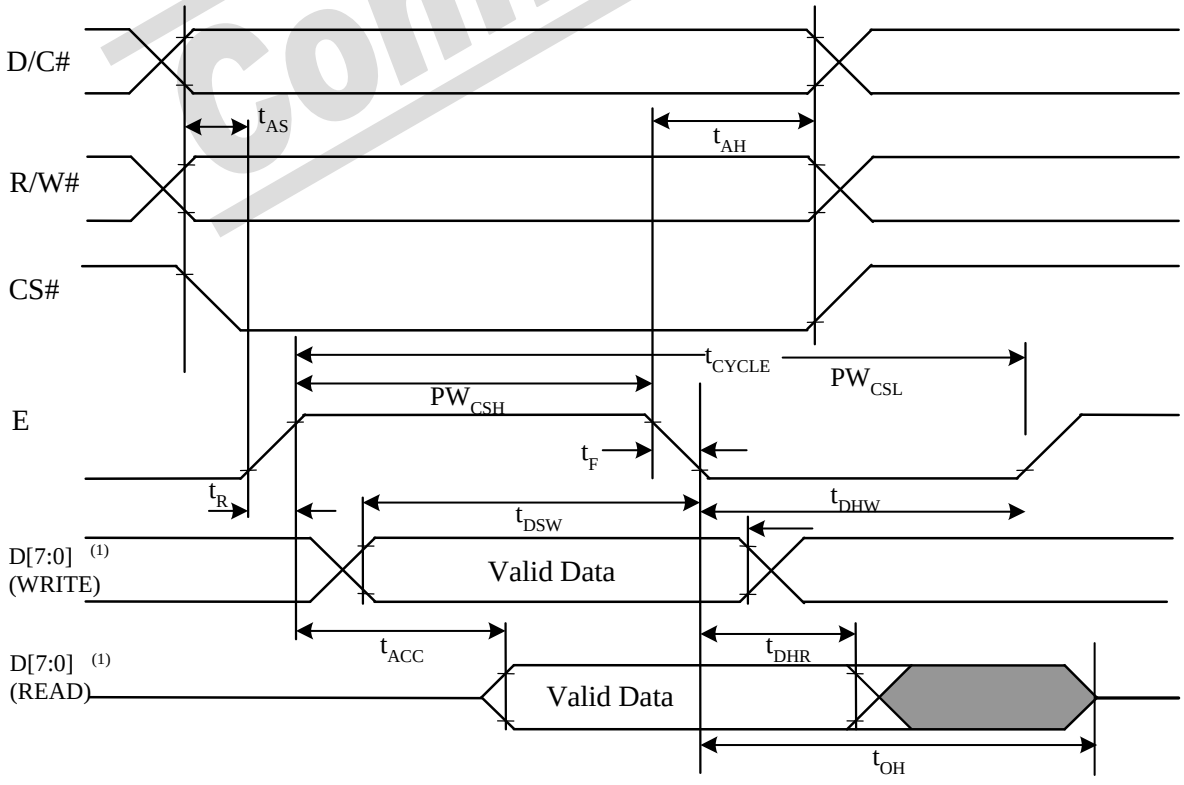
13.2.1 MCU 6800-Series Parallel Interface

Table 13-2 : 6800-Series MCU Parallel Interface Timing Characteristics

(V_{DDIO} - V_{SS} = 2.4V to 3.7V, T_{OPR} = 25°C, C_L=20pF)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time [20% ~ 80%]	-	-	15	ns
t_F	Fall Time [20% ~ 80%]	-	-	15	ns

Figure 13-1 : MCU 6800-series parallel interface characteristics



13.2.2 MCU 8080-Series Parallel Interface

Table 13-3 : MCU 8080-Series Parallel Interface Timing Characteristics

(V_{DDIO} - V_{SS} = 2.4V to 3.7V, T_{OPR} = 25°C, C_L=20pF)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time [20% ~ 80%]	-	-	15	ns
t_F	Fall Time [20% ~ 80%]	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 13-2 : 8080-series parallel interface characteristics (Form 1)

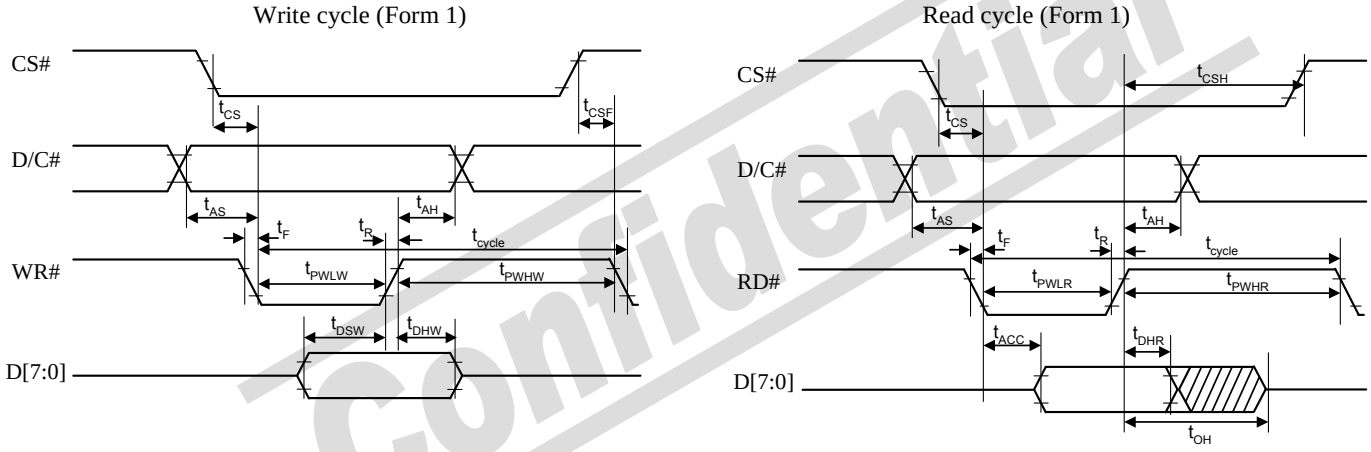
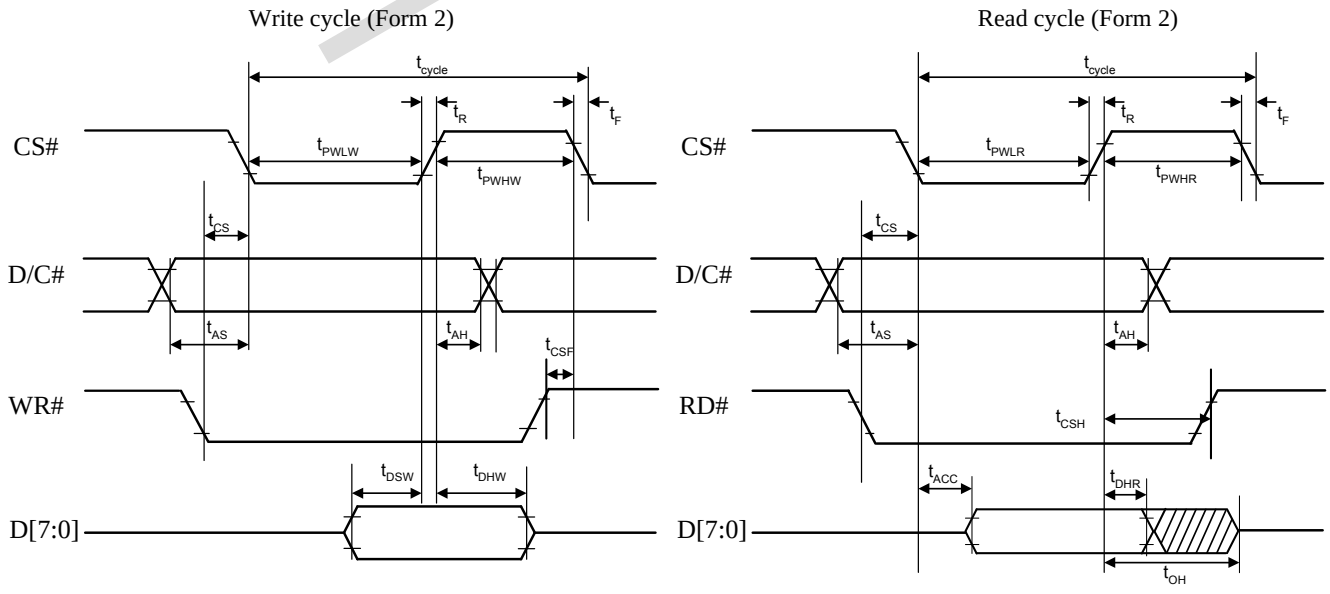


Figure 13-3 : 8080-series parallel interface characteristics (Form 2)



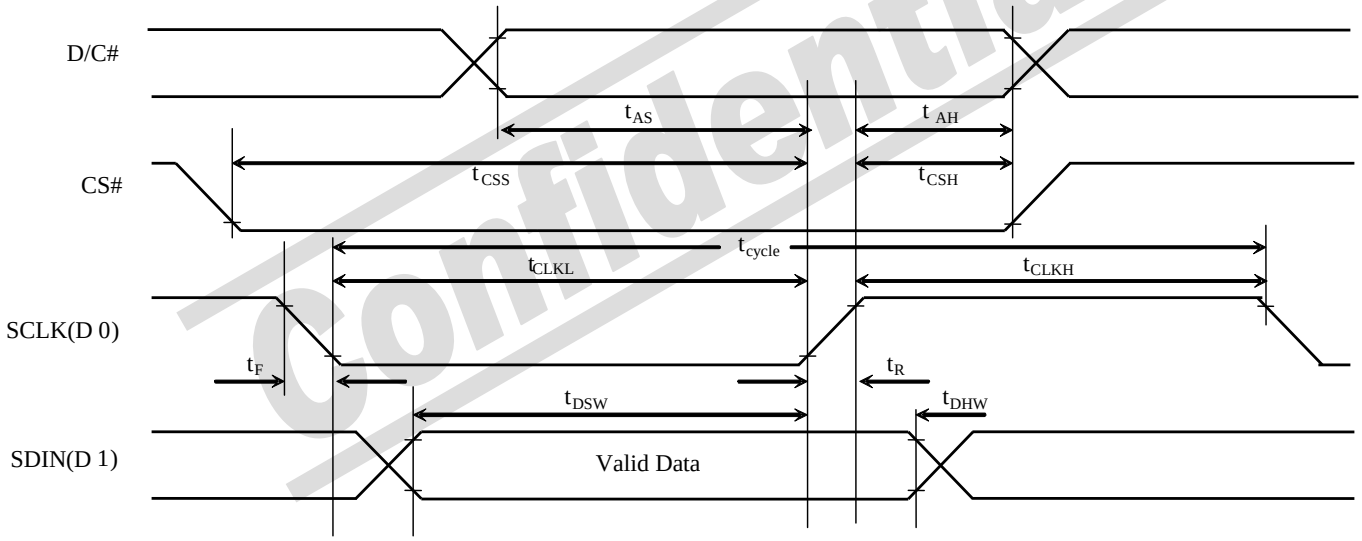
13.2.3 Serial Peripheral Interface

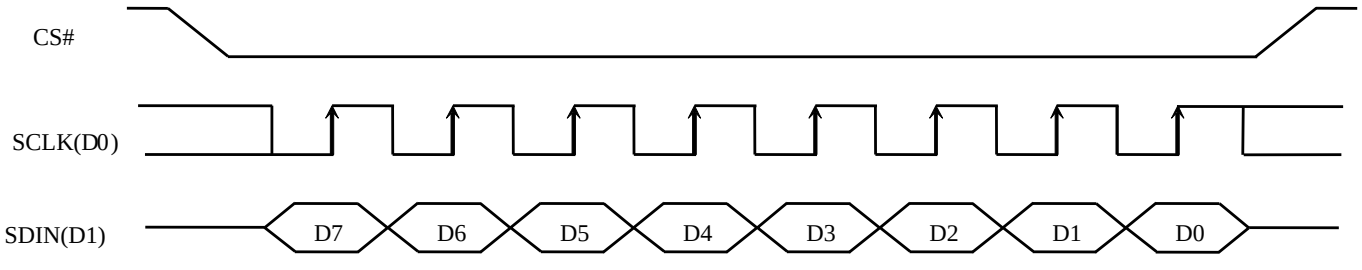
Table 13-4 : Serial Peripheral Interface Timing Characteristics

(V_{DDIO} - V_{SS} = 2.4V to 3.7V, T_{OPR} = 25°C, C_L=20pF)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time [20% ~ 80%]	-	-	15	ns
t_F	Fall Time [20% ~ 80%]	-	-	15	ns

Figure 13-4 : Serial peripheral interface characteristics





14 APPLICATION CIRCUIT

Figure 14-1 : Booster Connection Diagram

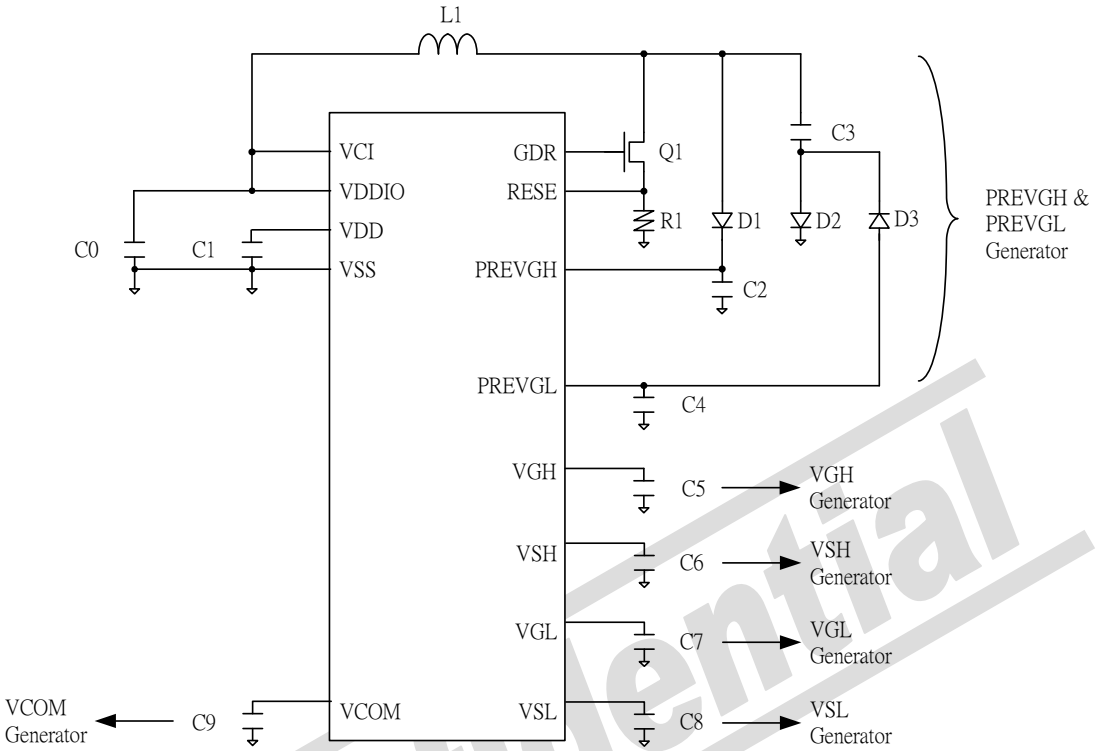


Figure 14-2 : Typical application diagram with SPI interface

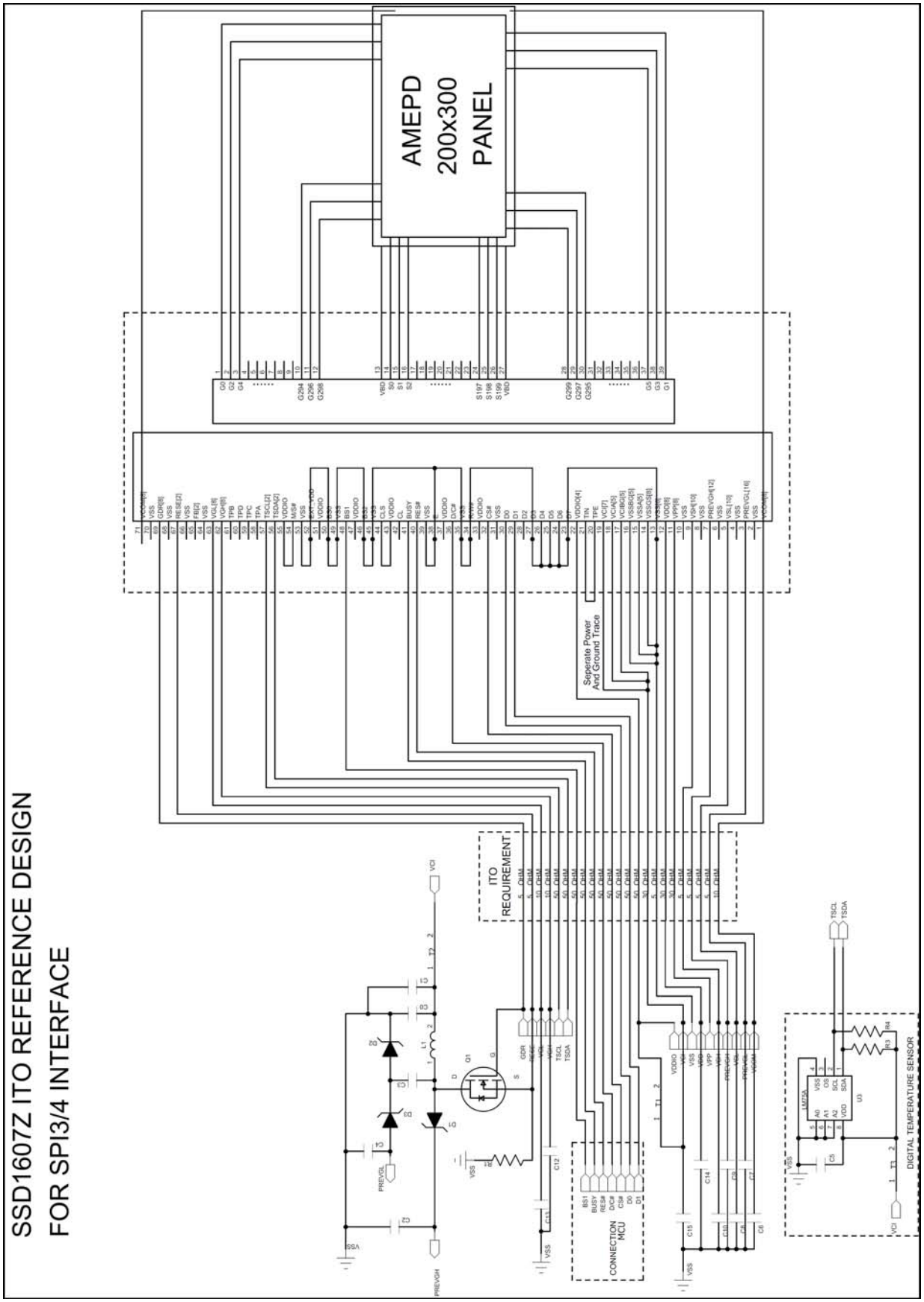


Table 14-1 : Reference Component Value

Part Name	Value	Max Volt. Rating [In V]	Pins Connected	MAX COG ITO resistance [in Ohm]
C0	1uF	6	VCI, VDDIO, VSS	5
C1	1uF	6	VDD, VSS	30
C2	1uF	50	PREVGH	5
C3	4.7uF	50	L1 and D2/D3	NA
C4	1uF	50	PREVGL	5
C5	1uF	25	VGH	10
C6	1uF	25	VSH	5
C7	1uF	25	VGL	10
C8	1uF	25	VSL	5
C9	1uF	6	VCOM	5
C10	10uF	6	VCI [Booster]	NA
C11	4.7uF	50	PREVGL [Booster]	NA
C12	1uF	50	PREVGH [Booster]	NA
C71	1uF	6	VCI [LM75A]	NA
L1	10uH			
Q1	NMOS [Vishay: Si1304BDL]		GDR, RESE	5
D1	Diode [OnSemi: MBR0530]		PREVGH	NA
D2	Diode [OnSemi: MBR0530]			NA
D3	Diode [OnSemi: MBR0530]		PREVGL, VSS	NA
R1	0.47 Ohm		RESE	5
R11	2.2kOhm			NA
R12	2.2kOhm			NA
U3	LM75A			NA

The product(s) listed in this datasheet comply with Directive 2002/95/EC of the European Parliament and of the council of 27 January 2004 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People’s Republic of China Electronic Industry Standard SJ/T 11363-2006 “Requirements for concentration limits for certain hazardous substances in electronic information products (电子信息产品中有毒有害物质的限量要求)”. Hazardous Substances test report is available upon request.

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