SSD1608

Advance Information

Active Matrix EPD 240 x 320
Display Driver with Controller

Appendix: IC Revision history of SSD1608 Specification

Revision	Change Items	Effective Date
1.0	Advance Information Release	12-Nov-13
1.1	Updated Section 3 - Ordering information	06-Jan-15

CONTENTS

TABLES

FIGURES

1 GENERAL DESCRIPTION

The SSD1608 is a CMOS active matrix bistable display driver with controller. It consists of 240 source outputs, 320 gate outputs, 1 VCOM and 1 VBD for border that can support a maximum display resolution 240x320 for single chip application. In addition, the SSD1608 has a cascade mode that can support higher display resolution.

The SSD1608 embeds booster, regulators and oscillator. Data/Commands are sent from general MCU through the hardware selectable 6800-/8080-series compatible Parallel Interface or Serial Peripheral Interface.

2 FEATURES

- Design for dot matrix type active matrix EPD display
- Resolution: 240 source outputs; 320 gate outputs; 1 VCOM; 1VBD for border
- Power supply
  - VCI: 2.4 to 3.7V
  - VDDIO: Connect to VCI
  - VDD: 1.8V, regulate from VCI supply

- Gate driving output voltage:
  - 2 levels output (VGH, VGL)
  - Max 42Vp-p
  - VGH: 15V to 22V;
  - VGL: -20V to -15V
  - Voltage adjustment in steps of 500mV.

- Source / VBD driving output voltage:
  - 3 levels output (VSH, VSS, VSL)
  - VSH: 10V to 17V
  - VSL: -10V to -17V
  - Voltage adjustment in steps of 500mV

- VCOM output voltage
  - -4V to -0.2V in 20mV resolution
  - 8 bits Non-volatile memory (OTP) for VCOM adjustment

- Source and gate scan direction control
- Low current deep sleep mode
- On chip display RAM with double display buffer [240x320 / 8 * 2 = 19200Byte]
- Waveform settings can be programmed and stored in On-chip OTP
- Programmable output waveform allowing flexibility for different applications / environments.
- Built in VCOM sensing
- On-chip oscillator.
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage.
- Cascade mode to support higher display resolution.
- I2C Single Master Interface to read external temperature sensor reading
- 8-bits Parallel (6800 & 8080), Serial peripheral interface available
- Available in COG package

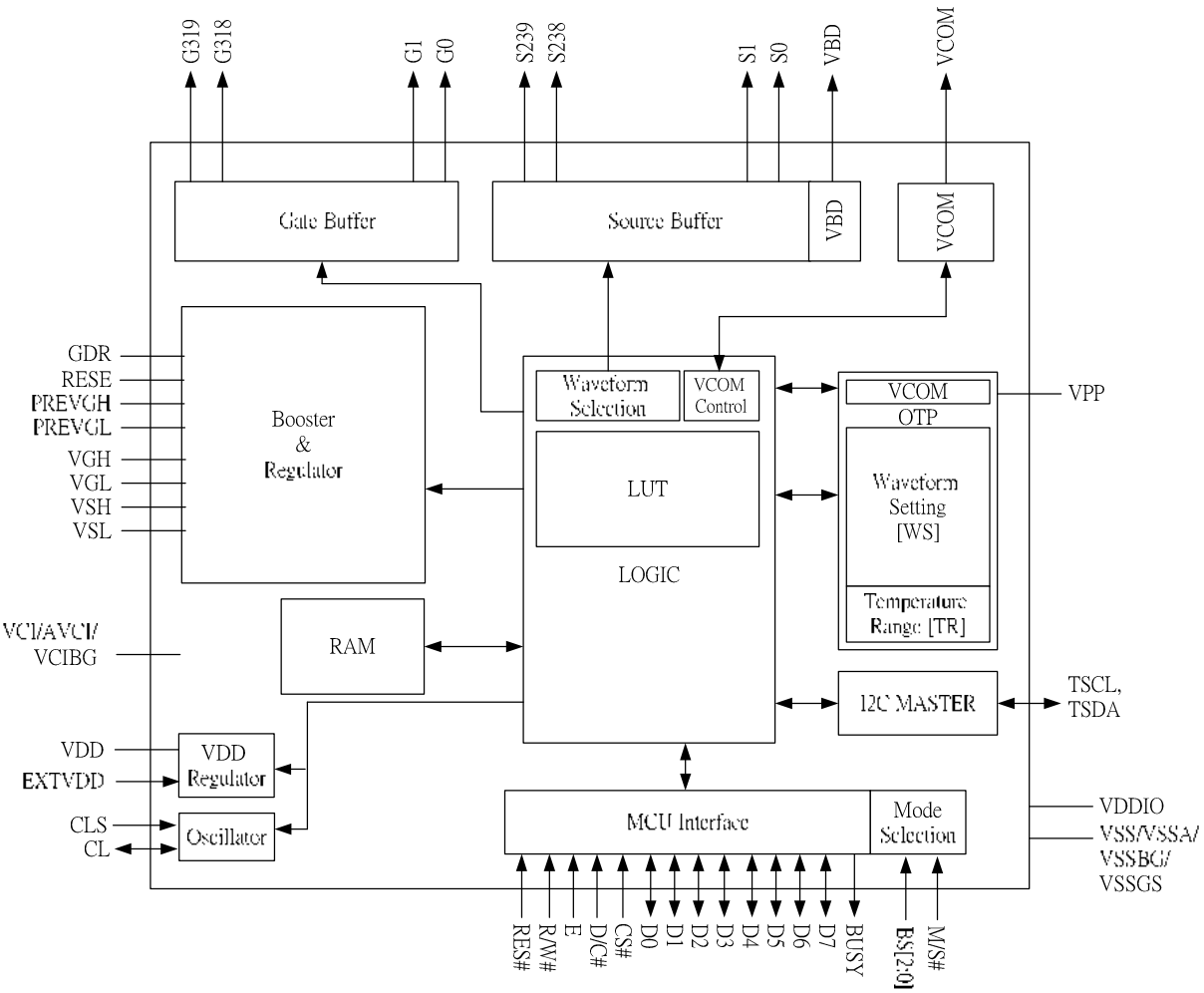
3 ORDERING INFORMATION

Table 3-1 : Ordering Information

Ordering Part Number	Package Form	Remark
SSD1608Z	Gold bump die	Bump Face Up On Waffle pack Die thickness: 300um Bump height: 12um
SSD1608Z8	Gold bump die	Bump Face Down On Waffle pack Die thickness: 300um Bump height: 12um

4 BLOCK DIAGRAM

Figure 4-1 : SSD1608 Block Diagram



5 PIN DESCRIPTION

Key: I = Input, O =Output, IO = Bi-directional (input/output), P = Power pin, C = Capacitor Pin
NC = Not Connected, Pull L =connect to V_{SS}, Pull H = connect to V_{DDIO}

Pin name	Type	Connect to	Function	Description	When not in use
Input power					
VCI	P	Power Supply	Power Supply	Power Supply for the chip	-
VCIA	P	Power Supply	Power Supply	Power input for the chip, Connected with VCI	-
VCIBG	P	Power Supply	Power Supply	Power input for the chip (Reference), Connected with VCI	-
VDDIO	P	Power Supply	Power for interface logic pins	Power Supply for the Interface It should be connected with VCI	-
VDD	P	Capacitor	Regulator output	Core logic power pin VDD can be regulated internally from VCI. - For the single chip application, a capacitor should be connected between VDD and VSS under all circumstances. - For the cascade mode application, a capacitor should be connected between VDD and VSS in the master chip under all circumstances. For the slave chip, the capacitor is not necessary as VDD will be supplied from the cascade master chip externally.	-
EXTVDD	I	VDDIO/VSS	Regulator bypass	This pin is VDD regulator bypass pin. - For the single chip application, EXTVDD should be connected to VSS. - For the cascade mode application, EXTVDD of the master chip should be connected to VSS while EXTVDD of the slave chip should be connected to VDDIO.	-
VSS	P	VSS	GND	Ground (Digital)	-
VSSA	P	VSS	GND	Ground (Analog) It should be connected with VSS.	-
VSSBG	P	VSS	GND	Ground (Reference) Connected with VSS	-
VSSGS	P	VSS	GND	Ground (Output) Connected with VSS	-
VPP	P	Power Supply	OTP power	Power Supply for OTP Programming	Open
Digital I/O					
D [7:0]	I/O	MPU	Data Bus	These pins are bi-directional data bus connecting to the MCU data bus. SPI mode: D0: SCLK D1: SDIN	D[2] : OPEN D[7:3]: VDDIO or VSS
CS#	I	MPU	Logic Control	This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW in parallel interface.	VDDIO or VSS

Pin name	Type	Connect to	Function	Description	When not in use
R/W# (WR#)	I	MPU		This pin is read / write control input pin connecting to the MCU interface. When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin R/W (WR#) can be connected to either VDDIO or VSS.	VDDIO or VSS
D/C#	I	MPU		This pin is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data at D [7:0] will be interpreted as data. When the pin is pulled LOW, the data at D [7:0] will be interpreted as command.	VDDIO or VSS
E (RD#)	I	MPU		This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin E (RD#) should be connected to either VDDIO or VSS	VDDIO or VSS
RES#	I	MPU	System Reset	This pin is reset signal input. Active Low.	-
BUSY	O	MPU	Device Busy Signal	This pin is Busy state output pin When Busy is High, the operation of the chip should not be interrupted, command should not be sent. For example., The chip would put Busy pin High when - Outputting display waveform; or - Programming with OTP - Communicating with digital temperature sensor In the cascade mode, the BUSY pin of the slave chip should be left open.	Open
CLS	I	VDDIO/VSS	Clock Mode Selection	This pin is internal clock enable pin. - For the single chip application, the CLS pin should be connected to VDDIO. - For the cascade mode application, the CLS pin of the master chip should be connected to VDDIO. The CLS pin of the slave chip should be connected to VSS to disable the internal clock as its CL pin should be connected to the CL pin of the master chip.	-
M/S#	I	VDDIO/VSS	Cascade Mode Selection	This pin is Master and Slave selection pin. - For the single chip application, the M/S# pin should be connected to VDDIO. - In the cascade mode: For Master Chip, the M/S# pin should be connected to VDDIO. For Slave Chip, the M/S# pin should be connected to VSS. The oscillator and the booster & regulator circuits of the slave chip will be disabled. The corresponding pins including CL, VDD, VDDIO, PREVGH, PREVGL, VSH, VSL, VGH, VGL and VCOM must be connected to the master chip.	

<table>
<tr><th>Pin name</th><th>Type</th><th>Connect to</th><th>Function</th><th>Description</th><th>When not in use</th></tr>
<tr><td>CL</td><td>I/O</td><td>NC</td><td>Clock signal</td><td>This is the clock signal pin.
When CLS is connected to VDDIO, the internal clock is enabled. The clock signal will be detected at CL. Leave the CL pin open when internal clock is enabled and used.
When CLS is connected to VSS, the internal clock is disabled. An external clock is fed in the CL pin.

In the cascade mode, the CL pin of the slave chip should be connected to the CL pin of the master chip.</td><td></td></tr>
<tr><td>BS [2:0]</td><td>I</td><td>VDDIO/VSS</td><td>MCU Interface Mode Selection</td><td>These pins are for selecting different bus interface.
BS2 should be connected to VSS.
Table 5-1 : MCU interface selection<table><tr><td>BS1</td><td>BS0</td><td>MPU Interface</td></tr><tr><td>L</td><td>L</td><td>4-lines serial peripheral interface (SPI)</td></tr><tr><td>L</td><td>H</td><td>8-bit 8080 parallel interface</td></tr><tr><td>H</td><td>L</td><td>3-lines serial peripheral interface (SPI) – 9 bits SPI</td></tr><tr><td>H</td><td>H</td><td>8-bit 6800 parallel interface</td></tr></table></td><td>-</td></tr>
<tr><td>TSDA</td><td>I/O</td><td>Temperature sensor SDA</td><td>Interface to Digital Temperature Sensor</td><td>This pin is I²C Interface to digital temperature sensor Data pin
External pull up resistor is required when connecting to I²C slave</td><td>Open</td></tr>
<tr><td>TSCL</td><td>O</td><td>Temperature sensor SCL</td><td>Interface to Digital Temperature Sensor</td><td>This pin is I²C Interface to digital temperature sensor Clock pin
External pull up resistor is required when connecting to I²C slave</td><td>Open</td></tr>
<tr><td colspan="6">Analog Pin</td></tr>
<tr><td>GDR</td><td>O</td><td>POWER MOSFET Driver Control</td><td>PREVGH & PREVGL Generation</td><td>This pin is N-Channel MOSFET Gate Drive Control.

In the cascade mode, the GDR pin of the slave chip should be left open.</td><td>-</td></tr>
<tr><td>RESE</td><td>I</td><td>Booster Control Input</td><td></td><td>This pin is the Current Sense Input for the Control Loop

In the cascade mode, the RESE pin of the slave chip should be left open.</td><td>-</td></tr>
<tr><td>FB</td><td>I</td><td>NC</td><td></td><td>Keep open.</td><td>Open</td></tr>
<tr><td>PREVGH</td><td>C</td><td>Stabilizing capacitor</td><td></td><td>This pin is the Power Supply pin for VGH and VSH.
A stabilizing capacitor should be connected between PREVGH and VSS.</td><td>-</td></tr>
<tr><td>PREVGL</td><td>C</td><td>Stabilizing capacitor</td><td></td><td>This pin is the Power Supply pin for VCOM, VGL and VSL.
A stabilizing capacitor should be connected between PREVGL and VSS.</td><td>-</td></tr>
<tr><td colspan="6"></td></tr>
<tr><td>VGH</td><td>C</td><td>Stabilizing capacitor</td><td>VGH, VGL Generation</td><td>Positive Gate driving voltage.
A stabilizing capacitor should be connected between VGH and VSS.</td><td>-</td></tr>
<tr><td>VGL</td><td>C</td><td>Stabilizing capacitor</td><td>VGL Generation</td><td>This pin is Negative Gate driving voltage.
A stabilizing capacitor should be connected between VGL and VSS.</td><td>-</td></tr>
</table>

Pin name	Type	Connect to	Function	Description	When not in use
VSH	C	Stabilizing capacitor	VSH, VSL Generation	This pin is Positive Source driving voltage. A stabilizing capacitor should be connected between VSH and VSS.	-
VSL	C	Stabilizing capacitor		This pin is Negative Source driving voltage. A stabilizing capacitor should be connected between VSL and VSS.	-
VCOM	C	Panel/ Stabilizing capacitor	VCOM	This pin is VCOM driving voltage A stabilizing capacitor should be connected between VCOM and VSS.	-
Panel Driving					
S [239:0]	O	Panel	Source driving signal	Source output pin	Open
G [319:0]	O	Panel	Gate driving signal	Gate output pin	Open
VBD	O	Panel	Border driving signal	Border output pin	Open
Others					
NC	NC	NC	Not Connected	Keep open. Don't connect with other NC pins	Open
TPA	NC	NC	Reserved for Testing	Keep open. Don't connect to NC pin or other test pins including TPA, TPB, TPC, TPD and TPE.	Open
TPB	NC	NC	Reserved for Testing	Keep open. Don't connect to NC pin or other test pins including TPA, TPB, TPC, TPD and TPE.	Open
TPC	NC	NC	Reserved for Testing	Keep open. Don't connect to NC pin or other test pins including TPA, TPB, TPC, TPD and TPE.	Open
TPD	NC	NC	Reserved for Testing	Keep open. Don't connect to NC pin or other test pins including TPA, TPB, TPC, TPD and TPE.	Open
TIN	I	NC	Reserved for Testing	Connect to TPE pin.	
TPE	O	NC	Reserved for Testing	Connect to TIN pin.	

6 FUNCTIONAL BLOCK DESCRIPTION

The device can drive an active matrix TFT EPD panel. It composes of 240 source outputs, 320 gate outputs, 1 VBD and 1 VCOM. It contains flexible built-in waveforms to drive the EPD panel.

6.1 MCU Interface

6.1.1 MCU Interface selection

The SSD1608 can support 6800-series/8080-series parallel interface and 3-wire/4-wire serial peripheral Interface. In the SSD1608, the MCU interface is pin selectable by BS0 and BS1 pins shown in Table 6-1.

Table 6-1 : MCU interface selection by BS0 and BS1

BS1	BS0	MPU Interface
L	L	4-lines serial peripheral interface (SPI)
L	H	8-bit 8080 parallel interface
H	L	3-lines serial peripheral interface (SPI) – 9 bits SPI
H	H	8-bit 6800 parallel interface

The MCU interface consists of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 6-2.

Table 6-2 : MCU interface assignment under different bus interface mode

Pin Name	Data/Command Interface								Control Signal				
Bus Interface	D7	D6	D5	D4	D3	D2	D1	D0	E (RD#)	R/W# (WR#)	CS#	D/C#	RES#
SPI4	L					NC	SDin	SCLK	L	L	CS#	D/C#	RES#
8-bit 8080	D [7:0]								RD#	WR#	CS#	D/C#	RES#
SPI3	L					NC	SDin	SCLK	L	L	CS#	L	RES#
8-bit 6800	D [7:0]								E	R/W#	CS#	D/C#	RES#

Note
(1) L is connected to V_{SS}
(2) H is connected to V_{DDIO}

6.1.2 MCU 6800-series Parallel Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.
A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

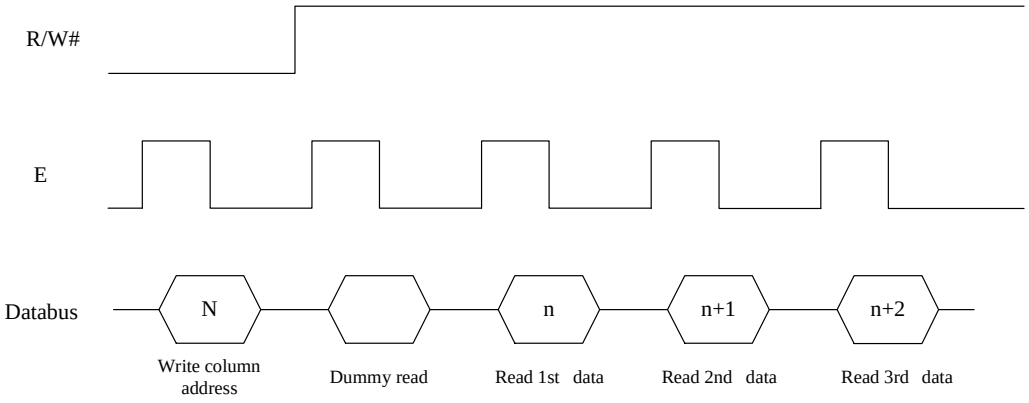
Table 6-3 : Control pins of 6800 interface

Function	E	R/W#	CS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note: ↓ stands for falling edge of signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 6-1.

Figure 6-1 : Data read back procedure - insertion of dummy read



6.1.3 MCU 8080-series Parallel Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 6-2 : Example of Write procedure in 8080 parallel interface mode

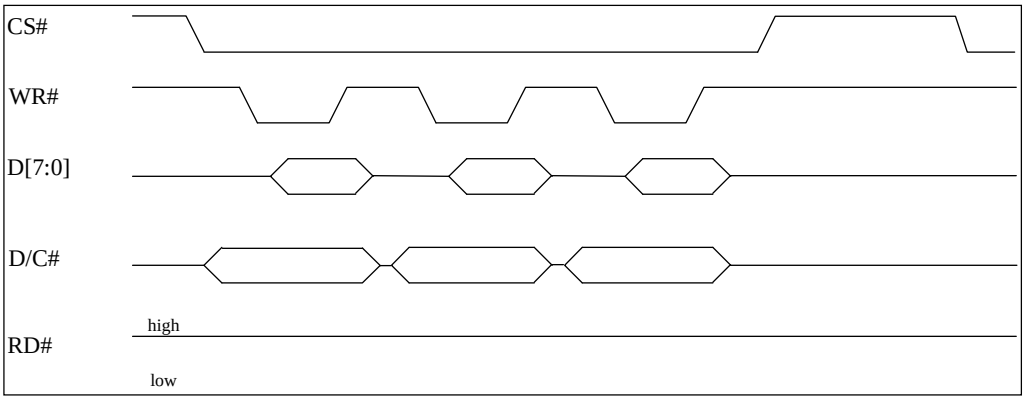


Figure 6-3 : Example of Read procedure in 8080 parallel interface mode

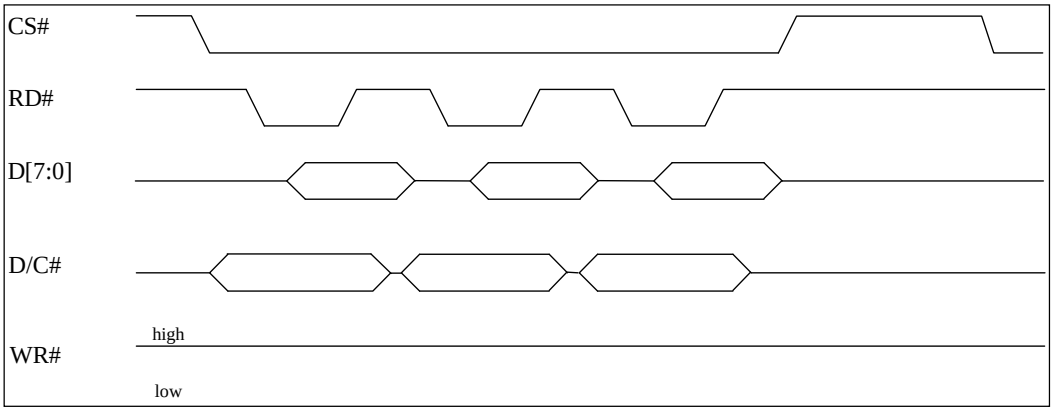


Table 6-4 : Control pins of 8080 interface (Form 1)

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
(1) ↑ stands for rising edge of signal
(2) Refer to Figure 12-2 for Form 1 8080-Series MPU Parallel Interface Timing Characteristics

Alternatively, RD# and WR# can be keep stable while CS# serves as the data/command latch signal.

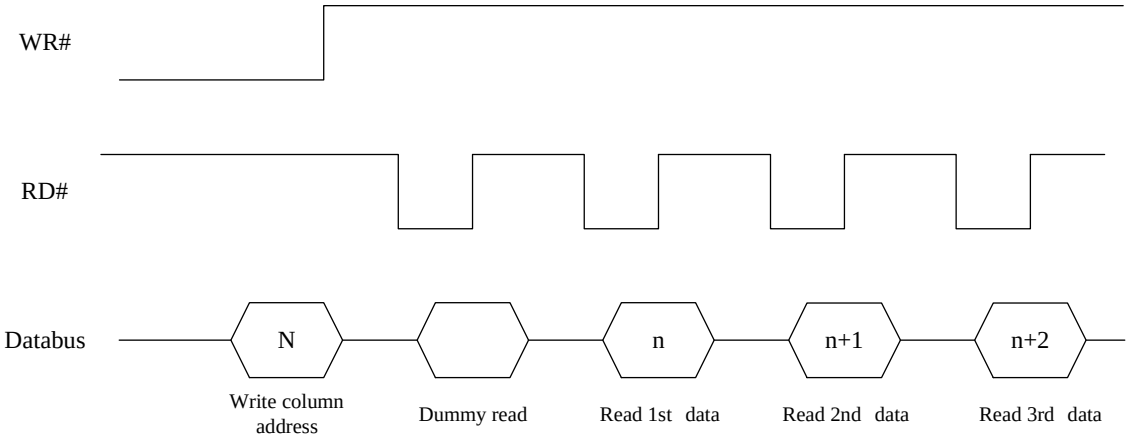
Table 6-5 : Control pins of 8080 interface (Form 2)

Function	RD#	WR#	CS#	D/C#
Write command	H	L	↑	L
Read status	L	H	↑	L
Write data	H	L	↑	H
Read data	L	H	↑	H

Note
(1) ↑ stands for rising edge of signal
(2) Refer to Figure 12-3 for Form 2 8080-Series MPU Parallel Interface Timing Characteristics

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 6-4.

Figure 6-4 : Display data read back procedure - insertion of dummy read



6.1.4 MCU Serial Peripheral Interface (4-wire SPI)

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, E and R/W# can be connected to an external ground.

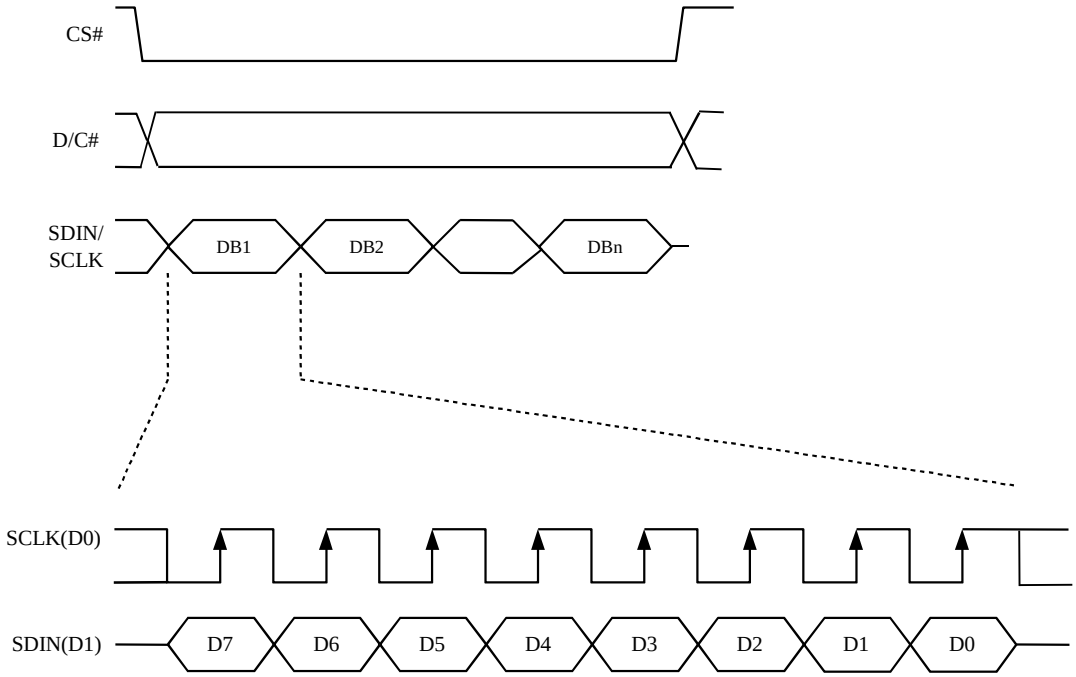
Table 6-6 : Control pins of 4-wire Serial Peripheral interface

Function	E(RD#)	R/W#(WR#)	CS#	D/C#	SCLK
Write command	Tie LOW	Tie LOW	L	L	↑
Write data	Tie LOW	Tie LOW	L	H	↑

Note: ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register in the order of D7, D6, ... D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.

Figure 6-5 : Write procedure in 4-wire Serial Peripheral Interface mode



6.1.5 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.
In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, R/W# (WR#)#, E and D/C# can be connected to an external ground.

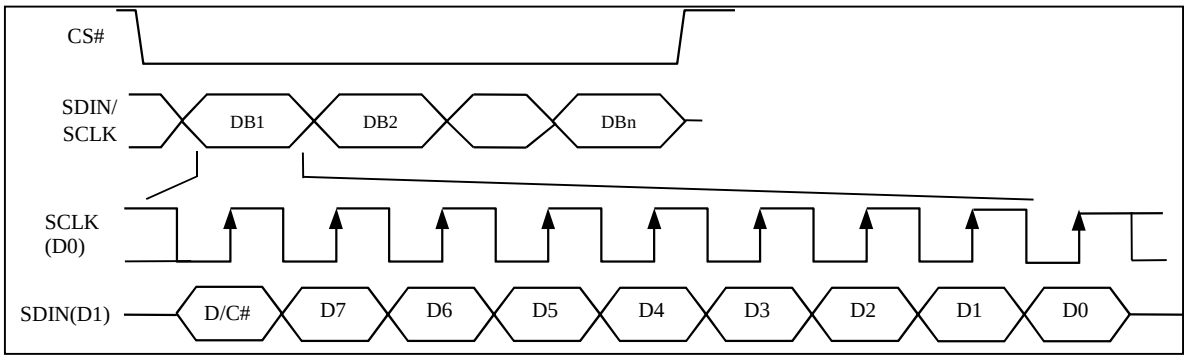
The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

Table 6-7 : Control pins of 3-wire Serial Peripheral interface

Function	E(RD#)	R/W#(WR#)	CS#	D/C#	SCLK
Write command	Tie LOW	Tie LOW	L	Tie LOW	↑
Write data	Tie LOW	Tie LOW	L	Tie LOW	↑

Note: ↑ stands for rising edge of signal

Figure 6-6 : Write procedure in 3-wire Serial Peripheral Interface mode



6.2 RAM

The On chip display RAM is holding the image data. 1 set of RAM is built for historical data and the other set is built for the current image data. The size of each RAM is 240x320 bits.

Table 6-8 shows the RAM map under the following condition:

- Command “Data Entry Mode” R11h is set to:

Address Counter update in X direction	AM=0
X: Increment Y: Increment	ID[1:0] =11

- Command “Driver Output Control” R01h is set to

320 Mux	MUX = 13Fh
Select G0 as 1st gate	GD = 0
Left and Right gate Interlaced	SM = 0
Scan From G0 to G319	TB = 0

- Command “Gate Start Position” R0Fh is set to:

Set the Start Position of Gate = G0	SCN=0

- Data byte sequence: DB0, DB1, DB2 … DB9599

Table 6-8 : RAM address map

		S0	S1	S2	S3	S4	S5	S6	S7	…	…	S232	S233	S234	S235	S236	S237	S238	S239	Source X-ADDR
		00h								…		1Dh								
G0	00h	DB0 [7]	DB0 [6]	DB0 [5]	DB0 [4]	DB0 [3]	DB0 [2]	DB0 [1]	DB0 [0]	…	…	DB29 [7]	DB29 [6]	DB29 [5]	DB29 [4]	DB29 [3]	DB29 [2]	DB29 [1]	DB29 [0]	
G1	01h	DB30 [7]	DB30 [6]	DB30 [5]	DB30 [4]	DB30 [3]	DB30 [2]	DB30 [1]	DB30 [0]	…	…	DB59 [7]	DB59 [6]	DB59 [5]	DB59 [4]	DB59 [3]	DB59 [2]	DB59 [1]	DB59 [0]	
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	
G318	13Eh	DB9540 [7]	DB9540 [6]	DB9540 [5]	DB9540 [4]	DB9540 [3]	DB9540 [2]	DB9540 [1]	DB9540 [0]	…	…	DB9569 [7]	DB9569 [6]	DB9569 [5]	DB9569 [4]	DB9569 [3]	DB9569 [2]	DB9569 [1]	DB9569 [0]	
G319	13Fh	DB9570 [7]	DB9570 [6]	DB9570 [5]	DB9570 [4]	DB9570 [3]	DB9570 [2]	DB9570 [1]	DB9570 [0]	…	…	DB9599 [7]	DB9599 [6]	DB9599 [5]	DB9599 [4]	DB9599 [3]	DB9599 [2]	DB9599 [1]	DB9599 [0]	
GATE	Y-ADDR																			

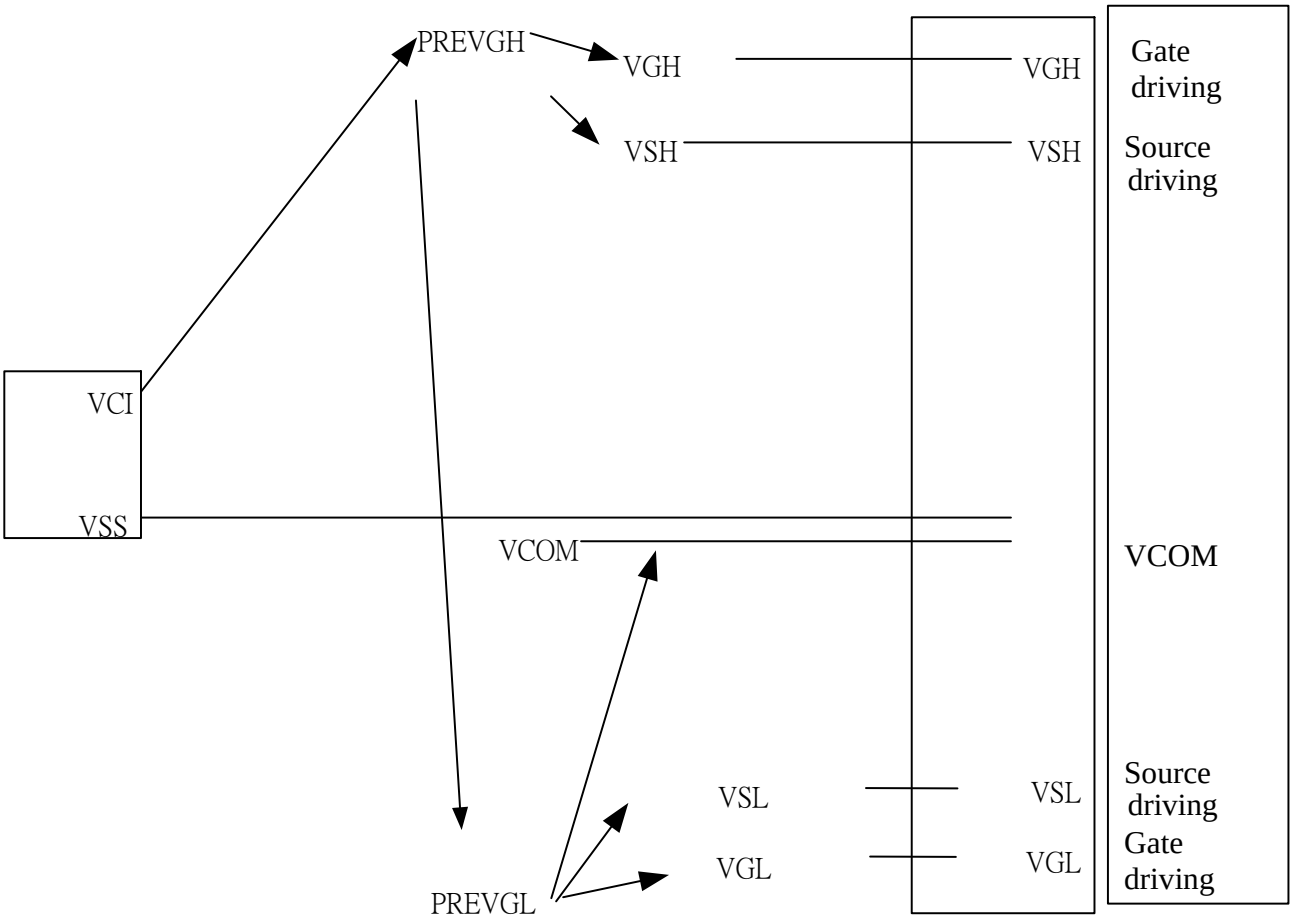
6.3 Oscillator

The on-chip oscillator is included for the use on waveform timing and Booster operations. In order to enable the internal oscillator, the CLS pin must be connected to VDDIO.

6.4 Booster & Regulator

A voltage generation system is included in the SSD1608. It provides all necessary driving voltages required for an AMEPD panel including VGH, VGL, VSH, VSL and VCOM. Figure 6-7 shows the relation of the voltages. External application circuit is needed to make the on-chip booster & regulator circuit work properly.

Figure 6-7 : Input and output voltage relation chart



- Max voltage difference between VGH and VGL is 42V.

6.5 Panel Driving Waveform

The Vpixel is defined as Figure 6-8, and its relations with GATE, SOURCE are shown in Figure 6-9.

Figure 6-8 : Vpixel Definition

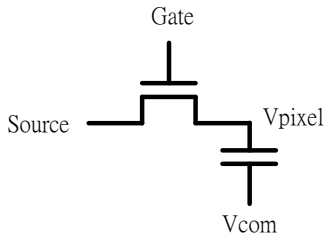
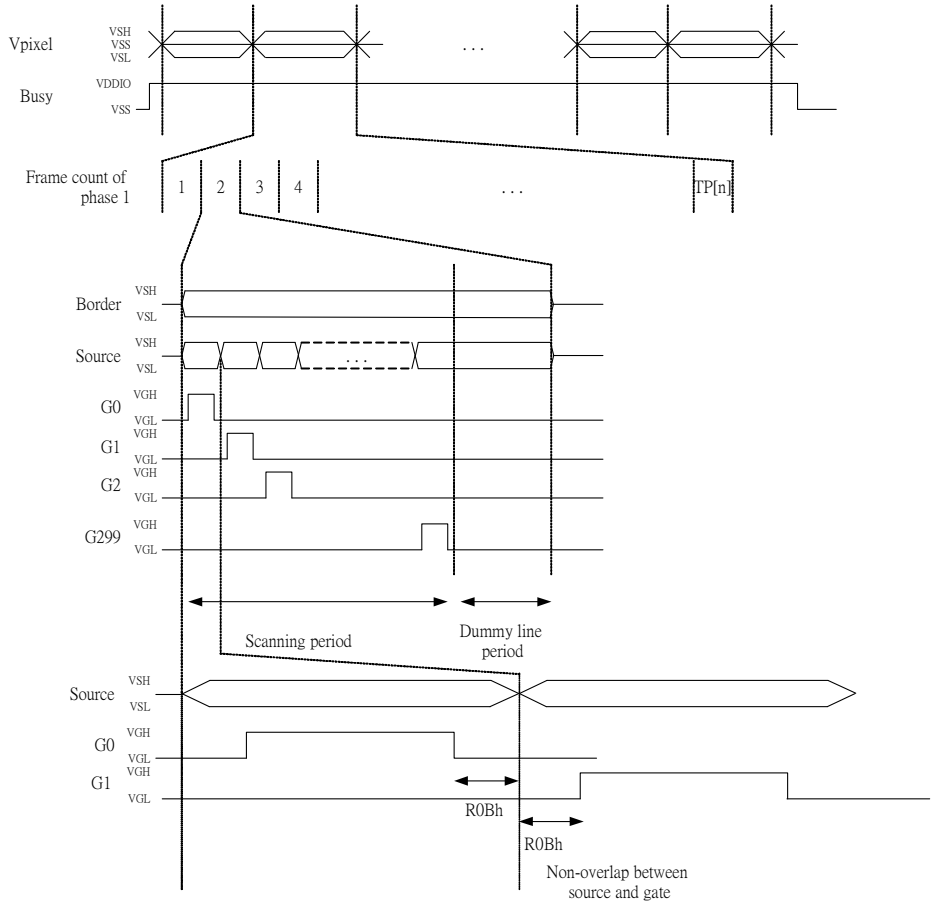


Figure 6-9 : The Relation of Vpixel Waveform with Gate and Source

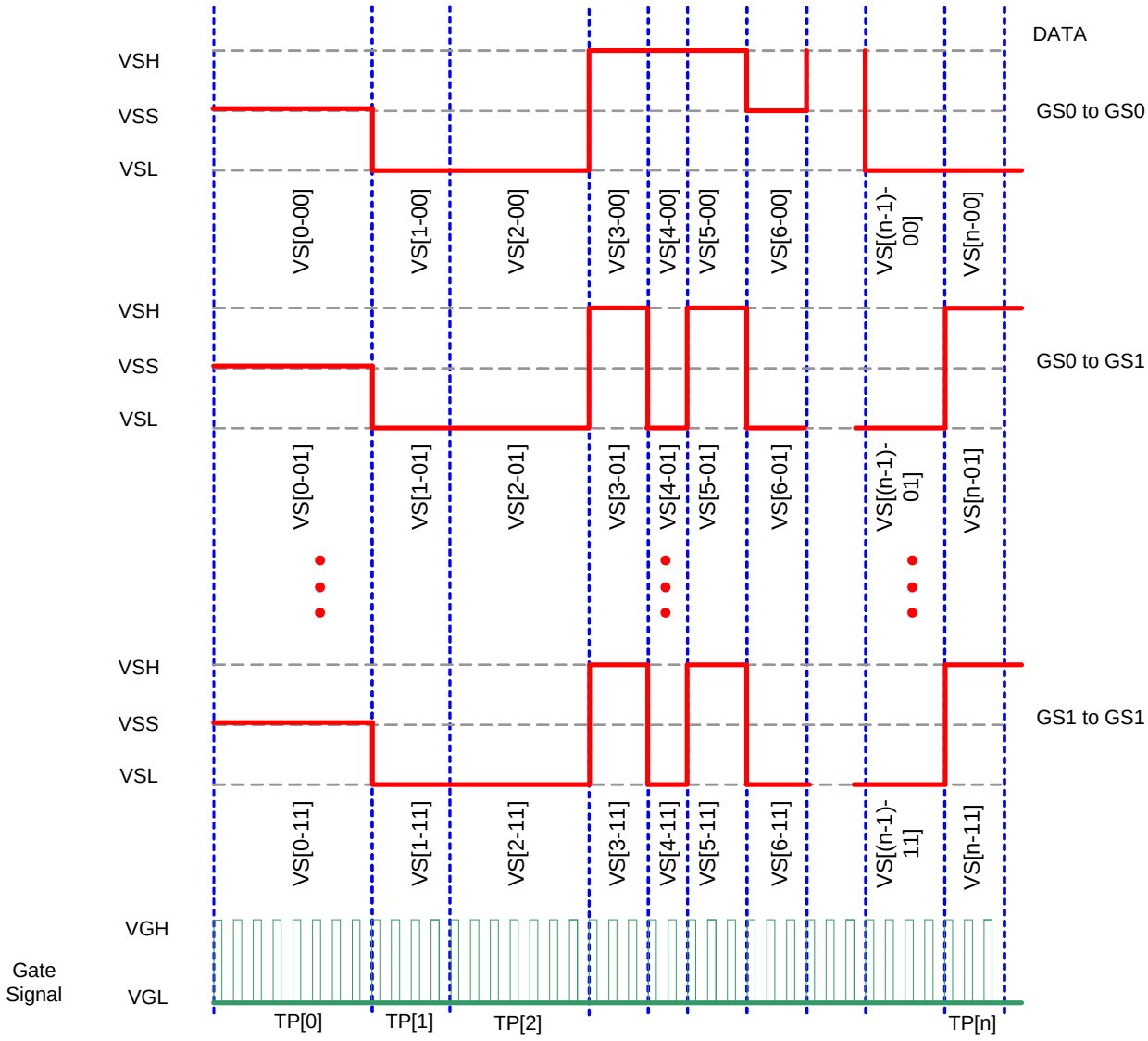


6.6 VCOM Sensing

This functional block provides the scheme to select the optimal VCOM DC level and programmed the setting into OTP.

6.7 Gate and Programmable Source waveform

Figure 6-10 : Programmable Source and Gate waveform illustration



- There are totally 20 phases for programmable Source waveform of different phase length.
- The phase period defined as TP [n] * T_{FRAME}, where TP [n] range from 0 to 15.
- TP [n] = 0 indicates phase skipped
- Source Voltage Level: VS [n-XY] is constant in each phase
- VS [n-XY] indicates the voltage in phase n for transition from GS X to GS Y
  - 00 – VSS
  - 01 – VSH
  - 10 – VSL
  - 11 – NA
- VS [n-XY] and TP[n] are stored in waveform lookup table register [LUT].

6.8 Waveform Look Up Table (LUT)

LUT contains 256 bits, which defines the display driving waveform settings. They are arranged in format shown in Figure 6-11.

Figure 6-11 : VS[n-XY] and TP[n] mapping in LUT

in Decimal	D7	D6	D5	D4	D3	D2	D1	D0
0	VS[0-11]		VS[0-10]		VS[0-01]		VS[0-00]	
1	VS[1-11]		VS[1-10]		VS[1-01]		VS[1-00]	
2	VS[2-11]		VS[2-10]		VS[2-01]		VS[2-00]	
3	VS[3-11]		VS[3-10]		VS[3-01]		VS[3-00]	
4	VS[4-11]		VS[4-10]		VS[4-01]		VS[4-00]	
5	VS[5-11]		VS[5-10]		VS[5-01]		VS[5-00]	
6	VS[6-11]		VS[6-10]		VS[6-01]		VS[6-00]	
7	VS[7-11]		VS[7-10]		VS[7-01]		VS[7-00]	
…	…		…		…		…	
16	VS[16-11]		VS[16-10]		VS[16-01]		VS[16-00]	
17	VS[17-11]		VS[17-10]		VS[17-01]		VS[17-00]	
18	VS[18-11]		VS[18-10]		VS[18-01]		VS[18-00]	
19	VS[19-11]		VS[19-10]		VS[19-01]		VS[19-00]	
20	TP[1]				TP[0]			
21	TP[3]				TP[2]			
…	…				…			
29	TP[19]				TP[18]			
30					VSH/VSL			
31								

6.9 OTP

The OTP is the non-volatile memory and is used to store the information of OTP Selection Option, VCOM value, 7 sets of WAVEFORM SETTING (WS) [256bits x 7] and 6 sets of TEMPERATURE RANGE (TR) [24bits x 6].

The OTP is the non-volatile memory and stored the information of:

- OTP Selection Option
- VCOM value
- Source value
- 7 set of WAVEFORM SETTING (WS) [256bits x 7]
- 6set of TEMPERATURE RANGE (TR) [24bits x 6]

For Programming the WS and TR, Write RAM is required, and the configurations should be

Command: Data Entry mode	C11, D03	Set Address automatic increment setting = X increment and Y increment Set Address counter update in X direction
Command: X RAM address start /end	C44, D00, D1D	Set RAM Address for S0 to S239
Command: Y RAM address start /end	C45, D00, D13F	Set RAM Address for G0 to G319
Command: RAM X address counter	C4E, D00	Set RAM X AC as 0
Command: RAM Y address counter	C4F, D000	Set RAM Y AC as 0

The mapping table of OTP is shown in below figure,

Figure 6-12 : OTP Content and Address Mapping

Default OTP ADDRESS	SPARE OTP ADDRESS	WRITE RAM ADDRESS X	WRITE RAM ADDRESS Y	D7	D6	D5	D4	D3	D2	D1	D0
0	256	0	0	VS[0-11]		VS[0-10]		VS[0-01]		VS[0-00]	
1	257	1	0	VS[1-11]		VS[1-10]		VS[1-01]		VS[1-00]	
2	258	2	0	VS[2-11]		VS[2-10]		VS[2-01]		VS[2-00]	
3	259	3	0	VS[3-11]		VS[3-10]		VS[3-01]		VS[3-00]	
4	260	4	0	VS[4-11]		VS[4-10]		VS[4-01]		VS[4-00]	
				…		…		…		…	
18	274	18	0	VS[18-11]		VS[18-10]		VS[18-01]		VS[18-00]	
19	275	19	0	VS[19-11]		VS[19-10]		VS[19-01]		VS[19-00]	
20	276	20	0	TP[1]				TP[0]			
21	277	21	0	TP[3]				TP[2]			
				…				…			
29	285	4	1	TP[19]				TP[18]			
30	286	5	1	Dummy				VSH/VSL			
31	287	6	1	DUMMY							
32	288	7	1	WS[1]							
63	319	13	2								
				…							
192	448	17	7	WS[6]							
223	479	23	8								
224	480	24	8	TEMP[1L][11:0]							
225	481	0	9								
226	482	1	9	TEMP[1-H][11:0]							
227	483	2	9	TEMP[2L][11:0]							
228	484	3	9								
229	485	4	9	TEMP[2-H][11:0]							
				…							
236	492	11	9	TEMP[5L][11:0]							
237	493	12	9								
238	494	13	9	TEMP[5-H][11:0]							
239	495	14	9	TEMP[6L][11:0]							
240	496	15	9								
241	497	16	9	TEMP[6-H][11:0]							

Remark:

- WS [m] means the waveform setting of temperature set m, the configuration are same as the definition in LUT. The corresponding low temperature range of WS[m] defined as TEMP [m-L] and high range defined as TEMP [m-H]
- Load WS [m] from OTP for LUT if Temp [m-L] < Temperature Register <= Temp [m-H]

6.9.1 Temperature Searching Mechanism

Legend:

WS#	Waveform Setting no. #
TR#	Temperature Range no. #
LUT	720 bit register storing the waveform setting (volatile)
Temperature register	12bit Register storing reading from temperature sensor (volatile)
OTP	A non-volatile storing 7 sets of waveform setting and 6 set of temperature range
WS_sel_address	an address pointer indicating the selected WS#

Figure 6-13 : Waveform Setting and Temperature Range # mapping

OTP (non-volatile)

WS0	
WS1	TR1
WS2	TR2
WS3	TR3
WS4	TR4
WS5	TR5
WS6	TR6

IC implementation requirement	
1	Default selection is **WS0**
2	Compare temperature register from **TR1 to TR6**, in sequence. **The last match will be recorded**
	i.e. If the temperature register fall in both TR3 and TR5. WS5 will be selected
3	If none of the range TR1 to TR6 is match, WS0 will be selected.
User application	
1	The default waveform should be programmed as WS0
2	There is no restriction on the sequence of TR1, TR2…. TR6.

6.10 External Temperature Sensor I2C Single Master Interface

The chip provides two I/O lines [TSDA and TSCL] for connecting digital temperature sensor for temperature reading sensing.
TSDA will treat as SDA line and TSCL will treat as SCL line. They are required connecting with external pull-up resistor.

1. If the Temperature value MSByte bit D11 = 0, then
The temperature is positive and value (DegC) = + (Temperature value) / 16
2. If the Temperature value MSByte bit D11 = 1, then
The temperature is negative and value (DegC) = ~ (2's complement of Temperature value) / 16

12-bit binary (2's complement)	Hexadecimal Value	Decimal Value	Value [DegC]
0111 1111 0000	7F0	2032	127
0111 1110 1110	7EE	2030	126.875
0111 1110 0010	7E2	2018	126.125
0111 1101 0000	7D0	2000	125
0001 1001 0000	190	400	25
0000 0000 0010	002	2	0.125
0000 0000 0000	000	0	0
1111 1111 1110	FFE	-2	-0.125
1110 0111 0000	E70	-400	-25
1100 1001 0010	C92	-878	-54.875
1100 1001 0000	C90	-880	-55

6.11 Cascade Mode

The SSD1608 has a cascade mode that can cascade 2 chips to achieve the display resolution up to 480 (sources) x 320 (gates). The pin M/S# is used to configure the chip. When M/S# is connected to VDDIO, the chip is configured as a master chip. When M/S# is connected to VSS, the chip is configured as a slave chip.

When the chip is configured as a master chip, it will be the same as a single chip application, ie, all circuit blocks will be worked as usual. When the chip is configured as a slave chip, its oscillator and booster & regulator circuit will be disabled. The oscillator clock and all booster voltages will be come from the master chip. Therefore, the corresponding pins including CL, VDD, PREVGH, PREVGL, VSH, VSL, VGH, VGL and VCOM must be connected to the master chip.

7 COMMAND TABLE

Table 7-1: Command Table

(D/C#=0, R/W#(WR#) = 0, E(RD#=1) unless specific setting is stated)

Command Table												
R/W#	**D/C#**	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
1	0	-	0	0	0	0	0	A_2	A_1	A_0	Status Read	Read Driver status on • A2: BUSY flag • A1,A0: Chip ID (01 as default)
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting A[8:0]: MUX setting as A[8:0] + 1 POR = 13Fh + 1 MUX B[2]: GD Selects the 1st output Gate GD=0 [POR], G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, … GD=1, G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, … B[1]: SM Change scanning order of gate driver. SM=0 [POR], G0, G1, G2, G3…G319 (left and right gate interlaced) SM=1, G0, G2, G4 …G318, G1, G3, …G319 B[0]: TB TB = 0 [POR], scan from G0 to G319 TB = 1, scan from G319 to G0.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1		0	0	0	0	0	B_2	B_1	B_0		
0	0	02	0	0	0	0	0	0	1	0	Reserve	

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage Control	Set Gate related driving voltage A[7:4]: VGH, 15 to 22V in 0.5V step A[3:0]: VGL, -15 to -20V in 0.5V step VGL default at -20V
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source output voltage magnitude A[3:0]: VSH/VSL 10V to 17V in 0.5V step
0	1		0	0	0	0	A_3	A_2	A_1	A_0		Source setting can be loaded from WS-BYTE31, D[3:0]
0	0	05	0	0	0	0	0	1	0	1	Reserve	
0	0	06	0	0	0	0	0	1	1	0	Reserve	

	VGH	VGL
0000	15	-15
0001	15.5	-15.5
0010	16	-16
0011	16.5	-16.5
0100	17	-17
0101	17.5	-17.5
0110	18	-18
0111	18.5	-18.5
1000	19	-19
1001	19.5	-19.5
1010	20	-20 [POR]
1011	20.5	NA
1100	21	NA
1101	21.5	NA
1110	22 [POR]	NA
1111	NA	NA

	VSH/VSL
0000	10
0001	10.5
0010	11
0011	11.5
0100	12
0101	12.5
0110	13
0111	13.5
1000	14
1001	14.5
1010	15.0 [POR]
1011	15.5
1100	16
1101	16.5
1110	17
1111	N/A

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	07	0	0	0	0	0	1	1	1	Display Control	Display control setting A[5] A[4] Description 1 1 All Gate output voltage level as VGH 0 1 All Gate output voltage level as VGL 1 0 Selected gate output as VGL, non-selected gate output as VGH 0 0 Selected gate output as VGH, non-selected gate output as VGL [POR]
0	1		0	0	A_5	A_4	0	0	0	0		
0	0	08	0	0	0	0	1	0	0	0	Reserve	
0	0	09	0	0	0	0	1	0	0	1	Reserve	
0	0	0A	0	0	0	0	1	0	1	0	Reserve	
0	0	0B	0	0	0	0	1	0	1	1	Gate and Source non overlap period Control	Set Delay of gate and source non overlap period: - Gate falling edge to source output change - Source change to Gate rising edge Delay Duration in terms of Oscillator clock [1/F_{OSC}] A [3:0] Delay Duration 0000 NA 0001 NA 0010 4 … 0101 10 [POR] … 1110 28 1111 NA
0	1		0	0	0	0	A_3	A_2	A_1	A_0		

Command Table												
R/W#	**D/C#**	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start Control	Booster Enable with Phase 1, Phase 2 and Phase 3 for soft start current setting. A[7:0] = CFh [POR] B[7:0] = CEh [POR] C[7:0] = 8Dh [POR]
0	1		1	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Phase1 Setting	
0	1		1	B_6	B_5	B_4	B_3	B_2	B_1	B_0	Phase2 Setting	
0	1		1	C_6	C_5	C_4	C_3	C_2	C_1	C_0	Phase3 Setting	
0	0	0D	0	0	0	0	1	1	0	1	Reserve	
0	0	0E	0	0	0	0	1	1	1	0	Reserve	
0	0	0F	0	0	0	0	1	1	1	1	Gate scan start position	Set the scanning start position of the gate driver. The valid range is from 0 to 319. When TB=0: SCN [8:0] = A[8:0] A[8:0] = 000h [POR] When TB=1: SCN [8:0] = 319 - A[8:0] A[8:0] = 000h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control A[0] : Description 0 Normal Mode [POR] 1 Enter Deep Sleep Mode
0	1		0	0	0	0	0	0	0	A_0		
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	A_2	A_1	A_0		
0	0	12	0	0	0	1	0	0	1	0	SWRESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode Note: RAM are unaffected by this command.
0	0	13	0	0	0	1	0	0	1	1	Reserve	
0	0	14	0	0	0	1	0	1	0	0	Reserve	
0	0	15	0	0	0	1	0	1	0	1	Reserve	
0	0	16	0	0	0	1	0	1	1	0	Reserve	
0	0	17	0	0	0	1	0	1	1	1	Reserve	
0	0	18	0	0	0	1	1	0	0	0	Reserve	
0	0	19	0	0	0	1	1	0	0	1	Reserve	
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[7:0] – MSByte 01111111[POR] B[7:0] – LSByte 11110000[POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	0	0	0	0		
0	0	1B	0	0	0	1	1	1	0	1	Temperature Sensor Control (Read from temperature register)	Read from temperature register. X[7:0] – MSByte Y[7:4] – LSByte
1	1		X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0		
1	1		Y_7	Y_6	Y_5	Y_4	0	0	0	0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	1C	0	0	0	1	1	1	0	0	Temperature Sensor Control (Write Command to temperature sensor)	Write Command to temperature sensor A[7:6] – Select no of byte to be sent 00 – Address + pointer 01 – Address + pointer + 1st parameter 10 – Address + pointer + 1st parameter + 2nd pointer 11 – Address A[5:0] – Pointer Setting B[7:0] – 1st parameter C[7:0] – 2nd parameter The command required CLKEN=1.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	0	1D	0	0	0	1	1	1	0	1	Temperature Sensor Control (Load temperature register with temperature sensor reading)	Load temperature register with temperature sensor reading BUSY=H for whole loading period The command required CLKEN=1.
0	0	1E	0	0	0	1	1	1	1	0	Reserve	
0	0	1F	0	0	0	1	1	1	1	1	Reserve	
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h User should not interrupt this operation to avoid corruption of panel images.
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	Option for Display Update Bypass Option used for Pattern Display, which is used for display the RAM content into the Display OLD RAM Bypass option A [7] A[7] = 1: Enable bypass A[7] = 0: Disable bypass [POR] A[4] value will be used as for bypass. A[4] = 0 [POR] A[1:0] Initial Update Option - Source Control
0	1		A_7	0	0	A_4	A_3	A_2	A_1	A_0		

A[1:0]	GSC	GSD
00	GS0	GS0
01 [POR]	GS0	GS1
10	GS1	GS0
11	GS1	GS1

Command Table

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>22</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td rowspan="2">Display Update Control 2</td><td rowspan="2">Display Update Sequence Option:
Enable the stage for Master Activation

<table><tr><th></th><th>Parameter (in Hex)</th></tr><tr><td>Enable Clock Signal,
Then Enable CP
Then Load Temperature value
Then Load LUT
Then INIITIAL DISPLAY
Then PATTERN DISPLAY
Then Disable CP
Then Disable OSC</td><td>FF
[POR]</td></tr><tr><td>Enable Clock Signal,
Then Enable CP
Then Load Temperature value
Then Load LUT
Then PATTERN DISPLAY
Then Disable CP
Then Disable OSC</td><td>F7</td></tr><tr><td>To Enable Clock Signal
(CLKEN=1)</td><td>80</td></tr><tr><td>To Enable Clock Signal,
then Enable CP
(CLKEN=1, CPEN=1)</td><td>C0</td></tr><tr><td>To INITIAL DISPLAY + PATTEN DISPLAY</td><td>0C</td></tr><tr><td>To INITIAL DISPLAY</td><td>08</td></tr><tr><td>To DISPLAY PATTEN</td><td>04</td></tr><tr><td>To Disable CP,
then Disable Clock Signal
(CLKEN=1, CPEN=1)</td><td>03</td></tr><tr><td>To Disable Clock Signal
(CLKEN=1)</td><td>01</td></tr></table>
Remark:
CLKEN=1:
If CLS=VDDIO then Enable OSC
If CLS=VSS then Enable External Clock
CLKEN=0:
If CLS=VDDIO then Disable OSC
AND
INTERNAL CLOCK Signal = VSS,</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>0</td><td>23</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Reserve</td><td></td></tr>
<tr><td>0</td><td>0</td><td>24</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Write RAM</td><td>After this command, data entries will be written into the RAM until another command is written. Address pointers will advance accordingly.</td></tr>
<tr><td>0</td><td>0</td><td>25</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>Read RAM</td><td>After this command, data read on the MCU bus will fetch data from RAM, until another command is written. Address pointers will advance accordingly.</td></tr>
<tr><td>0</td><td>0</td><td>26</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Reserve</td><td></td></tr>
<tr><td>0</td><td>0</td><td>27</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>Reserve</td><td></td></tr>
</table>

Command Table												
R/W#	**D/C#**	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	0	28	0	0	1	0	1	0	0	0	VCOM Sense	Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value. The sensed VCOM voltage is stored in register The command required CLKEN=1.
0	0	29	0	0	1	0	1	0	0	1	VCOM Sense Duration	Stabling time between entering VCOM sensing mode and reading acquired. VCOM sense duration = Setting + 1 Seconds 0x09(10Seconds) [POR]
0	1		0	0	0	0	A_3	A_2	A_1	A_0		
0	0	2A	0	0	1	0	1	0	1	0	Program VCOM OTP	Program VCOM register into OTP
0	0	2B	0	0	1	0	1	0	1	1	Reserve	
0	0	2C	0	0	1	0	1	0	1	1	Write VCOM register	Write VCOM register from MCU interface
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	2D	0	0	1	0	1	1	0	1	Read OTP Registers	Read register reading to MCU A [7:0] Spare OTP Option B [7:0] VCOM Register
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	0	2E	0	0	1	0	1	1	1	0	Reserve	
0	0	2F	0	0	1	0	1	1	1	1	Reserve	
0	0	30	0	0	1	1	0	0	0	0	Program WS OTP	Program OTP of Waveform Setting The contents should be written into RAM before sending this command.
0	0	31	0	0	1	1	0	0	0	1	Reserve	
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU [240 bits], (excluding the VSH/VSL and Dummy bit)
0 0 0 … 0 0	1 1 1 … 1 1		LUT [30 bytes]									
0	0	33	0	0	1	1	0	0	1	1	Read LUT register	Read from LUT register [240 bits] (excluding the VSH/VSL and Dummy bit)
1 1 1 … 1 1	1 1 1 … 1 1		LUT [30 bytes]									

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	34	0	0	1	1	0	1	0	0	Reserve	
0	0	35	0	0	1	1	0	1	0	1	Reserve	
0	0	36	0	0	1	1	0	1	1	0	Program OTP selection	Program OTP Selection according to the OTP Selection Control [R37h]
0	0	37	0	0	1	1	0	1	1	1	OTP selection Control	Write the OTP Selection: A[7]=1 spare VCOM OTP A[6] VCOM_Status A[5]=1 spare WS OTP A[4] WS_Status A[3:0] are reserved OTP bit. User can treat the bits as Version Control.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	38	0	0	1	1	1	0	0	0	Reserve	
0	0	39	0	0	1	1	1	0	0	1	Reserve	
0	0	3A	0	0	1	1	1	0	1	0	Set dummy line period	Set number of dummy line period A[6:0]: Number of dummy line period in term of TGate A[6:0] = 02h [POR] Available setting 0 to 127.
0	1		0	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	3B	0	0	1	1	1	0	1	1	Set Gate line width	Set Gate line width (TGate) A[3:0] Line width in us A[3:0] TGate 0000 30 0001 34 0010 38 0011 40 0100 44 0101 46 0110 52 0111 56 1000 62 [POR] 1001 68 1010 78 1011 88 1100 104 1101 125 1110 156 1111 208 Remark: Default value will give 50Hz Frame frequency under 22 dummy line pulse setting.
0	1		0	0	0	0	A_3	A_2	A_1	A_0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A [7] Follow Source at Initial Update Display A [7]=0: [POR] A [7]=1: Follow Source at Initial Update Display for VBD, A [6:0] setting are being overridden at Initial Display STAGE. A [6] Select GS Transition/ Fix Level for VBD A [6]=0: Select GS Transition A[3:0] for VBD A [6]=1: Select FIX level Setting A[5:4] for VBD [POR] A [5:4] Fix Level Setting for VBD A[5:4] / VBD level: 00 / VSS; 01 / VSH; 10 / VSL; 11[POR] / HiZ A [1:0] GS transition setting for VBD (Select waveform like data A[3:2] to data A[1:0]) A[1:0] / GSA / GSB: 00 / GS0 / GS0; 01 [POR] / GS0 / GS1; 10 / GS1 / GS0; 11 / GS1 / GS1
0	1		A_7	A_6	A_5	A_4	0	0	A_1	A_0		
0	0	3D	0	0	1	1	1	1	0	1	Reserve	
0	0	3E	0	0	1	1	1	1	1	0	Reserve	
0	0	3F	0	0	1	1	1	1	1	1	Reserve	
0	0	40	0	1	0	0	0	0	0	0	Reserve	
0	0	41	0	1	0	0	0	0	0	1	Reserve	
0	0	42	0	1	0	0	0	0	1	0	Reserve	
0	0	43	0	1	0	0	0	0	1	1	Reserve	
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit A[4:0]: XSA[4:0], XStart, POR = 00h B[4:0]: XEA[4:0], XEnd, POR = 1Dh
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	B_4	B_3	B_2	B_1	B_0		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit A[8:0]: YSA[8:0], YStart, POR = 000h B[8:0]: YEA[8:0], YEnd, POR = 13Fh
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		0	0	0	0	0	0	0	B_8		
0	0	46	0	1	0	0	0	1	1	0	Reserve	
0	0	47	0	1	0	0	0	1	1	1	Reserve	
0	0	48	0	1	0	0	1	0	0	0	Reserve	

Command Table												
R/W#	**D/C#**	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	0	49	0	1	0	0	1	0	0	1	Reserve	
0	0	4A	0	1	0	0	1	0	1	0	Reserve	
0	0	4B	0	1	0	0	1	0	1	1	Reserve	
0	0	4C	0	1	0	0	1	1	0	0	Reserve	
0	0	4D	0	1	0	0	1	1	0	1	Reserve	
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[4:0]: XAD[4:0], POR is 00h
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: YAD8:0], POR is 000h
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1	FF	1	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read Commands.

8 Command DESCRIPTION

8.1 Driver Output Control (01h)

This double byte command has multiple configurations and each bit setting is described as follows:

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0
POR		0	0	1	0	1	0	1	1
W	1								MUX8
POR									1
W	1						GD	SM	TB
POR							0	0	0

MUX[8:0]: Specify number of lines for the driver: MUX[8:0] + 1. Multiplex ratio (MUX ratio) from 16 MUX to 320MUX.

GD: Selects the 1st output Gate

This bit is made to match the GATE layout connection on the panel. It defines the first scanning line.

SM: Change scanning order of gate driver.

When SM is set to 0, left and right interlaced is performed.

When SM is set to 1, no splitting odd / even of the GATE signal is performed,

Output pin assignment sequence is shown as below (for 320 MUX ratio):

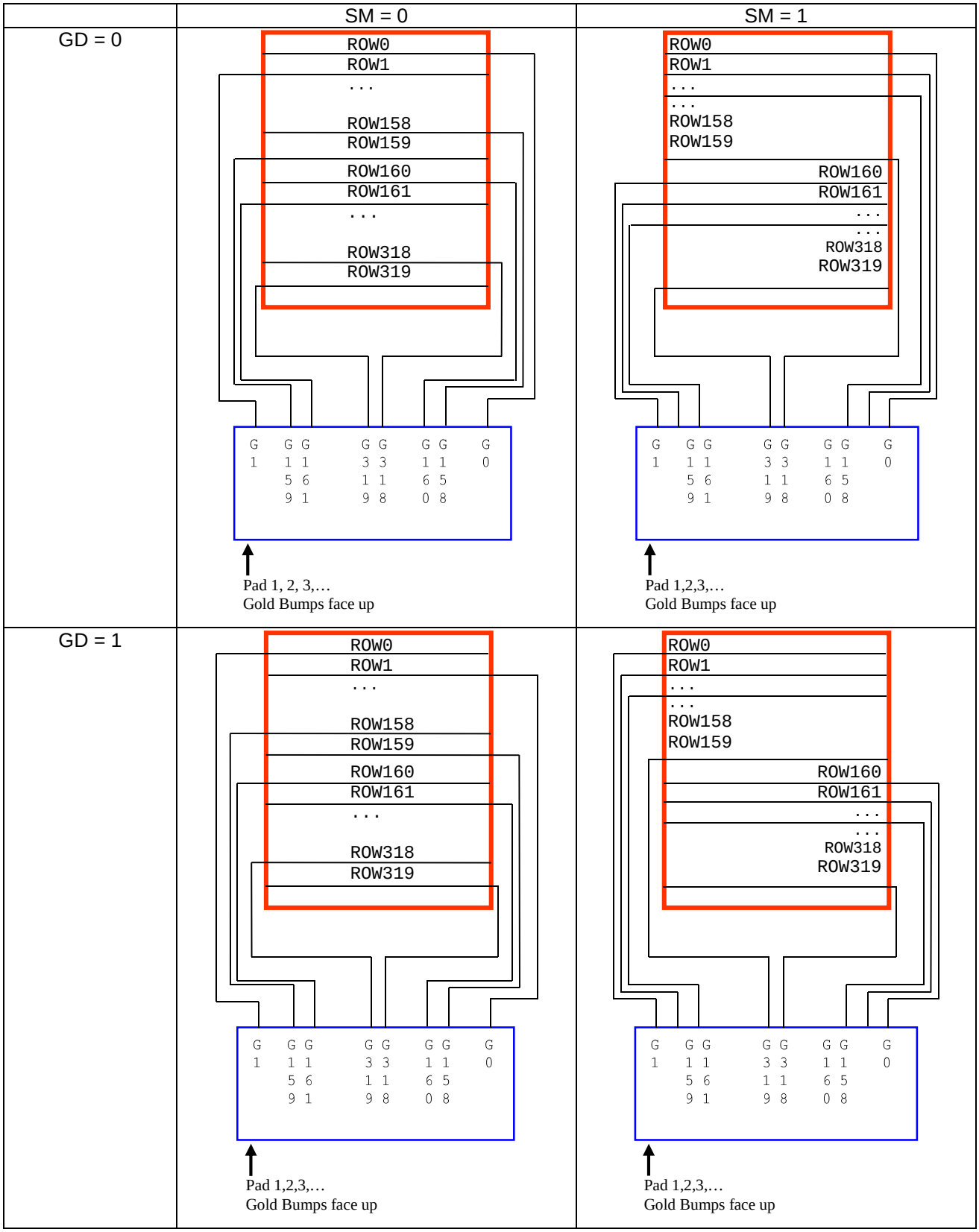
	SM=0	SM=0	SM=1	SM=1
Driver	**GD=0**	**GD=1**	**GD=0**	**GD=1**
G0	ROW0	ROW1	ROW0	ROW160
G1	ROW1	ROW0	ROW160	ROW0
G2	ROW2	ROW3	ROW1	ROW161
G3	ROW3	ROW2	ROW161	ROW1
:	:	:	:	:
G158	ROW158	ROW159	ROW79	ROW239
G159	ROW159	ROW158	ROW239	ROW79
G160	ROW160	ROW161	ROW80	ROW240
G161	ROW161	ROW160	ROW240	ROW80
:	:	:	:	:
G316	ROW316	ROW317	ROW158	ROW318
G317	ROW317	ROW316	ROW318	ROW158
G318	ROW318	ROW319	ROW159	ROW319
G319	ROW319	ROW318	ROW319	ROW159

See “Scan Mode Setting” on next page.

TB: Change scanning direction of gate driver.

This bit defines the scanning direction of the gate for flexible layout of signals in module either from up to down (TB = 0) or from bottom to up (TB = 1).

Figure 8-1: Output pin assignment on different Scan Mode Setting



8.2 Gate Scan Start Position (0Fh)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
POR		0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	0	SCN8
POR		0	0	0	0	0	0	0	0

This command is to set Gate Start Position for determining the starting gate of display RAM by selecting a value from 0 to319. Figure 8-2 shows an example using this command of this command when MUX ratio= 320 and MUX ratio= 160 “ROW” means the graphic display data RAM row.

Figure 8-2: Example of Set Display Start Line with no Remapping

	MUX ratio (01h) = 13Fh	MUX ratio (01h) = 09Fh	MUX ratio (01h) = 09Fh
GATE Pin	Gate Start Position (0Fh) = 000h	Gate Start Position (0Fh) = 000h	Gate Start Position (0Fh) = 050h
G0	ROW0	ROW0	-
G1	ROW1	ROW1	-
G2	ROW2	ROW2	-
G3	ROW3	ROW3	-
:	:	:	:
:	:	:	:
G78	:	:	-
G79	:	:	-
G80	:	:	ROW80
G81	:	:	ROW81
:	:	:	:
:	:	:	:
G158	ROW158	ROW158	:
G159	ROW159	ROW159	:
G160	ROW160	-	:
G161	ROW161	-	:
:	:	:	:
	:	:	:
G238	:	:	ROW238
G239	:	:	ROW239
G240	:	:	-
G241	:	:	-
	:	:	:
:	:	:	:
G316	ROW316	-	-
G317	ROW317	-	-
G318	ROW318	-	-
G319	ROW319	-	-
Display Example			

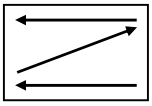
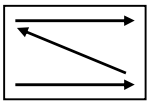
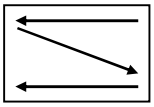
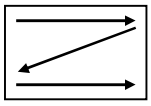
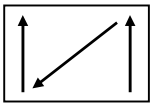
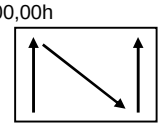
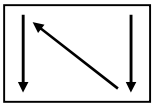
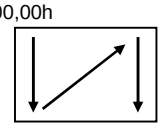
8.3 Data Entry Mode Setting (11h)

This command has multiple configurations and each bit setting is described as follows:

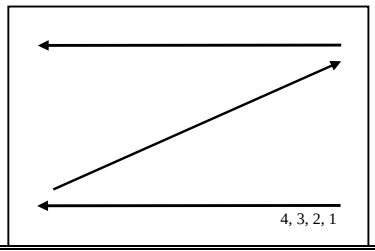
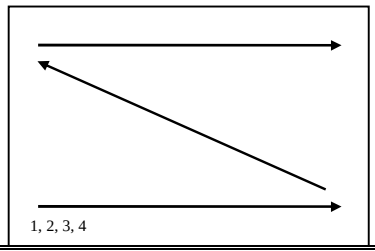
R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1						AM	ID1	ID0
POR		0	0	0	0	0	0	1	1

ID[1:0]: The address counter is automatically incremented by 1, after data is written to the RAM when ID[1:0] = “01”. The address counter is automatically decremented by 1, after data is written to the RAM when ID[1:0] = “00”. The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. The direction of the address when data is written to the RAM is set by AM bits.

AM: Set the direction in which the address counter is updated automatically after data are written to the RAM. When AM = “0”, the address counter is updated in the X direction. When AM = “1”, the address counter is updated in the Y direction. When window addresses are selected, data are written to the RAM area specified by the window addresses in the manner specified with ID[1:0] and AM bits.

	ID [1:0]="00” X: decrement Y: decrement	ID [1:0]="01” X: increment Y: decrement	ID [1:0]="10” X: decrement Y: increment	ID [1:0]="11” X: increment Y: increment
AM="0” X-mode	00,00h  18,1BFh	00,00h  18,1BFh	00,00h  18,1BFh	00,00h  18,1BFh
AM="1” Y-mode	00,00h  18,1BFh	00,00h  18,1BFh	00,00h  18,1BFh	00,00h  18,1BFh

The pixel sequence is defined by the ID [0],

	ID[1:0]="00” X: decrement Y: decrement	ID[1:0]="01” X: increment Y: decrement
AM="0” X-mode	00,00h  4, 3, 2, 1	00,00h  1, 2, 3, 4

1D,13Fh

8.4 Set RAM X - Address Start / End Position (44h)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1				XSA4	XSA3	XSA2	XSA1	XSA0
POR		0	0	0	0	0	0	0	0
W	1				XEA4	XEA3	XEA2	XEA1	XEA0
POR		0	0	0	1	1	1	0	1

XSA[4:0]/XEA[4:0]: Specify the start/end positions of the window address in the X direction by 8 times address unit. Data is written to the RAM within the area determined by the addresses specified by XSA [4:0] and XEA [4:0]. These addresses must be set before the RAM write.
It allows on XEA [4:0] ≤ XSA [4:0]. The settings follow the condition on 00h ≤ XSA [4:0], XEA [4:0] ≤ 1Dh. The windows is followed by the control setting of Data Entry Setting (R11h)

8.5 Set RAM Y - Address Start / End Position (45h)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	YSA7	YSA6	YSA5	YSA4	YSA3	YSA2	YSA1	YSA0
POR	0	0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	0	YSA8
POR		0	0	0	0	0	0	0	0
W	1	YEA7	YEA6	YEA5	YEA4	YEA3	YEA2	YEA1	YEA0
POR		0	0	1	1	1	1	1	1
W	1	0	0	0	0	0	0	0	YEA8
POR		0	0	0	0	0	0	0	1

YSA[8:0]/YEA[8:0]: Specify the start/end positions of the window address in the Y direction by an address unit. Data is written to the RAM within the area determined by the addresses specified by YSA [8:0] and YEA [8:0]. These addresses must be set before the RAM write.
It allows YEA [8:0] ≤ YSA [8:0]. The settings follow the condition on 00h ≤ YSA [8:0], YEA [8:0] ≤ 13Fh. The windows is followed by the control setting of Data Entry Setting (R11h)

8.6 Set RAM Address Counter (4Eh-4Fh)

Reg#	R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
4Eh	W	1				XAD4	XAD3	XAD2	XAD1	XAD0
	POR		0	0	0	0	0	0	0	0
4Fh	W	1	YAD7	YAD6	YAD5	YAD4	YAD3	YAD2	YAD1	YAD0
	POR		0	0	0	0	0	0	0	0
4Fh	W	1								YAD8
	POR									0

XAD[4:0]: Make initial settings for the RAM X address in the address counter (AC).
YAD[8:0]: Make initial settings for the RAM Y address in the address counter (AC).

After RAM data is written, the address counter is automatically updated according to the settings with AM, ID bits and setting for a new RAM address is not required in the address counter. Therefore, data is written consecutively without setting an address. The address counter is not automatically updated when data is read out from the RAM. RAM address setting cannot be made during the standby mode. The address setting should be made within the area designated with window addresses which is controlled by the Data Entry Setting (R11h) {AM, ID[1:0]} ; RAM Address XStart / XEnd Position (R44h) and RAM Address Ystart /Yend Position (R45h). Otherwise undesirable image will be displayed on the Panel.

9 Typical Operating Sequence

9.1 Normal Display

Sequence	Action by	Command	Action Description	Remark
1	User	-	Power on (VCI supply);	
2	User	-	HW Reset	
	IC		After HW reset, the IC will have Registers load with POR value Ready for command input VCOM register loaded with OTP value IC enter idle mode	
3		-	Send initial code to driver including setting of	
	User	C 01	Command: Panel configuration (MUX, Source gate scanning direction)	
	User	C 03	Command: VGH, VGL voltage	
	User	C 04	Command: VSH / VSL voltage	
	User	C 3A	Command: Set dummy line pulse period	
	User	C 3B	Command: Set Gate line width	
	User	C 3C	Command: Select Border waveform	
4		-	Data operations	
	User	C 11	Command: Data Entry mode	
	User	C 44	Command: X RAM address start /end	
	User	C 45	Command: Y RAM address start /end	
	User	C 4E	Command: RAM X address counter	
	User	C 4F	Command: RAM Y address counter	
	User	C 24	Command: write display data to RAM	
			Ram Content for Display	
5	User	C 22	Command: Display Update Control 2	
	User	C 20	Command: Master Activation	
	IC	-	Booster and regulators turn on	
	IC	-	Load temperature register with sensor reading	
	IC	-	Load LUT register with corresponding waveform setting stored in OTP)	
	IC	-	Send output waveform according initial update option	
	IC	-	Send output waveform according to data	
	IC	-	Booster and Regulators turn off	
	IC	-	Back to idle mode	
6	User	-	IC power off;	

OTP Selection bit:

Set on R37h, and read from R2Dh, A[7:6] used for VCOM and A[5:4] used for OTP

A[7:6] / [5:4]	Description
00	It indicates fresh device, OTP read and program would be made on Default OTP set User required setting and programming the bits into 01.
01	It indicates default OTP programmed device, OTP read would be made on Default OTP set. User require setting and programming the bits into 11
11	It indicates SPARE OTP programmed device, only OTP read would be made on SPARE OTP set. User should stop the OTP programming if 11 is found at OTP checking stage

9.2 VCOM OTP Program

Sequence	Action by	Command	Action Description	Remark
1	User	-	Power on (VCI and VPP supply)	
2	User	-	HW Reset	
3	User	C 2D	Check whether the IC status and determine whether "default" or "spare" OTP should be used	
4	User		If the IC had been OTP twice (both default and spare had been used up). The operation should stop	
5	User	C 37	Proceed OTP sequence. Command: Indicate which OTP location to be use (default or spare)	OTP selection register
	User	C 22 D 80 C 20	Command: CLKEN=1	
	User	-	Wait until BUSY = L	
6	User	C 36	Program OTP selection register	
	User	-	Wait until BUSY = L	
	User	-	Power OFF (VPP supply)	
7		-	Send initial code to driver including setting of (or leave as POR)	VCOM sensing should have same setting during application
	User	C 01	Command: Panel configuration (MUX, Source gate scanning direction)	
	User	C 03	Command: VGH, VGL voltage	
	User	C 04	Command: VSH / VSL voltage	
	User	C 3A	Command: Set dummy line pulse period	
	User	C 32	VCOM sense required full set of LUT for operation, USER required writing LUT in register 32h	
		-	LUT parameter	
	User	C 22 D 40 C 20	Command: Booster on and High voltage ready	
	User	-	Wait until BUSY = L	
8	User	C 28	Command: Enter VCOM sensing mode	
	IC	-	VCOM pin in sensing mode	
	IC	-	All Source cell have VSS output	
			All Gate scanning continuously	
	IC	-	Wait for 10s	According to R29h
	IC	-	Detect VCOM voltage and store in register	
	IC	-	All Gate Stop Scanning.	
	User	-	Wait until BUSY = L	
9	User	C 22 D 02 C 20	Command: Booster and High voltage disable	
	User	-	Wait until BUSY = L	
	User	-	Power On (VPP supply)	
10	User	C 2A	Command: VCOM OTP program	
	User	-	Wait until BUSY = L	
11	User	C 22 D 01 C 20	Command: CLKEN=0	
	User	-	Wait until BUSY = L	
12	User	-	IC power off (VCI and VPP Supply)	

9.3 WS OTP Program

Sequence	Action by	Command	Action Description	Remark
1	User	-	Power on (VCI supply)	
2	User	-	Power on (VPP supply)	
3	User	-	HW Reset	
4	User	C 2D	Check whether the IC status and determine whether "default" or "spare" OTP should be used	
5	User		If the IC had been OTP twice (both default and spare had been used up). The operation should stop	
6	User	C 37	Proceed OTP sequence. Command: Indicate which OTP location to be use (default or spare)	OTP selection register
	User	C 22 D 80 C 20	Command: CLKEN=1	
	User	-	Wait BUSY = L	
7	User	C 36	Program OTP selection register	
	User	-	Wait BUSY = L	
8	User	C 24	Write corresponding data into RAM	
			Following specific format	
			Write into RAM	
			Full LUT (11 entries + Temperature range) must be written at the same time	
	User	C 4E D 00 C 4F D 00	Command: Initial Ram address counter	
9	User	C 30	Waveform Setting OTP programming	
	IC	-	BUSY pin pull H	
	IC	-	Check the OTP Selection	
	IC	-	IC control OTP programming time, and transfer data to selected OTP	
	IC	-	BUSY pin pull L	
	User	-	Wait BUSY = L	
10	User	C 22 D 01 C 20	Command: CLKEN=0	
	User	-	Wait BUSY = L	
11	User	-	IC power off	

10 MAXIMUM RATINGS

Table 10-1: Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CI}	Logic supply voltage	-0.5 to +4.0	V
V_{IN}	Logic Input voltage	-0.5 to V_{DDIO}+0.5	V
V_{OUT}	Logic Output voltage	-0.5 to V_{DDIO}+0.5	V
T_{OPR}	Operation temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-65 to +150	°C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

11 ELECTRICAL CHARACTERISTICS

The following specifications apply for: VSS=0V, VCI=3.0V, VDD=1.8V, T_{OPR}=25ºC.

Table 11-1: DC Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
V_{CI}	VCI operation voltage		VCI	2.4	3.0	3.7	V
V_{DD}	VDD operation voltage		VDD	1.7	1.8	1.9	V
V_{COM}	VCOM output voltage		VCOM	-4.0		-0.2	V
V_{GATE}	Gate output voltage		G0-319	-20		+22	V
$V_{GATE(p-p)}$	Gate output peak to peak voltage		G0-319			42	V
V_{SH}	Positive Source output voltage		S0-239	+10		+17	V
V_{SL}	Negative Source output voltage		S0-239		-VSH		V
V_{IH}	High level input voltage		D[7:0], CS#, R/W#, D/C#, E, RES#, CLS, M/S#, CL, BS[2:0], TSDA, TSCL	$0.8V_{DDIO}$			V
V_{IL}	Low level input voltage					$0.2V_{DDIO}$	V
V_{OH}	High level output voltage	IOH = -100uA	D[7:0], BUSY, CL, TSDA, TSCL	$0.9V_{DDIO}$			V
V_{OL}	Low level output voltage	IOL = 100uA				$0.1V_{DDIO}$	V
V_{PP}	OTP Program voltage		VPP		7.5		V
Idslp_VCI	Deep Sleep mode current	VCI=3.7V DC/DC OFF No clock No output load Ram data not retain	V_{CI}		2	5	uA
Islp_VCI	Sleep mode current	VCI=3.7V DC/DC OFF No clock No output load Ram data retain	VCI		35	50	uA
Iopr_VCI	Operating current	VCI=3.0V DC/DC on VGH=22V VGL=-20V VSH=15V VSL=-15V VCOM = -2V No waveform transitions. No loading. No RAM read/write No OTP read /write Osc on Bandgap on	VCI		2000		uA
V_{GH}	Operating Mode Output Voltage	VCI=3.0V DC/DC on	VGH	21	22	23	V

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
V_{SH}		VGH=22V VGL=-20V VSH=15V VSL=-15V VCOM = -2V No waveform transitions. No loading. Osc on Bandgap on	VSH	14.5	15	15.5	V
V_{COM}			VCOM	-2.5	-2	-1.5	V
V_{SL}			VSL	-15.5	-15	-14.5	V
V_{GL}			VGL	-21	-20	-19	V

Table 11-2: Regulators Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
IVGH	VGH current	VGH = 22V	VGH			400	uA
IVGL	VGL current	VGL = -20V	VGL			600	uA
IVSH	VSH current	VSH = +15V	VSH			4000	uA
IVSL	VSL current	VSL = -15V	VSL			4000	uA
IVCOM	VCOM current	VCOM = -2V	VCOM			100	uA

12 AC CHARACTERISTICS

12.1 Oscillator frequency

The following specifications apply for: VSS=0V, VCI=3.0V, VDD=1.8V, T_{OPR}=25ºC.

Table 12-1: Oscillator Frequency

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
Fosc	Internal Oscillator frequency	VCI=2.4 to 3.7V	CL	0.95	1	1.05	MHz

12.2 Interface Timing

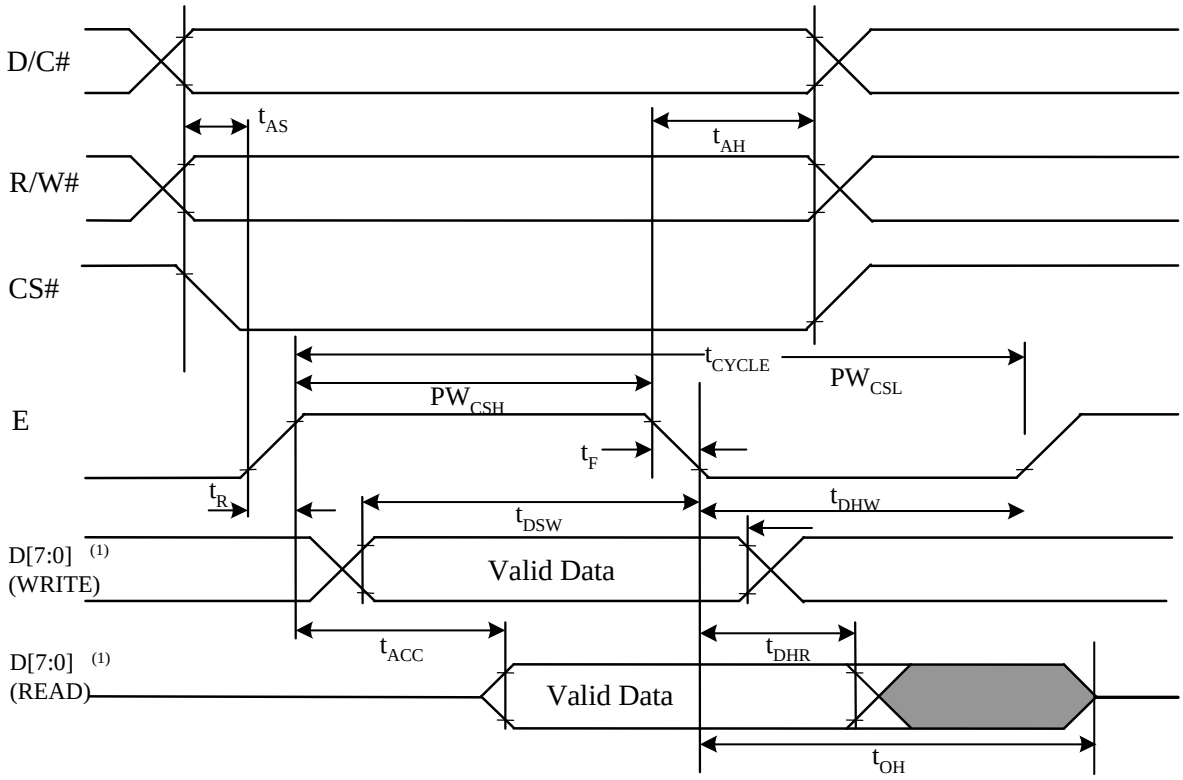
12.2.1 MCU 6800-Series Parallel Interface

Table 12-2 : 6800-Series MCU Parallel Interface Timing Characteristics

(V_{DDIO} - V_{SS} = 2.4V to 3.7V, T_{OPR} = 25°C, C_L=20pF)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time [20% ~ 80%]	-	-	15	ns
t_F	Fall Time [20% ~ 80%]	-	-	15	ns

Figure 12-1 : MCU 6800-series parallel interface characteristics



12.2.2 MCU 8080-Series Parallel Interface

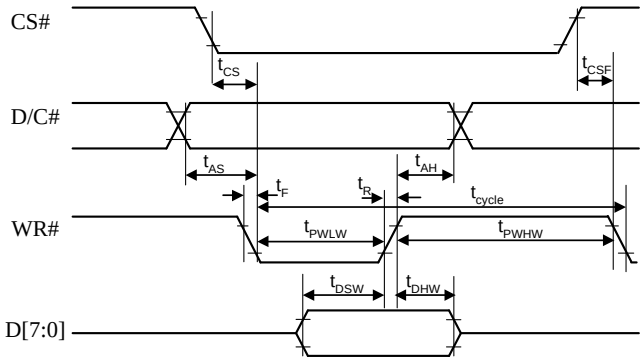
Table 12-3 : MCU 8080-Series Parallel Interface Timing Characteristics

(V_{DDIO} - V_{SS} = 2.4V to 3.7V, T_{OPR} = 25°C, C_L=20pF)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time [20% ~ 80%]	-	-	15	ns
t_F	Fall Time [20% ~ 80%]	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 12-2 : 8080-series parallel interface characteristics (Form 1)

Write cycle (Form 1)



Read cycle (Form 1)

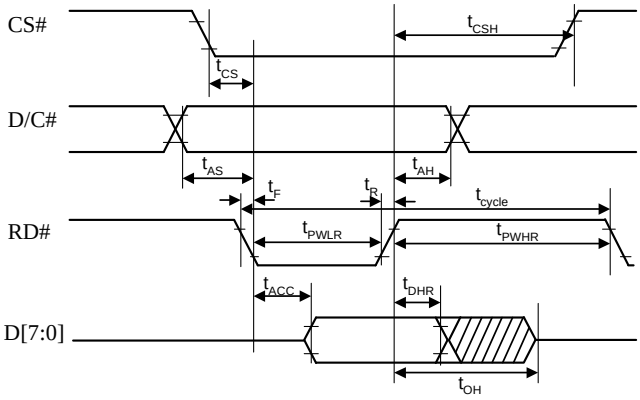
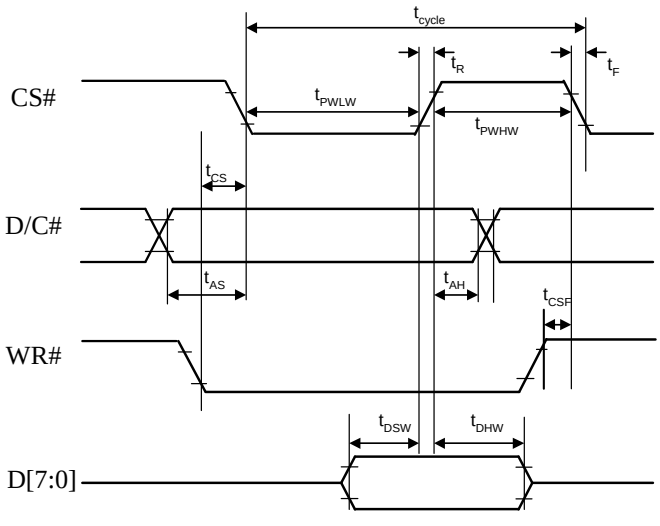
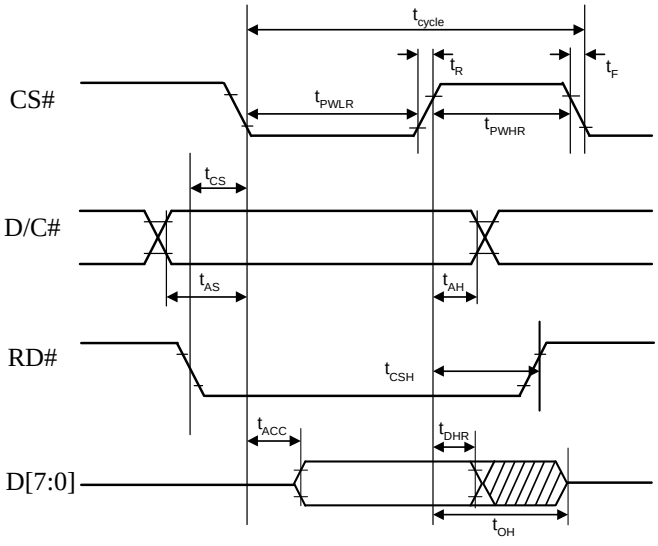


Figure 12-3 : 8080-series parallel interface characteristics (Form 2)

Write cycle (Form 2)



Read cycle (Form 2)



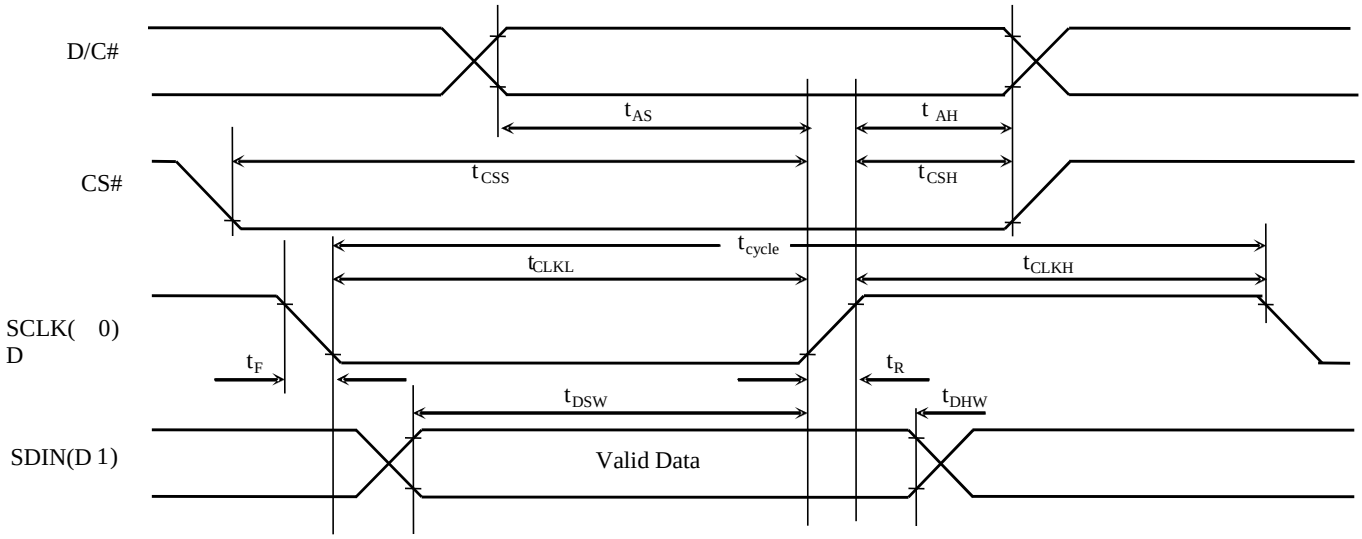
12.2.3 Serial Peripheral Interface

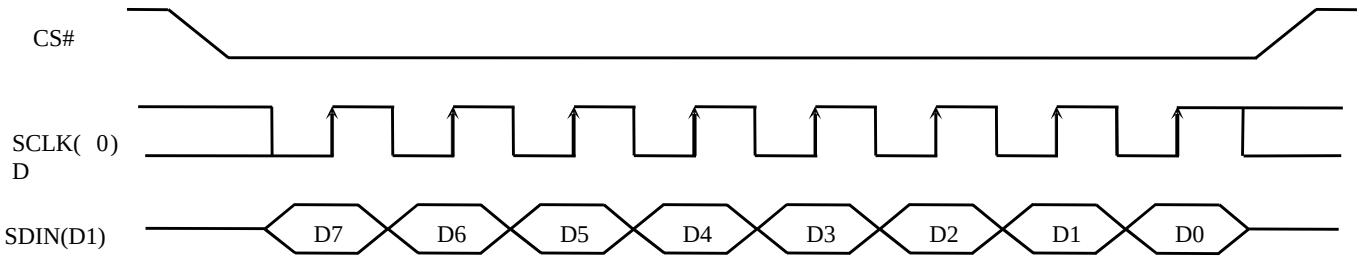
Table 12-4 : Serial Peripheral Interface Timing Characteristics

(V_{DDIO} - V_{SS} = 2.4V to 3.7V, T_{OPR} = 25°C, C_L=20pF)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time [20% ~ 80%]	-	-	15	ns
t_F	Fall Time [20% ~ 80%]	-	-	15	ns

Figure 12-4 : Serial peripheral interface characteristics





13 APPLICATION CIRCUIT

Figure 13-1 : Booster Connection Diagram

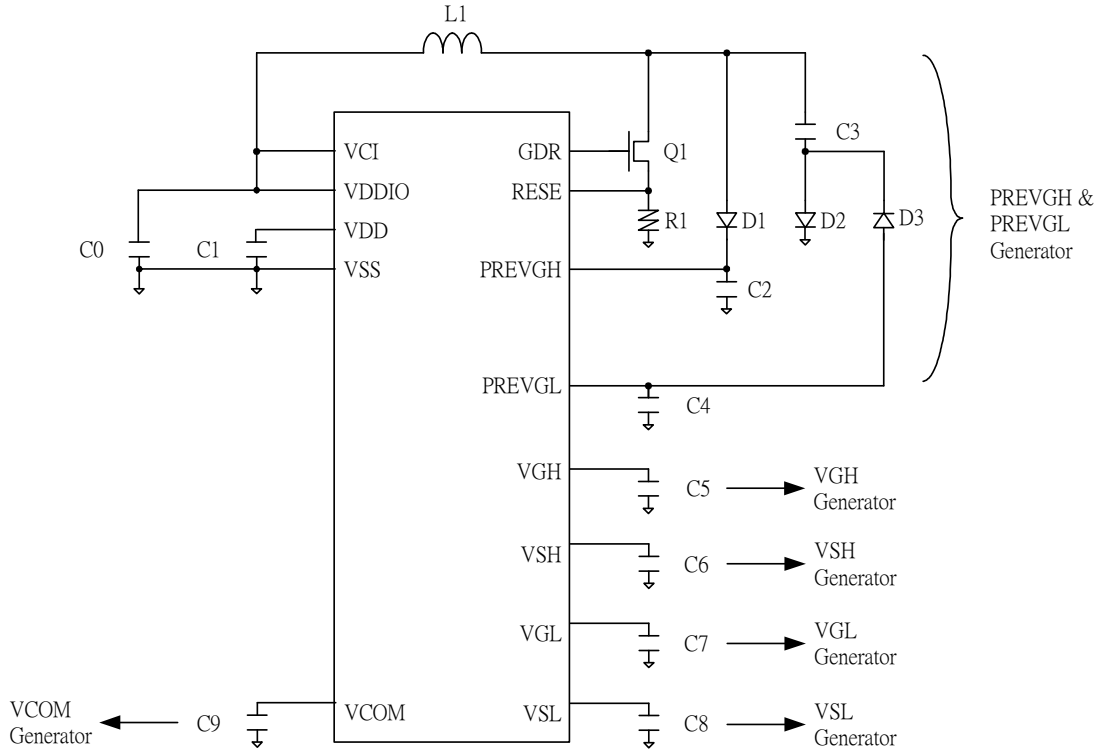


Figure 13-2 : Typical application diagram with SPI interface

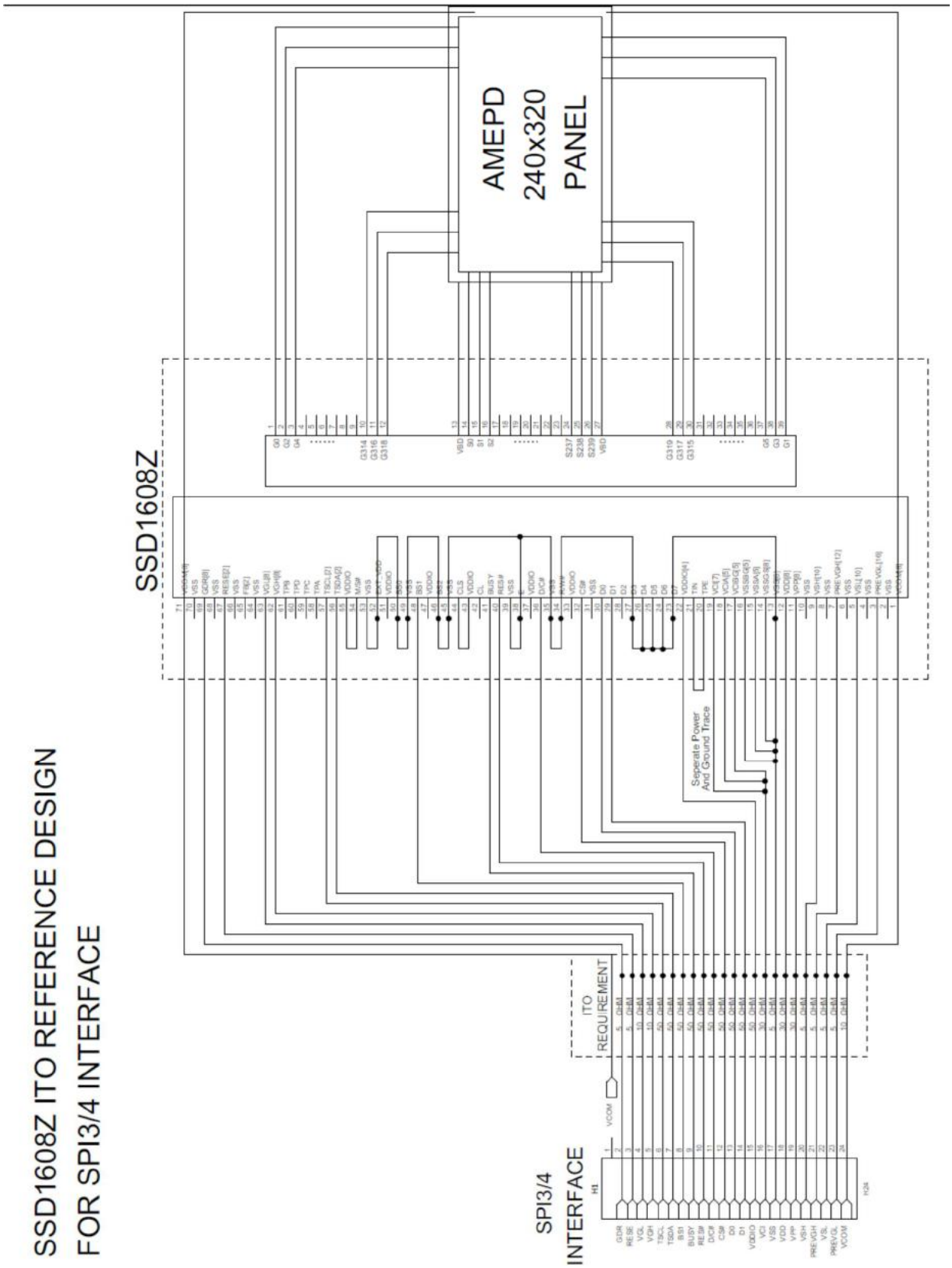


Table 13-1 : Reference Component Value

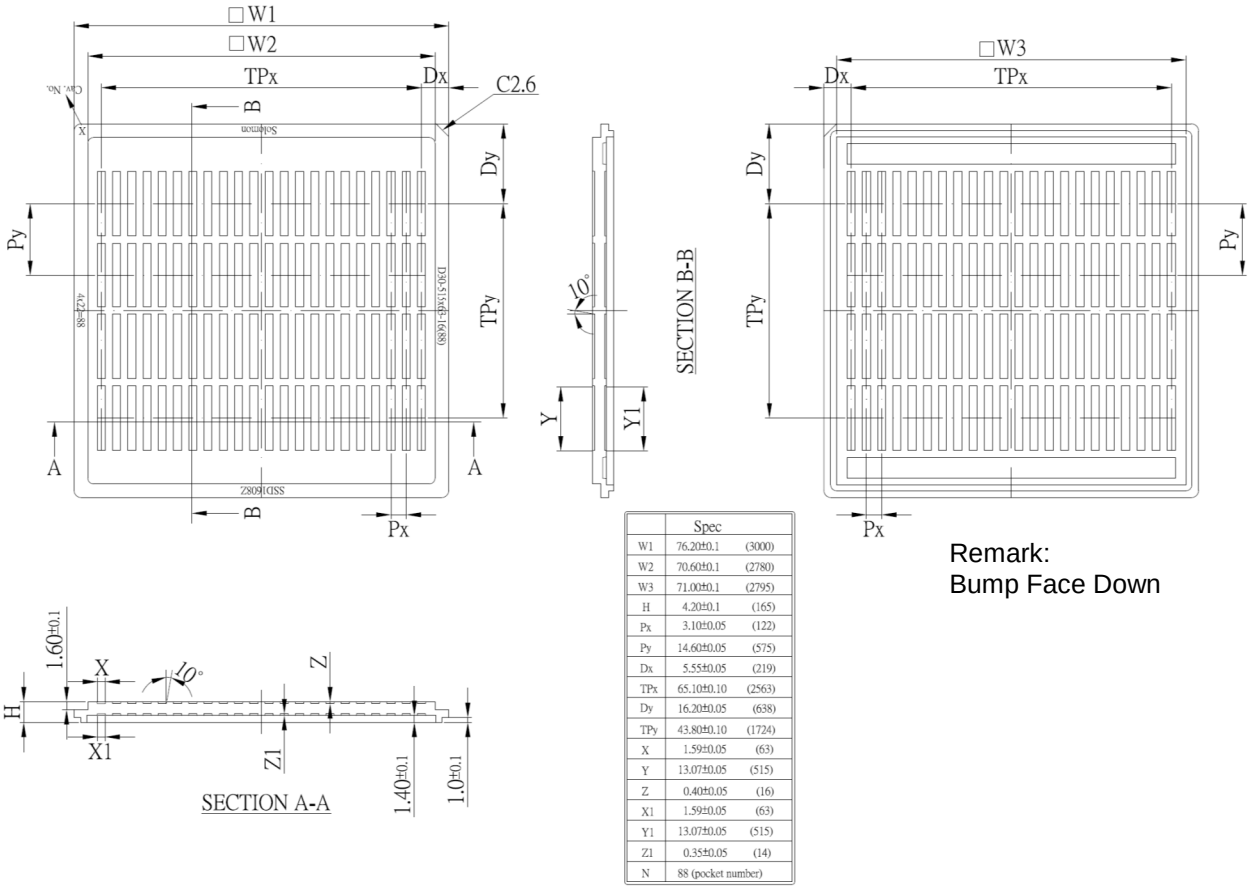
Part Name	Value	Max Volt. Rating [In V]	Pins Connected	MAX COG ITO resistance [in Ohm]
C0	1uF	6	VCI, VDDIO, VSS	5
C1	1uF	6	VDD, VSS	30
C2	1uF	50	PREVGH	5
C3	4.7uF	50	L1 and D2/D3	NA
C4	1uF	50	PREVGL	5
C5	1uF	25	VGH	10
C6	1uF	25	VSH	5
C7	1uF	25	VGL	10
C8	1uF	25	VSL	5
C9	1uF	6	VCOM	5
C10	10uF	6	VCI [Booster]	NA
C11	4.7uF	50	PREVGL [Booster]	NA
C12	1uF	50	PREVGH [Booster]	NA
C71	1uF	6	VCI [LM75A]	NA
L1	47uH			
Q1	NMOS [Vishay: Si1304BDL]		GDR, RESE	5
D1	Diode [OnSemi: MBR0530]		PREVGH	NA
D2	Diode [OnSemi: MBR0530]			NA
D3	Diode [OnSemi: MBR0530]		PREVGL, VSS	NA
R1	2.2 Ohm		RESE	5
R11	2.2kOhm			NA
R12	2.2kOhm			NA
U3	LM75A			NA

Remark: The Reference component value based on Command 0x0C, Data 0xCF,Data 0xCE,Data 0x8D sent before master activation [Command 0x20]

14 PACKAGE INFORMATION

14.1 DIE TRAY DIMENSIONS

Figure 14-1 SSD1608Z8 die tray information



	Spec	
W1	76.20±0.1	(3000)
W2	70.60±0.1	(2780)
W3	71.00±0.1	(2795)
H	4.20±0.1	(165)
Px	3.10±0.05	(122)
Py	14.60±0.05	(575)
Dx	5.55±0.05	(219)
TPx	65.10±0.10	(2563)
Dy	16.20±0.05	(638)
TPy	43.80±0.10	(1724)
X	1.59±0.05	(63)
Y	13.07±0.05	(515)
Z	0.40±0.05	(16)
X1	1.59±0.05	(63)
Y1	13.07±0.05	(515)
Z1	0.35±0.05	(14)
N	88 (pocket number)	

Remark:
Bump Face Down

The product(s) listed in this datasheet comply with Directive 2011/65/EU of the European Parliament and of the council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People’s Republic of China Electronic Industry Standard SJ/T 11363-2006 “Requirements for concentration limits for certain hazardous substances in electronic information products (电子信息产品中有毒有害物质的限量要求)”. Hazardous Substances test report is available upon request.

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