

SSD1675B

Advance Information

**160 Source x 296 Gate Red/Black/White
Active Matrix EPD Display Driver with Controller**

This document contains information on a new product. Specifications and information herein are subject to change without notice.

<http://www.solomon-systech.com>

SSD1675B

Rev 1.4

P 1/47

May 2019

Copyright © 2019 **Solomon Systech Limited**



CONTENTS

1	GENERAL DESCRIPTION	5
2	FEATURES	5
3	ORDERING INFORMATION	6
4	BLOCK DIAGRAM	6
5	PIN DESCRIPTION	7
6	FUNCTIONAL BLOCK DESCRIPTION	10
6.1	MCU INTERFACE	10
6.1.1	MCU INTERFACE SELECTION	10
6.1.2	MCU SERIAL INTERFACE (4-WIRE SPI)	10
6.1.3	MCU SERIAL PERIPHERAL INTERFACE (3-WIRE SPI)	11
6.2	OSCILLATOR	12
6.3	BOOSTER & REGULATOR	12
6.4	VCOM SENSING	12
6.5	RAM	13
6.6	PROGRAMMABLE WAVEFORM FOR GATE, SOURCE AND VCOM	13
6.7	WAVEFORM SETTING	15
6.8	TEMPERATURE SENSING	16
6.8.1	INTERNAL TEMPERATURE SENSOR	16
6.8.2	EXTERNAL TEMPERATURE SENSOR I2C SINGLE MASTER INTERFACE	16
6.8.3	FORMAT OF TEMPERATURE VALUE	16
6.9	WAVEFORM SETTING SEARCHING MECHANISM	17
6.10	ONE TIME PROGRAMMABLE (OTP) MEMORY	18
6.10.1	THE FORMAT FOR TEMPERATURE RANGE (TR)	18
6.11	VCI DETECTION	19
6.12	HV READY DETECTION	19
7	COMMAND TABLE	20
8	COMMAND DESCRIPTION	35
8.1	DRIVER OUTPUT CONTROL (01H)	35
8.2	GATE SCAN START POSITION (0FH)	37
8.3	DATA ENTRY MODE SETTING (11H)	38
8.4	SET RAM X - ADDRESS START / END POSITION (44H)	39
8.5	SET RAM Y - ADDRESS START / END POSITION (45H)	39
8.6	SET RAM ADDRESS COUNTER (4EH-4FH)	39
9	OPERATION FLOW AND CODE SEQUENCE	40
9.1	GENERAL OPERATION FLOW TO DRIVE DISPLAY PANEL	40
10	ABSOLUTE MAXIMUM RATING	41
11	ELECTRICAL CHARACTERISTICS	41
12	AC CHARACTERISTICS	43
12.1.1	SERIAL PERIPHERAL INTERFACE	43
13	APPLICATION CIRCUIT	44
14	PACKAGE INFORMATION	45
14.1.1	DIE TRAY DIMENSIONS FOR SSD1675BZ	45
14.1.2	DIE TRAY DIMENSIONS FOR SSD1675BZ8	46

TABLES

TABLE 3-1 : ORDERING INFORMATION	6
TABLE 5-1: POWER SUPPLY PINS	7
TABLE 5-2: INTERFACE LOGIC PINS.....	8
TABLE 5-3: ANALOG PINS.....	9
TABLE 5-4: DRIVER OUTPUT PINS.....	9
TABLE 5-5: MISCELLANEOUS PINS	9
TABLE 6-1 : INTERFACE PINS ASSIGNMENT UNDER DIFFERENT MCU INTERFACE	10
TABLE 6-2 : CONTROL PINS STATUS OF 4-WIRE SPI	10
TABLE 6-3 : CONTROL PINS STATUS OF 3-WIRE SPI	11
TABLE 6-4 : RAM BIT AND LUT MAPPING FOR 3-COLOR DISPLAY.....	13
TABLE 6-5 : RAM BIT AND LUT MAPPING FOR BLACK/WHITE DISPLAY	13
TABLE 6-6 : VS _[NX-LUTM] SETTINGS FOR SOURCE VOLTAGE AND VCOM VOLTAGE	14
TABLE 6-7 : EXAMPLE OF 12-BIT BINARY TEMPERATURE SETTINGS FOR TEMPERATURE RANGES	16
TABLE 6-8 : EXAMPLE OF WAVEFORM SETTINGS SELECTION BASED ON TEMPERATURE RANGES.	17
TABLE 7-1: COMMAND TABLE	20
TABLE 10-1 : MAXIMUM RATINGS	41
TABLE 11-1: DC CHARACTERISTICS.....	41
TABLE 11-2: REGULATORS CHARACTERISTICS	42
TABLE 12-1 : SERIAL PERIPHERAL INTERFACE TIMING CHARACTERISTICS	43
TABLE 13-1: COMPONENT LIST FOR SSD1675B APPLICATION CIRCUIT.....	44

FIGURES

FIGURE 4-1 : SSD1675B BLOCK DIAGRAM.....	6
FIGURE 6-1 : WRITE PROCEDURE IN 4-WIRE SPI MODE	10
FIGURE 6-2 : READ PROCEDURE IN 4-WIRE SPI MODE.....	11
FIGURE 6-3 : WRITE PROCEDURE IN 3-WIRE SPI.....	11
FIGURE 6-4 : READ PROCEDURE IN 3-WIRE SPI MODE.....	12
FIGURE 6-5 : GATE WAVEFORM AND PROGRAMMABLE SOURCE AND VCOM WAVEFORM ILLUSTRATION.....	13
FIGURE 6-6 : WAVEFORM SETTING	15
FIGURE 6-7 : THE WAVEFORM SETTING MAPPING IN OTP FOR WAVEFORM SETTING AND TEMPERATURE RANGE .	18
FIGURE 6-8 : FORMAT OF TEMPERATURE RANGE (TR) IN OTP	18
FIGURE 8-1: OUTPUT PIN ASSIGNMENT ON DIFFERENT SCAN MODE SETTING.....	36
FIGURE 8-2: EXAMPLE OF SET DISPLAY START LINE WITH NO REMAPPING	37
FIGURE 9-1: OPERATION FLOW TO DRIVE DISPLAY PANEL	40
FIGURE 12-1: SPI TIMING DIAGRAM.....	43
FIGURE 13-1: SCHEMATIC OF SSD1675B APPLICATION CIRCUIT.....	44
FIGURE 14-1 : SSD1675BZ DIE TRAY INFORMATION (UNIT: MM).....	45
FIGURE 14-2 : SSD1675BZ8 DIE TRAY INFORMATION (UNIT: MM).....	46

1 GENERAL DESCRIPTION

SSD1675B is an Active Matrix EPD display driver with controller for Red/Black/White EPD displays.

It consists of 160 source outputs, 296 gate outputs, 1 VCOM and 1VBD (for border), which can support displays with resolution up to 160 x 296.

In the SSD1675B, data and commands are sent from MCU through hardware selectable serial peripheral interface. It has embedded booster, regulator and oscillator which is suitable for EPD display applications.

2 FEATURES

- Design for dot matrix type active matrix EPD display, support Red/Black/White color
- Resolution: 160 source outputs, 296 gate outputs, 1 VCOM and 1VBD (for border)
- Power supply:
 - VCI: 2.2 to 3.7V
 - VDDIO: Connect to VCI
 - VDD: 1.8V, regulate from VCI supply
- On chip display RAM
 - Mono B/W: 160x296 bits
 - Mono Red: 160x296 bits
- On-chip booster and regulator for generating VCOM, Gate and Source driving voltage
- Gate driving output voltage: 2-level outputs (VGH, VGL), Max 40Vp-p
 - VGH: 12V to 20V (Voltage adjustment step: 500mV)
 - VGL: -VGH (Voltage adjustment step: 500mV)
- Source / VBD driving output voltage: 4-levels outputs (VSH1, VSH2, VSS and VSL)
 - VSH1/VSH2: 2.4V to 17V (Voltage adjustment step: 100mV for 2.4V to 8.8V, 200mV for 9V to 17V)
 - VSL: -9V to -17V (Voltage adjustment step: 500mV)
- VCOM output voltage
 - DCVCOM: -3V to -0.2V in 100mV resolution
 - ACVCOM: 3-level outputs (VSH1+DCVCOM, DCVCOM, VSL+DCVCOM)
- On-chip oscillator, adjustable frame rate from 15Hz to 200Hz (for Gate setting as 296 MUX)
- Programmable output waveform:
 - 40 phases (4 phases/group, 10 groups with repeat function)
 - 1 to 256 times for repeat count
 - Max. 255 frame/phase
- Embedded OTP to store the waveform settings and parameters:
 - 36 sets of Waveform Settings (WS) including waveform look up table (LUT), gate/source voltage, VCOM value and frame rate
 - 36 sets of Temperature Range (TR)
 - Display mode selection
 - 4-byte waveform version
 - 10-byte User ID
- Embedded OTP to store the init code setting
- External or internal generated voltage for burning OTP
- Built-in CRC checking method for RAM content and WS & TR in OTP
- Panel break diagnostic
- VCI low voltage detection
- Driving voltage ready detection
- Support display partial update
- Auto write RAM command for regular patterns
- Internal Temperature Sensor of +/-2degC accuracy from -25degC to 50degC
- I2C single master interface to communicate with external temperature sensor
- MCU interface: 4-wire or 3-wire Serial peripheral interface (maximum SPI write speed 20MHz)
- Available in COG package

3 ORDERING INFORMATION

Table 3-1 : Ordering Information

Ordering Part Number	Package Form	Remark
SSD1675BZ	Gold Bump Die	Bump Face Up On Waffle pack Die thickness: 300um Bump height: 12um
SSD1675BZ8	Gold Bump Die	Bump Face Down On Waffle pack Die thickness: 300um Bump height: 12um

4 BLOCK DIAGRAM

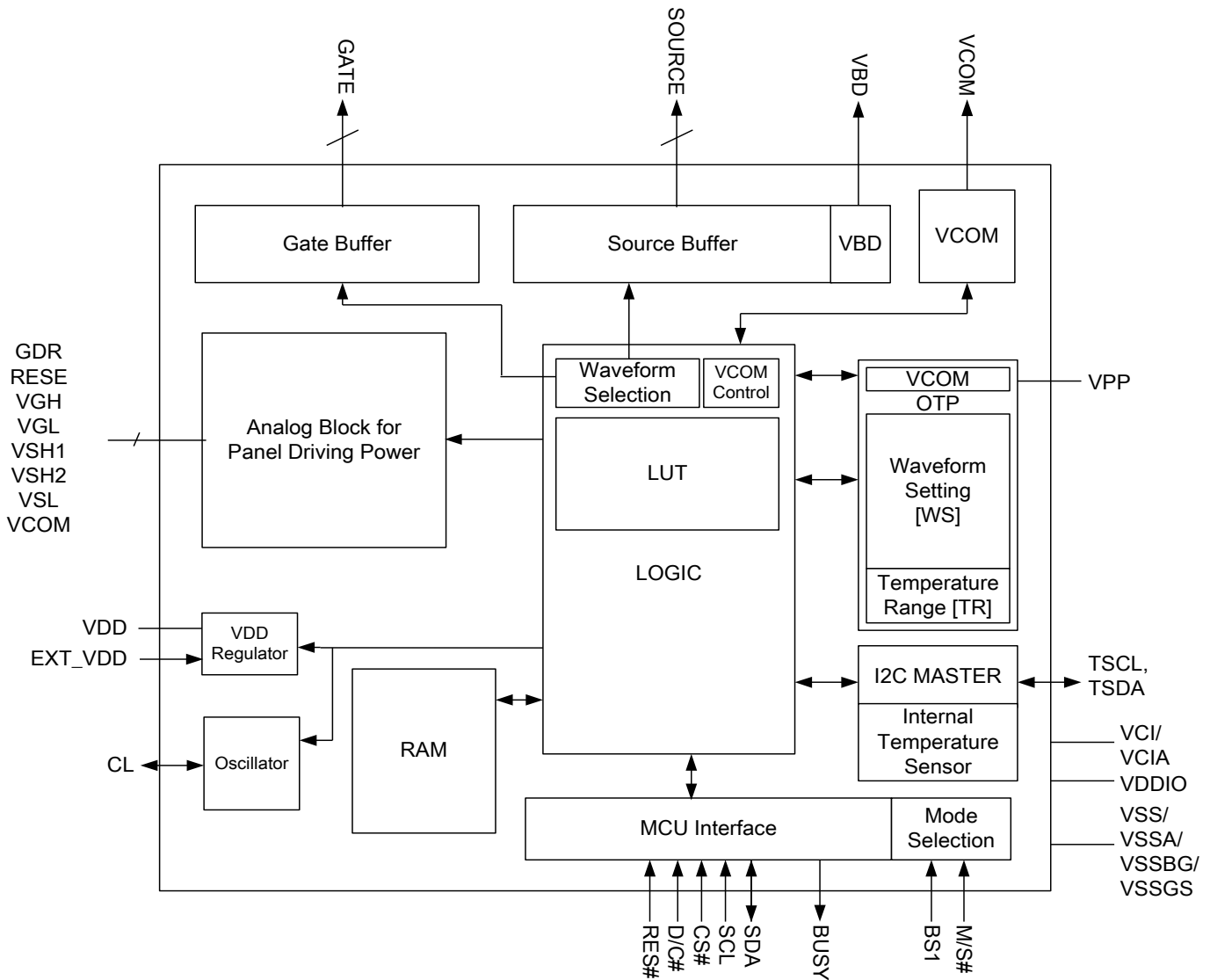


Figure 4-1 : SSD1675B Block Diagram

5 PIN DESCRIPTION

Key:

I = Input
 O =Output
 IO = Bi-directional (input/output)
 P = Power pin
 C = Capacitor Pin
 NC = Not Connected

Table 5-1: Power Supply Pins

Name	Type	Connect to	Function	Description	When not in use
VCI	P	Power Supply	Power Supply	Power input pin for the chip.	-
VCIA	P	Power Supply	Power Supply	Power input pin for the chip. - Connect to VCI in the application circuit.	-
VDDIO	P	Power Supply	Power for interface logic pins	Power input pin for the Interface. - Connect to VCI in the application circuit.	-
VDD	P	Capacitor	Regulator output	Core logic power pin VDD can be regulated internally from VCI. - A capacitor should be connected between VDD and VSS under all circumstances.	-
EXTVDD	I	VDDIO/ VSS	Regulator bypass	VDD regulator bypass pin. - EXTVDD should be connected to VSS in the application circuit.	-
VSS	P	VSS	GND	Ground (Digital).	-
VSSA	P	VSS	GND	Ground (Analog) - Connect to VSS in the application circuit.	-
VSSBG	P	VSS	GND	Ground (Reference) pin. - Connect to VSS in the application circuit.	-
VSSGS	P	VSS	GND	Ground (Output) pin. - Connect to VSS in the application circuit.	-
VPP	P	Power Supply	OTP power	Power Supply for OTP Programming.	Open

Table 5-2: Interface Logic Pins

Name	Type	Connect to	Function	Description	When not in use						
SCL	I	MPU	Data Bus	This pin is serial clock pin for interface. Refer to MCU interface in Section 6.1.	-						
SDA	I/O	MPU	Data Bus	This pin is serial data pin for interface. Refer to MCU interface in Section 6.1.	-						
CS#	I	MPU	Logic Control	This pin is the chip select input connecting to the MCU. Refer to MCU interface in Section 6.1.	VDDIO or VSS						
D/C#	I	MPU	Logic Control	This pin is Data/Command control pin connecting to the MCU. Refer to MCU interface in Section 6.1.	VDDIO or VSS						
RES#	I	MPU	System Reset	This pin is reset signal input. Active Low.	-						
BUSY	O	MPU	Device Busy Signal	This pin is Busy state output pin. When Busy is High, the operation of the chip should not be interrupted, and command should not be sent. For example., The chip would output Busy pin as High when - Outputting display waveform; or - Programming with OTP - Communicating with digital temperature sensor	Open						
M/S#	I	VDDIO/VSS	Reserved	- The M/S# pin should be connected to VDDIO.	-						
CL	I/O	NC	Clock signal	This pin is the clock signal pin. - The CL pin should be left open.	Open						
BS1	I	VDDIO/VSS	MCU Interface Mode Selection	This pin is for selecting 3-wire or 4-wire SPI bus. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>BS1</th> <th>MCU Interface</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>4-wire SPI</td> </tr> <tr> <td>H</td> <td>3-wire SPI (9-bit SPI)</td> </tr> </tbody> </table>	BS1	MCU Interface	L	4-wire SPI	H	3-wire SPI (9-bit SPI)	-
BS1	MCU Interface										
L	4-wire SPI										
H	3-wire SPI (9-bit SPI)										
TSDA	I/O	Temperature sensor SDA	Interface to Digital Temp. Sensor	This pin is I ² C Interface to digital temperature sensor Data pin. External pull up resistor is required when connecting to I ² C slave.	Open						
TSCL	O	Temperature sensor SCL	Interface to Digital Temp. Sensor	This pin is I ² C Interface to digital temperature sensor Clock pin. External pull up resistor is required when connecting to I ² C slave.	Open						

Table 5-3: Analog Pins

Name	Type	Connect to	Function	Description	When not in use
GDR	O	POWER MOSFET Driver Control	VGH, VGL Generation	This pin is N-Channel MOSFET gate drive control pin.	-
RESE	I	Booster Control Input		This pin is Current sense input pin for the control Loop.	-
VGH	C	Stabilizing capacitor		This pin is Positive Gate driving voltage. Connect a stabilizing capacitor between VGH and VSS in the application circuit.	-
VGL	C	Stabilizing capacitor		This pin is Negative Gate driving voltage. Connect a stabilizing capacitor between VGL and VSS in the application circuit.	-
VSH1	C	Stabilizing capacitor	VSH1, VSH2, VSL Generation	This pin is Positive Source driving voltage, VSH1 Connect a stabilizing capacitor between VSH1 and VSS in the application circuit.	-
VSH2	C	Stabilizing capacitor		This pin is Positive Source driving voltage, VSH2 Connect a stabilizing capacitor between VSH2 and VSS in the application circuit.	
VSL	C	Stabilizing capacitor		This pin is Negative Source driving voltage. Connect a stabilizing capacitor between VSL and VSS in the application circuit.	-
VCOM	C	Panel/ Stabilizing capacitor	VCOM Generation	This pins is VCOM driving voltage Connect a stabilizing capacitor between VCOM and VSS in the application circuit.	-

Table 5-4: Driver Output Pins

Name	Type	Connect to	Function	Description	When not in use
S [159:0]	O	Panel	Source driving signal	Source output pin.	Open
G [295:0]	O	Panel	Gate driving signal	Gate output pin.	Open
VBD	O	Panel	Border driving signal	Border output pin.	Open

Table 5-5: Miscellaneous Pins

Name	Type	Connect to	Function	Description	When not in use
NC	NC	NC	Not Connected	This is dummy pin. It should not be connected with other NC pins.	Open
RSV	NC	NC	Reserved	This is a reserved pin and should be kept open.	Open
TPA, TPB, TPC, TPD, TPF, FB	NC	NC	Reserved for Testing	Reserved pins. - Keep open. - Do not connect to other NC pins and test pins including TPA, TPB, TPC, TPD, TPE, TPF, TIN and FB.	Open
TIN	I	NC	Reserved for Testing	This is a reserved pin and should be kept open.	Open
TPE	O	NC	Reserved for Testing	This is a reserved pin and should be kept open.	Open

6 Functional Block Description

6.1 MCU Interface

6.1.1 MCU Interface selection

The SSD1675B can support 3-wire/4-wire serial peripheral. In the SSD1675B, the MCU interface is pin selectable by BS1 shown in Table 6-1.

Table 6-1 : Interface pins assignment under different MCU interface

MCU Interface	Pin Name					
	BS1	RES#	CS#	D/C#	SCL	SDA
4-wire serial peripheral interface (SPI)	L	RES#	CS#	DC#	SCL	SDA
3-wire serial peripheral interface (SPI) – 9 bits SPI	H	RES#	CS#	L	SCL	SDA

Note

(1) L is connected to V_{SS} and H is connected to V_{DDIO}

6.1.2 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, D/C# and CS#. The control pins status in 4-wire SPI in writing command/data is shown in Table 6-2 and the write procedure 4-wire SPI is shown in Table 6-2

Table 6-2 : Control pins status of 4-wire SPI

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

Note:

- (1) L is connected to V_{SS} and H is connected to V_{DDIO}
- (2) ↑ stands for rising edge of signal
- (3) SDA (Write Mode) is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

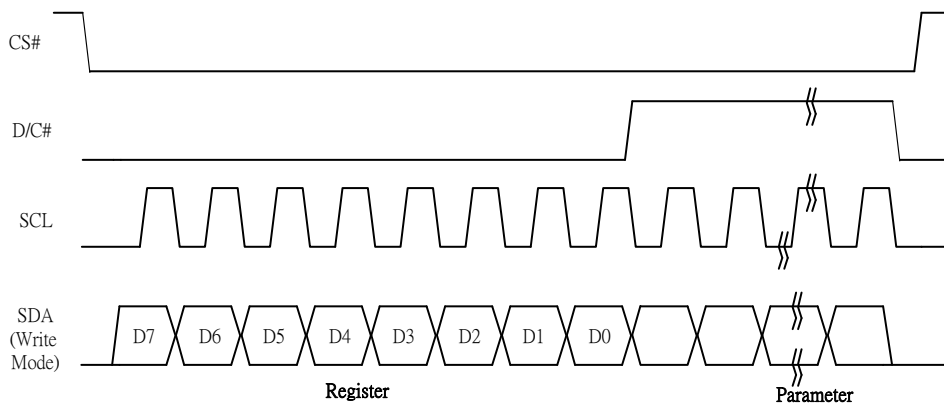


Figure 6-1 : Write procedure in 4-wire SPI mode

In the read operation (Command 0x1B, 0x27, 0x2D, 0x2E, 0x2F, 0x35). After CS# is pulled low, the first byte sent is command byte, D/C# is pulled low. After command byte sent, the following byte(s) read are data byte(s), so D/C# bit is then pulled high. An 8-bit data will be shifted out on every clock falling edge. The serial data SDA bit shifting sequence is D7, D6, to D0 bit. Figure 6-2 shows the read procedure in 4-wire SPI.

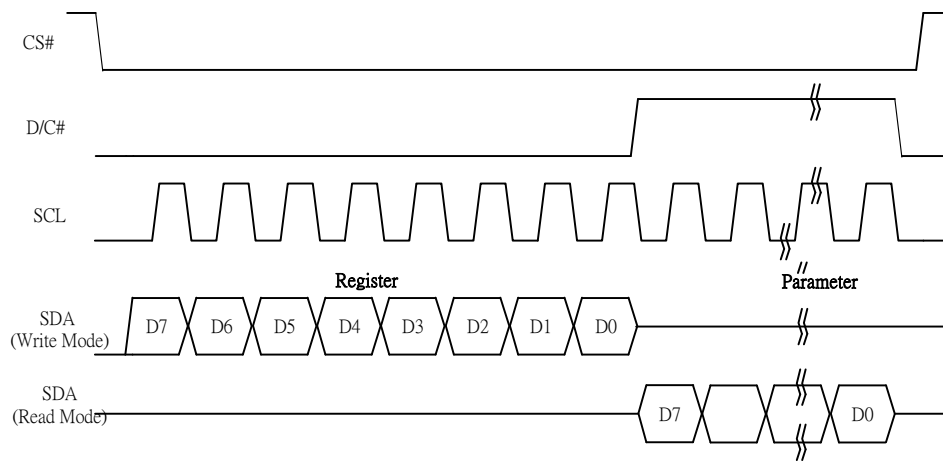


Figure 6-2 : Read procedure in 4-wire SPI mode

6.1.3 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data SDA and CS#. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 6-3.

In the write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1, the following byte is data. Table 6-3 shows the write procedure in 3-wire SPI

Table 6-3 : Control pins status of 3-wire SPI

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

Note:

- (1) L is connected to V_{SS} and H is connected to V_{DDIO}
- (2) ↑ stands for rising edge of signal

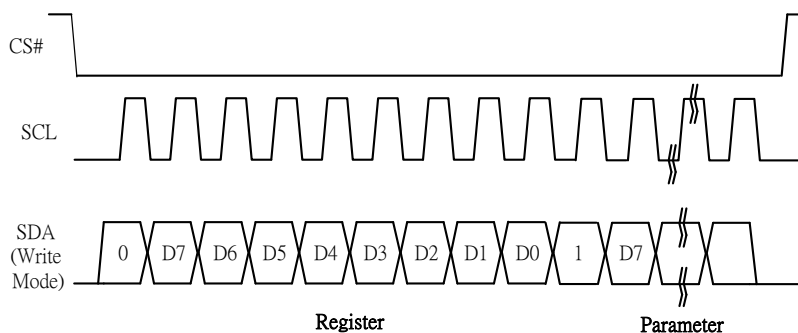


Figure 6-3 : Write procedure in 3-wire SPI

In the read operation (Register 0x1B, 0x27, 0x2D, 0x2E, 0x2F, 0x35). SDA data are transferred in the unit of 9 bits. After CS# pull low, the first byte is command byte, the D/C# bit is as 0 and following with the register byte. After command byte send, the following byte(s) are data byte(s), with D/C# bit is 1. After D/C# bit sending from MCU, an 8-bit data will be shifted out on every clock falling edge. The serial data SDA bit shifting sequence is D7, D6, to D0 bit. Figure 6-4 shows the read procedure in 3-wire SPI.

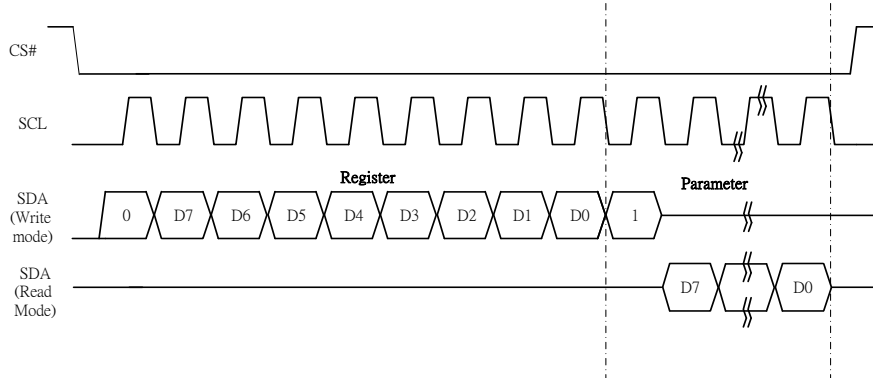


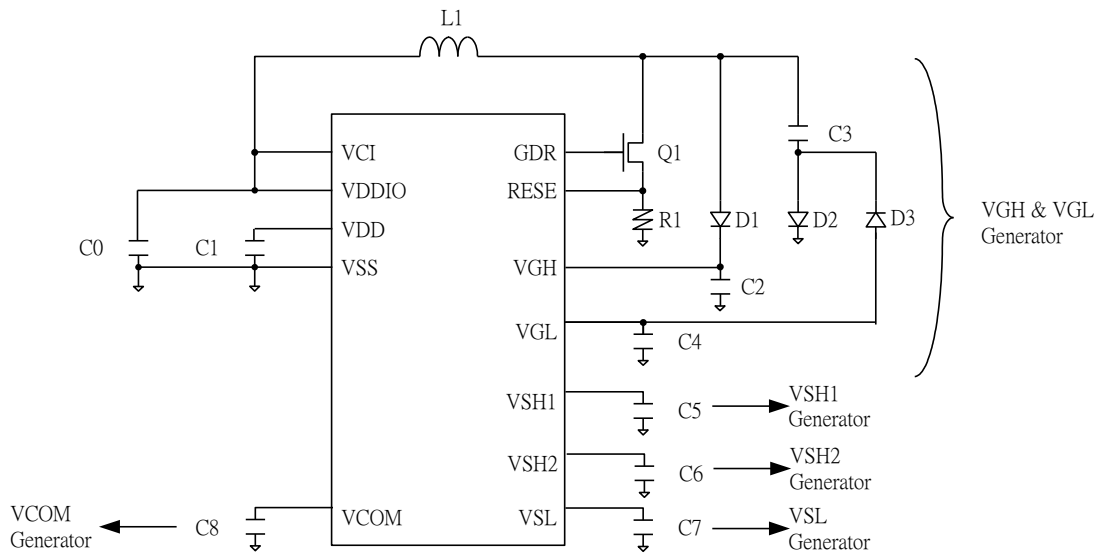
Figure 6-4 : Read procedure in 3-wire SPI mode

6.2 OSCILLATOR

The oscillator module generates the clock reference for waveform timing and analog operations.

6.3 BOOSTER & REGULATOR

A voltage generation system is included in the driver. It provides all necessary driving voltages required for an AMEPD panel including VGH, VGL, VSH1, VSH2, VSL and VCOM. External application circuit is needed to make the on-chip booster & regulator circuit work properly.



6.4 VCOM SENSING

This functional block provides the scheme to select the optimal VCOM DC level. The sensed value can be programmed into OTP.

The flow of VCOM sensing:

- Active Gate is scanning during the VCOM sense Period.
- Source are VSS.
- VCOM pin used for sensing.
- During Sensing period, BUSY is high.
- After Sensing, Active Gate return to non-select stage.

In the programmable waveform for Source and VCOM, there are 10 groups (Group0 to Group9) and each group has 4 phases (Phase A to Phase D). Totally, there are 40 phases. In addition, in each phase, the phase length (TP[nX]) can be set by number of frame from 0 to 255 frames. Also, each group can be repeated with repeat counting number (RP[n]) from 1 to 256 times. For the voltage, there is four levels for Source voltage (VSS, VSH1, VSH2, VSL) and three levels for VCOM voltage (DCVCOM, VSH1+DCVCOM, VSL+DCVCOM).

The description of each parameter is as follows.

- 1) TP[nX] represents the phase length set by the number of frame.
 - The range of TP[nX] is from 0 to 255.
 - n represents the Group number from 0 to 9; X represents the phase number from A to D.
 - When TP[nX] = 0, the phase is skipped. When TP[nX] = 1, the phase is 1 frame, and so on. The maximum phase length is 255 frame.

- 2) RP[n] represents the repeat counting number for the Group.
 - The range of RP[n] is from 0 to 255.
 - n represents the Group number from 0 to 9.
 - RP[n] = 0 indicates that the repeat times = 1, RP[n] = 1 indicates that the repeat times = 2, and so on. The maximum repeat times is 256.

- 3) VS[nX-LUTm] represents Source and VCOM voltage level which is used in each phase. Table 6-6 shows the voltage settings for source voltage and VCOM voltage.
 - n represents the Group number from 0 to 9.
 - m represents the LUT number from 0-4.

Table 6-6 : VS[nX-LUTm] settings for Source voltage and VCOM voltage

VS[nX-LUTm]	Source voltage	VCOM voltage
00	VSS	DCVCOM
01	VSH1	VSH1 + DCVCOM
10	VSL	VSL + DCVCOM
11	VSH2	N/A

6.7 WAVEFORM SETTING

As described in Section 6.6, parameters TP[nX], RP[n] and VS[nX-LUTm] are used to define the driving waveform. In the SSD1675B, there are 107 bytes in the waveform setting to store LUT0, LUT1, LUT2, LUT3 and LUT4, gate voltage, source voltage and frame rate. The waveform LUT of a particular temperature range can be loaded from OTP or written by MCU.

- WS byte 0~99, the content of VS [n-XY], TP [n#] and RP[n] are defined by Register 0x32
- WS byte 100, the content of gate level, is the parameter defined by Register 0x03.
- WS byte 101~103, the content of source level, is the parameter defined by Register 0x04.
- WS byte 104, the content of VCOM level, is the parameter defined by Register 0x2C.
- WS byte 105~106, the content of frame rate, is the parameter defined by Register 0x3A and 0x3B respectively.

The SSD1675B waveform setting is shown in Figure 6-6 : Waveform Setting.

addr.	D7	D6	D5	D4	D3	D2	D1	D0	addr.	D7	D6	D5	D4	D3	D2	D1	D0
0	VS[0A-L0]		VS[0B-L0]		VS[0C-L0]		VS[0D-L0]		50								TP[0A]
1	VS[1A-L0]		VS[1B-L0]		VS[1C-L0]		VS[1D-L0]		51								TP[0B]
2	VS[2A-L0]		VS[2B-L0]		VS[2C-L0]		VS[2D-L0]		52								TP[0C]
3	VS[3A-L0]		VS[3B-L0]		VS[3C-L0]		VS[3D-L0]		53								TP[0D]
4	VS[4A-L0]		VS[4B-L0]		VS[4C-L0]		VS[4D-L0]		54								RP[0]
5	VS[5A-L0]		VS[5B-L0]		VS[5C-L0]		VS[5D-L0]		55								TP[1A]
6	VS[6A-L0]		VS[6B-L0]		VS[6C-L0]		VS[6D-L0]		56								TP[1B]
7	VS[7A-L0]		VS[7B-L0]		VS[7C-L0]		VS[7D-L0]		57								TP[1C]
8	VS[8A-L0]		VS[8B-L0]		VS[8C-L0]		VS[8D-L0]		58								TP[1D]
9	VS[9A-L0]		VS[9B-L0]		VS[9C-L0]		VS[9D-L0]		59								RP[1]
10	VS[0A-L1]		VS[0B-L1]		VS[0C-L1]		VS[0D-L1]		60								TP[2A]
11	VS[1A-L1]		VS[1B-L1]		VS[1C-L1]		VS[1D-L1]		61								TP[2B]
12	VS[2A-L1]		VS[2B-L1]		VS[2C-L1]		VS[2D-L1]		62								TP[2C]
13	VS[3A-L1]		VS[3B-L1]		VS[3C-L1]		VS[3D-L1]		63								TP[2D]
14	VS[4A-L1]		VS[4B-L1]		VS[4C-L1]		VS[4D-L1]		64								RP[2]
15	VS[5A-L1]		VS[5B-L1]		VS[5C-L1]		VS[5D-L1]		65								TP[3A]
16	VS[6A-L1]		VS[6B-L1]		VS[6C-L1]		VS[6D-L1]		66								TP[3B]
17	VS[7A-L1]		VS[7B-L1]		VS[7C-L1]		VS[7D-L1]		67								TP[3C]
18	VS[8A-L1]		VS[8B-L1]		VS[8C-L1]		VS[8D-L1]		68								TP[3D]
19	VS[9A-L1]		VS[9B-L1]		VS[9C-L1]		VS[9D-L1]		69								RP[3]
20	VS[0A-L2]		VS[0B-L2]		VS[0C-L2]		VS[0D-L2]		70								TP[4A]
21	VS[1A-L2]		VS[1B-L2]		VS[1C-L2]		VS[1D-L2]		71								TP[4B]
22	VS[2A-L2]		VS[2B-L2]		VS[2C-L2]		VS[2D-L2]		72								TP[4C]
23	VS[3A-L2]		VS[3B-L2]		VS[3C-L2]		VS[3D-L2]		73								TP[4D]
24	VS[4A-L2]		VS[4B-L2]		VS[4C-L2]		VS[4D-L2]		74								RP[4]
25	VS[5A-L2]		VS[5B-L2]		VS[5C-L2]		VS[5D-L2]		75								TP[5A]
26	VS[6A-L2]		VS[6B-L2]		VS[6C-L2]		VS[6D-L2]		76								TP[5B]
27	VS[7A-L2]		VS[7B-L2]		VS[7C-L2]		VS[7D-L2]		77								TP[5C]
28	VS[8A-L2]		VS[8B-L2]		VS[8C-L2]		VS[8D-L2]		78								TP[5D]
29	VS[9A-L2]		VS[9B-L2]		VS[9C-L2]		VS[9D-L2]		79								RP[5]
30	VS[0A-L3]		VS[0B-L3]		VS[0C-L3]		VS[0D-L3]		80								TP[6A]
31	VS[1A-L3]		VS[1B-L3]		VS[1C-L3]		VS[1D-L3]		81								TP[6B]
32	VS[2A-L3]		VS[2B-L3]		VS[2C-L3]		VS[2D-L3]		82								TP[6C]
33	VS[3A-L3]		VS[3B-L3]		VS[3C-L3]		VS[3D-L3]		83								TP[6D]
34	VS[4A-L3]		VS[4B-L3]		VS[4C-L3]		VS[4D-L3]		84								RP[6]
35	VS[5A-L3]		VS[5B-L3]		VS[5C-L3]		VS[5D-L3]		85								TP[7A]
36	VS[6A-L3]		VS[6B-L3]		VS[6C-L3]		VS[6D-L3]		86								TP[7B]
37	VS[7A-L3]		VS[7B-L3]		VS[7C-L3]		VS[7D-L3]		87								TP[7C]
38	VS[8A-L3]		VS[8B-L3]		VS[8C-L3]		VS[8D-L3]		88								TP[7D]
39	VS[9A-L3]		VS[9B-L3]		VS[9C-L3]		VS[9D-L3]		89								RP[7]
40	VS[0A-L4]		VS[0B-L4]		VS[0C-L4]		VS[0D-L4]		90								TP[8A]
41	VS[1A-L4]		VS[1B-L4]		VS[1C-L4]		VS[1D-L4]		91								TP[8B]
42	VS[2A-L4]		VS[2B-L4]		VS[2C-L4]		VS[2D-L4]		92								TP[8C]
43	VS[3A-L4]		VS[3B-L4]		VS[3C-L4]		VS[3D-L4]		93								TP[8D]
44	VS[4A-L4]		VS[4B-L4]		VS[4C-L4]		VS[4D-L4]		94								RP[8]
45	VS[5A-L4]		VS[5B-L4]		VS[5C-L4]		VS[5D-L4]		95								TP[9A]
46	VS[6A-L4]		VS[6B-L4]		VS[6C-L4]		VS[6D-L4]		96								TP[9B]
47	VS[7A-L4]		VS[7B-L4]		VS[7C-L4]		VS[7D-L4]		97								TP[9C]
48	VS[8A-L4]		VS[8B-L4]		VS[8C-L4]		VS[8D-L4]		98								TP[9D]
49	VS[9A-L4]		VS[9B-L4]		VS[9C-L4]		VS[9D-L4]		99								RP[9]
									100								VGH
									101								VSH1
									102								VSH2
									103								VSL
									104								VCOM
									105								Frame 1
									106								Frame 2

Figure 6-6 : Waveform Setting

6.8 Temperature Sensing

The SSD1675B has internal temperature sensor to detect the environment temperature or can communicate with the external temperature sensor by I2C single master interface or can communicate with the external MCU to get the temperature value through SPI. In the SSD1675B, there is a dedicated format for the temperature value so that the driver IC can understand it. The format of temperature value is described in Section 6.8.3.

6.8.1 Internal Temperature Sensor

The internal temperature sensor can be selected by command register. The accuracy of it is $\pm 2\text{degC}$ from -25degC to 50degC.

6.8.2 External Temperature Sensor I2C Single Master Interface

The driver IC can communicate with the external temperature sensor through I2C single master interface (TSDA and TSCL). TSDA will be SDA and TSCL will be SCL. TSDA and TSCL are required to connect with external pull-up resistor. Temperature register value of external temperature sensor can be read by command register.

6.8.3 Format of temperature value

The temperature value is defined by 12-bit binary. The rules are shown as below.

- If the Temperature value MSByte bit D11 = 0, then the temperature is positive and value (DegC) = + (Temperature value) / 16
- If the Temperature value MSByte bit D11 = 1, then the temperature is negative and value (DegC) = - (2's complement of Temperature value) / 16

Table 6-7 shows some examples of 12-bit binary temperature value:

Table 6-7 : Example of 12-bit binary temperature settings for temperature ranges

12-bit binary (2's complement)	Hexadecimal Value	TR Value [DegC]
0111 1111 1111	7FF	128
0111 1111 1111	7FF	127.9
0110 0100 0000	640	100
0101 0000 0000	500	80
0100 1011 0000	4B0	75
0011 0010 0000	320	50
0001 1001 0000	190	25
0000 0000 0100	004	0.25
0000 0000 0000	000	0
1111 1111 1100	FFC	-0.25
1110 0111 0000	E70	-25
1100 1001 0000	C90	-55

6.9 Waveform Setting searching mechanism

As mentioned in Section 6.7, the SSD1675B OTP can store waveform setting and temperature range. If waveform setting and temperature range are programmed in OTP memory, corresponding waveform LUT can be selected according to the sensed temperature to drive the display. The Waveform Setting searching mechanism by driver IC is as follows.

- 1) Read temperature value by command register in the format of 12-bit binary.
- 2) According to read temperature and display mode selection, search LUT in OTP from TR0 to TR35 in sequence. The last match will be selected, then, the corresponding WS will be loaded in the LUT register to drive the display.

Remark: Waveform LUT selection criteria is “Lower temperature bound < Sensed temperature ≤ Upper temperature bound”.

Table 6-8 shows an example for the waveform LUT searching from OTP:

- If the read temperature is 25degC, then, WS4 will be selected.
- If the read temperature is 34degC, then, WS7 will be selected. Although 34degC is also in the temperature range TR6, according to searching mechanism, the last match should be selected. Therefore, WS7 is selected.

Table 6-8 : Example of waveform settings selection based on temperature ranges.

Waveform LUT in OTP	Temperature Range in OTP	TR Lower Limit [Hex]	TR Upper Limit [Hex]	Temperature range in OTP
WS0	TR0	800	050	-128 DegC < Temperature ≤ 5 DegC
WS1	TR1	050	0A0	5 DegC < Temperature ≤ 10DegC
WS2	TR2	0A0	0F0	10 DegC < Temperature ≤ 15DegC
WS3	TR3	0F0	140	15 DegC < Temperature ≤ 20DegC
WS4	TR4	140	190	20 DegC < Temperature ≤ 25DegC
WS5	TR5	190	1E0	25 DegC < Temperature ≤ 30DegC
WS6	TR6	1E0	230	30 DegC < Temperature ≤ 35DegC
WS7	TR7	210	7FF	33 DegC < Temperature ≤ 127.9DegC
Others	Others	000	000	

Precaution:

Please ensure the temperature range covers whole range of application temperatures, display will not be updated if no suitable temperature range matches the sensed temperature.

6.10 One Time Programmable (OTP) Memory

In the SSD1675B, there is an embedded OTP memory which is designed to store the waveform settings of different temperature range and some variables/parameters. The OTP memory can store 36 sets of waveform LUT settings (WS), 36 sets of temperature range (TR), VCOM value, display mode selection, waveform version and user ID. Figure 6 7 shows the address mapping of the 36 waveform setting (WS0 to WS35) and temperature range (TR0 to TR35).

addr.	D7	D6	D5	D4	D3	D2	D1	D0
0	WS0							
...								
106								
107	WS1							
...								
213								
214	WS2							
...								
320								
321	WS3							
...								
427								
	...							
	...							
3638	WS34							
...								
3744								
3745	WS35							
...								
3851								
3852	TR0							
3853								
3854								
3855	TR1							
3856								
3857								
3858	TR2							
3859								
3860								
3861	TR3							
3862								
3863								
3864	TR4							
3865								
3866								
	...							
	...							
3954	TR34							
3955								
3956								
3957	TR35							
3958								
3959								

Figure 6-7 : The Waveform setting mapping in OTP for waveform setting and temperature range

6.10.1 The Format for Temperature Range (TR)

The format of TR Lower limit and Upper limit as shown in Figure 6-8 which temp_L[11:0] is the lower limit and temp_H[11:0] is the upper limit of the temperature range. There has 36sets of TR for waveform LUT searching.

D7	D6	D5	D4	D3	D2	D1	D0
temp_L[7:0]							
temp_H[3:0]				temp_L[11:8]			
temp_H[11:4]							

Figure 6-8 : Format of Temperature Range (TR) in OTP

6.11 VCI Detection

The VCI detection function is used to detect the VCI level when it is lower than V_{low} , threshold voltage set by register.

In the SSD1675B, there is a command to execute the VCI detection function. When the VCI detection command is issued, the VCI detection will be executed. During the detection period, BUSY output is at high level. BUSY output is at low level when the detection is completed. Then, user can issue the Status Bit Read command to check the status bit for the result of VCI, which 0 is normal, 1 is $VCI < V_{low}$.

6.12 HV Ready Detection

The HV Ready detection function is used for checking if driving voltage is ready before driven the EPD panel.

In the SSD1675B, it has the flexibility to set the number of detection and the detection duration for each HV ready detection operation. And, during the detection period, BUSY output is at high level until the operation is completed. After BUSY become low level, the detection result can be read from Status register.

7 COMMAND TABLE

Table 7-1: Command Table

Command Table											Command	Description																																								
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0																																										
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	<p>Gate setting A[8:0]= 127h [POR], 296 MUX MUX Gate lines setting as (A[8:0] + 1).</p> <p>B[2:0] = 000 [POR]. Gate scanning sequence and direction</p> <p>B[2]: GD Selects the 1st output Gate GD=0 [POR], G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, ... GD=1, G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, ...</p> <p>B[1]: SM Change scanning order of gate driver. SM=0 [POR], G0, G1, G2, G3...295 (left and right gate interlaced) SM=1, G0, G2, G4 ...G294, G1, G3, ...G295</p> <p>B[0]: TB TB = 0 [POR], scan from G0 to G295 TB = 1, scan from G295 to G0.</p>																																								
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																																										
0	1		0	0	0	0	0	0	0	A ₈																																										
0	1		0	0	0	0	0	B ₂	B ₁	B ₀																																										
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage Control	<p>Set Gate driving voltage A[4:0] = 00h [POR] VGH setting from 12V to 20V</p> <table border="1"> <thead> <tr> <th>A[4:0]</th> <th>VGH</th> <th>A[4:0]</th> <th>VGH</th> </tr> </thead> <tbody> <tr> <td>07h</td> <td>12</td> <td>10h</td> <td>16.5</td> </tr> <tr> <td>08h</td> <td>12.5</td> <td>11h</td> <td>17</td> </tr> <tr> <td>09h</td> <td>13</td> <td>12h</td> <td>17.5</td> </tr> <tr> <td>0Ah</td> <td>13.5</td> <td>13h</td> <td>18</td> </tr> <tr> <td>0Bh</td> <td>14</td> <td>14h</td> <td>18.5</td> </tr> <tr> <td>0Ch</td> <td>14.5</td> <td>15h</td> <td>19</td> </tr> <tr> <td>0Dh</td> <td>15</td> <td>16h</td> <td>19.5</td> </tr> <tr> <td>0Eh</td> <td>15.5</td> <td>17h</td> <td>20</td> </tr> <tr> <td>0Fh</td> <td>16</td> <td>Other</td> <td>NA</td> </tr> </tbody> </table>	A[4:0]	VGH	A[4:0]	VGH	07h	12	10h	16.5	08h	12.5	11h	17	09h	13	12h	17.5	0Ah	13.5	13h	18	0Bh	14	14h	18.5	0Ch	14.5	15h	19	0Dh	15	16h	19.5	0Eh	15.5	17h	20	0Fh	16	Other	NA
A[4:0]	VGH	A[4:0]	VGH																																																	
07h	12	10h	16.5																																																	
08h	12.5	11h	17																																																	
09h	13	12h	17.5																																																	
0Ah	13.5	13h	18																																																	
0Bh	14	14h	18.5																																																	
0Ch	14.5	15h	19																																																	
0Dh	15	16h	19.5																																																	
0Eh	15.5	17h	20																																																	
0Fh	16	Other	NA																																																	
0	1		0	0	0	A ₄	A ₃	A ₂	A ₁	A ₀																																										

Command Table																																																																																																																																																																																																																																																																																																	
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																																																																																																																																																																																																																																																																																					
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source driving voltage A[7:0] = 41h [POR], VSH1 at 15V B[7:0] = A8h [POR], VSH2 at 5V. C[7:0] = 32h [POR], VSL at -15V																																																																																																																																																																																																																																																																																					
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																																																																																																																																																																																																																																																																																							
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀																																																																																																																																																																																																																																																																																							
0	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀																																																																																																																																																																																																																																																																																							
A[7]/B[7] = 1, VSH1/VSH2 voltage setting from 2.4V to 8.8V				A[7]/B[7] = 0, VSH1/VSH2 voltage setting from 9V to 17V				C[7] = 0, VSL setting from -9V to -17V																																																																																																																																																																																																																																																																																									
<table border="1"> <thead> <tr> <th>A/B[7:0]</th> <th>VSH1/VSH2</th> <th>A/B[7:0]</th> <th>VSH1/VSH2</th> </tr> </thead> <tbody> <tr><td>8Eh</td><td>2.4</td><td>AFh</td><td>5.7</td></tr> <tr><td>8Fh</td><td>2.5</td><td>B0h</td><td>5.8</td></tr> <tr><td>90h</td><td>2.6</td><td>B1h</td><td>5.9</td></tr> <tr><td>91h</td><td>2.7</td><td>B2h</td><td>6</td></tr> <tr><td>92h</td><td>2.8</td><td>B3h</td><td>6.1</td></tr> <tr><td>93h</td><td>2.9</td><td>B4h</td><td>6.2</td></tr> <tr><td>94h</td><td>3</td><td>B5h</td><td>6.3</td></tr> <tr><td>95h</td><td>3.1</td><td>B6h</td><td>6.4</td></tr> <tr><td>96h</td><td>3.2</td><td>B7h</td><td>6.5</td></tr> <tr><td>97h</td><td>3.3</td><td>B8h</td><td>6.6</td></tr> <tr><td>98h</td><td>3.4</td><td>B9h</td><td>6.7</td></tr> <tr><td>99h</td><td>3.5</td><td>BAh</td><td>6.8</td></tr> <tr><td>9Ah</td><td>3.6</td><td>BBh</td><td>6.9</td></tr> <tr><td>9Bh</td><td>3.7</td><td>BCh</td><td>7</td></tr> <tr><td>9Ch</td><td>3.8</td><td>BDh</td><td>7.1</td></tr> <tr><td>9Dh</td><td>3.9</td><td>BEh</td><td>7.2</td></tr> <tr><td>9Eh</td><td>4</td><td>BFh</td><td>7.3</td></tr> <tr><td>9Fh</td><td>4.1</td><td>C0h</td><td>7.4</td></tr> <tr><td>A0h</td><td>4.2</td><td>C1h</td><td>7.5</td></tr> <tr><td>A1h</td><td>4.3</td><td>C2h</td><td>7.6</td></tr> <tr><td>A2h</td><td>4.4</td><td>C3h</td><td>7.7</td></tr> <tr><td>A3h</td><td>4.5</td><td>C4h</td><td>7.8</td></tr> <tr><td>A4h</td><td>4.6</td><td>C5h</td><td>7.9</td></tr> <tr><td>A5h</td><td>4.7</td><td>C6h</td><td>8</td></tr> <tr><td>A6h</td><td>4.8</td><td>C7h</td><td>8.1</td></tr> <tr><td>A7h</td><td>4.9</td><td>C8h</td><td>8.2</td></tr> <tr><td>A8h</td><td>5</td><td>C9h</td><td>8.3</td></tr> <tr><td>A9h</td><td>5.1</td><td>CAh</td><td>8.4</td></tr> <tr><td>AAh</td><td>5.2</td><td>CBh</td><td>8.5</td></tr> <tr><td>ABh</td><td>5.3</td><td>CCh</td><td>8.6</td></tr> <tr><td>ACH</td><td>5.4</td><td>CDh</td><td>8.7</td></tr> <tr><td>ADh</td><td>5.5</td><td>CEh</td><td>8.8</td></tr> <tr><td>A Eh</td><td>5.6</td><td>Other</td><td>NA</td></tr> </tbody> </table>				A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2	8Eh	2.4	AFh	5.7	8Fh	2.5	B0h	5.8	90h	2.6	B1h	5.9	91h	2.7	B2h	6	92h	2.8	B3h	6.1	93h	2.9	B4h	6.2	94h	3	B5h	6.3	95h	3.1	B6h	6.4	96h	3.2	B7h	6.5	97h	3.3	B8h	6.6	98h	3.4	B9h	6.7	99h	3.5	BAh	6.8	9Ah	3.6	BBh	6.9	9Bh	3.7	BCh	7	9Ch	3.8	BDh	7.1	9Dh	3.9	BEh	7.2	9Eh	4	BFh	7.3	9Fh	4.1	C0h	7.4	A0h	4.2	C1h	7.5	A1h	4.3	C2h	7.6	A2h	4.4	C3h	7.7	A3h	4.5	C4h	7.8	A4h	4.6	C5h	7.9	A5h	4.7	C6h	8	A6h	4.8	C7h	8.1	A7h	4.9	C8h	8.2	A8h	5	C9h	8.3	A9h	5.1	CAh	8.4	AAh	5.2	CBh	8.5	ABh	5.3	CCh	8.6	ACH	5.4	CDh	8.7	ADh	5.5	CEh	8.8	A Eh	5.6	Other	NA	<table border="1"> <thead> <tr> <th>A/B[7:0]</th> <th>VSH1/VSH2</th> <th>A/B[7:0]</th> <th>VSH1/VSH2</th> </tr> </thead> <tbody> <tr><td>23h</td><td>9</td><td>3Ch</td><td>14</td></tr> <tr><td>24h</td><td>9.2</td><td>3Dh</td><td>14.2</td></tr> <tr><td>25h</td><td>9.4</td><td>3Eh</td><td>14.4</td></tr> <tr><td>26h</td><td>9.6</td><td>3Fh</td><td>14.6</td></tr> <tr><td>27h</td><td>9.8</td><td>40h</td><td>14.8</td></tr> <tr><td>28h</td><td>10</td><td>41h</td><td>15</td></tr> <tr><td>29h</td><td>10.2</td><td>42h</td><td>15.2</td></tr> <tr><td>2Ah</td><td>10.4</td><td>43h</td><td>15.4</td></tr> <tr><td>2Bh</td><td>10.6</td><td>44h</td><td>15.6</td></tr> <tr><td>2Ch</td><td>10.8</td><td>45h</td><td>15.8</td></tr> <tr><td>2Dh</td><td>11</td><td>46h</td><td>16</td></tr> <tr><td>2Eh</td><td>11.2</td><td>47h</td><td>16.2</td></tr> <tr><td>2Fh</td><td>11.4</td><td>48h</td><td>16.4</td></tr> <tr><td>30h</td><td>11.6</td><td>49h</td><td>16.6</td></tr> <tr><td>31h</td><td>11.8</td><td>4Ah</td><td>16.8</td></tr> <tr><td>32h</td><td>12</td><td>4Bh</td><td>17</td></tr> <tr><td>33h</td><td>12.2</td><td>Other</td><td>NA</td></tr> <tr><td>34h</td><td>12.4</td><td></td><td></td></tr> <tr><td>35h</td><td>12.6</td><td></td><td></td></tr> <tr><td>36h</td><td>12.8</td><td></td><td></td></tr> <tr><td>37h</td><td>13</td><td></td><td></td></tr> <tr><td>38h</td><td>13.2</td><td></td><td></td></tr> <tr><td>39h</td><td>13.4</td><td></td><td></td></tr> <tr><td>3Ah</td><td>13.6</td><td></td><td></td></tr> <tr><td>3Bh</td><td>13.8</td><td></td><td></td></tr> </tbody> </table>				A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2	23h	9	3Ch	14	24h	9.2	3Dh	14.2	25h	9.4	3Eh	14.4	26h	9.6	3Fh	14.6	27h	9.8	40h	14.8	28h	10	41h	15	29h	10.2	42h	15.2	2Ah	10.4	43h	15.4	2Bh	10.6	44h	15.6	2Ch	10.8	45h	15.8	2Dh	11	46h	16	2Eh	11.2	47h	16.2	2Fh	11.4	48h	16.4	30h	11.6	49h	16.6	31h	11.8	4Ah	16.8	32h	12	4Bh	17	33h	12.2	Other	NA	34h	12.4			35h	12.6			36h	12.8			37h	13			38h	13.2			39h	13.4			3Ah	13.6			3Bh	13.8			<table border="1"> <thead> <tr> <th>C[7:0]</th> <th>VSL</th> </tr> </thead> <tbody> <tr><td>1Ah</td><td>-9</td></tr> <tr><td>1Ch</td><td>-9.5</td></tr> <tr><td>1Eh</td><td>-10</td></tr> <tr><td>20h</td><td>-10.5</td></tr> <tr><td>22h</td><td>-11</td></tr> <tr><td>24h</td><td>-11.5</td></tr> <tr><td>26h</td><td>-12</td></tr> <tr><td>28h</td><td>-12.5</td></tr> <tr><td>2Ah</td><td>-13</td></tr> <tr><td>2Ch</td><td>-13.5</td></tr> <tr><td>2Eh</td><td>-14</td></tr> <tr><td>30h</td><td>-14.5</td></tr> <tr><td>32h</td><td>-15</td></tr> <tr><td>34h</td><td>-15.5</td></tr> <tr><td>36h</td><td>-16</td></tr> <tr><td>38h</td><td>-16.5</td></tr> <tr><td>3Ah</td><td>-17</td></tr> <tr><td>Other</td><td>NA</td></tr> </tbody> </table>				C[7:0]	VSL	1Ah	-9	1Ch	-9.5	1Eh	-10	20h	-10.5	22h	-11	24h	-11.5	26h	-12	28h	-12.5	2Ah	-13	2Ch	-13.5	2Eh	-14	30h	-14.5	32h	-15	34h	-15.5	36h	-16	38h	-16.5	3Ah	-17	Other	NA
A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2																																																																																																																																																																																																																																																																																														
8Eh	2.4	AFh	5.7																																																																																																																																																																																																																																																																																														
8Fh	2.5	B0h	5.8																																																																																																																																																																																																																																																																																														
90h	2.6	B1h	5.9																																																																																																																																																																																																																																																																																														
91h	2.7	B2h	6																																																																																																																																																																																																																																																																																														
92h	2.8	B3h	6.1																																																																																																																																																																																																																																																																																														
93h	2.9	B4h	6.2																																																																																																																																																																																																																																																																																														
94h	3	B5h	6.3																																																																																																																																																																																																																																																																																														
95h	3.1	B6h	6.4																																																																																																																																																																																																																																																																																														
96h	3.2	B7h	6.5																																																																																																																																																																																																																																																																																														
97h	3.3	B8h	6.6																																																																																																																																																																																																																																																																																														
98h	3.4	B9h	6.7																																																																																																																																																																																																																																																																																														
99h	3.5	BAh	6.8																																																																																																																																																																																																																																																																																														
9Ah	3.6	BBh	6.9																																																																																																																																																																																																																																																																																														
9Bh	3.7	BCh	7																																																																																																																																																																																																																																																																																														
9Ch	3.8	BDh	7.1																																																																																																																																																																																																																																																																																														
9Dh	3.9	BEh	7.2																																																																																																																																																																																																																																																																																														
9Eh	4	BFh	7.3																																																																																																																																																																																																																																																																																														
9Fh	4.1	C0h	7.4																																																																																																																																																																																																																																																																																														
A0h	4.2	C1h	7.5																																																																																																																																																																																																																																																																																														
A1h	4.3	C2h	7.6																																																																																																																																																																																																																																																																																														
A2h	4.4	C3h	7.7																																																																																																																																																																																																																																																																																														
A3h	4.5	C4h	7.8																																																																																																																																																																																																																																																																																														
A4h	4.6	C5h	7.9																																																																																																																																																																																																																																																																																														
A5h	4.7	C6h	8																																																																																																																																																																																																																																																																																														
A6h	4.8	C7h	8.1																																																																																																																																																																																																																																																																																														
A7h	4.9	C8h	8.2																																																																																																																																																																																																																																																																																														
A8h	5	C9h	8.3																																																																																																																																																																																																																																																																																														
A9h	5.1	CAh	8.4																																																																																																																																																																																																																																																																																														
AAh	5.2	CBh	8.5																																																																																																																																																																																																																																																																																														
ABh	5.3	CCh	8.6																																																																																																																																																																																																																																																																																														
ACH	5.4	CDh	8.7																																																																																																																																																																																																																																																																																														
ADh	5.5	CEh	8.8																																																																																																																																																																																																																																																																																														
A Eh	5.6	Other	NA																																																																																																																																																																																																																																																																																														
A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2																																																																																																																																																																																																																																																																																														
23h	9	3Ch	14																																																																																																																																																																																																																																																																																														
24h	9.2	3Dh	14.2																																																																																																																																																																																																																																																																																														
25h	9.4	3Eh	14.4																																																																																																																																																																																																																																																																																														
26h	9.6	3Fh	14.6																																																																																																																																																																																																																																																																																														
27h	9.8	40h	14.8																																																																																																																																																																																																																																																																																														
28h	10	41h	15																																																																																																																																																																																																																																																																																														
29h	10.2	42h	15.2																																																																																																																																																																																																																																																																																														
2Ah	10.4	43h	15.4																																																																																																																																																																																																																																																																																														
2Bh	10.6	44h	15.6																																																																																																																																																																																																																																																																																														
2Ch	10.8	45h	15.8																																																																																																																																																																																																																																																																																														
2Dh	11	46h	16																																																																																																																																																																																																																																																																																														
2Eh	11.2	47h	16.2																																																																																																																																																																																																																																																																																														
2Fh	11.4	48h	16.4																																																																																																																																																																																																																																																																																														
30h	11.6	49h	16.6																																																																																																																																																																																																																																																																																														
31h	11.8	4Ah	16.8																																																																																																																																																																																																																																																																																														
32h	12	4Bh	17																																																																																																																																																																																																																																																																																														
33h	12.2	Other	NA																																																																																																																																																																																																																																																																																														
34h	12.4																																																																																																																																																																																																																																																																																																
35h	12.6																																																																																																																																																																																																																																																																																																
36h	12.8																																																																																																																																																																																																																																																																																																
37h	13																																																																																																																																																																																																																																																																																																
38h	13.2																																																																																																																																																																																																																																																																																																
39h	13.4																																																																																																																																																																																																																																																																																																
3Ah	13.6																																																																																																																																																																																																																																																																																																
3Bh	13.8																																																																																																																																																																																																																																																																																																
C[7:0]	VSL																																																																																																																																																																																																																																																																																																
1Ah	-9																																																																																																																																																																																																																																																																																																
1Ch	-9.5																																																																																																																																																																																																																																																																																																
1Eh	-10																																																																																																																																																																																																																																																																																																
20h	-10.5																																																																																																																																																																																																																																																																																																
22h	-11																																																																																																																																																																																																																																																																																																
24h	-11.5																																																																																																																																																																																																																																																																																																
26h	-12																																																																																																																																																																																																																																																																																																
28h	-12.5																																																																																																																																																																																																																																																																																																
2Ah	-13																																																																																																																																																																																																																																																																																																
2Ch	-13.5																																																																																																																																																																																																																																																																																																
2Eh	-14																																																																																																																																																																																																																																																																																																
30h	-14.5																																																																																																																																																																																																																																																																																																
32h	-15																																																																																																																																																																																																																																																																																																
34h	-15.5																																																																																																																																																																																																																																																																																																
36h	-16																																																																																																																																																																																																																																																																																																
38h	-16.5																																																																																																																																																																																																																																																																																																
3Ah	-17																																																																																																																																																																																																																																																																																																
Other	NA																																																																																																																																																																																																																																																																																																
0	0	08	0	0	0	0	1	0	0	0	Initial Code Setting OTP Program	Program Initial Code Setting The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.																																																																																																																																																																																																																																																																																					
0	0	09	0	0	0	0	1	0	0	1	Write Register for Initial Code Setting	Write Register for Initial Code Setting Selection A[7:0] ~ D[7:0]: Reserved Details refer to Application Notes of Initial Code Setting																																																																																																																																																																																																																																																																																					
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																																																																																																																																																																																																																																																																																							
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀																																																																																																																																																																																																																																																																																							
0	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀																																																																																																																																																																																																																																																																																							
0	1		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀																																																																																																																																																																																																																																																																																							
0	0	0A	0	0	0	0	1	0	1	0	Read Register for Initial Code Setting	Read Register for Initial Code Setting																																																																																																																																																																																																																																																																																					

Command Table											Command	Description																																																								
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0																																																										
0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start Control	Booster Enable with Phase 1, Phase 2 and Phase 3 for soft start current and duration setting. A[7:0] -> Soft start setting for Phase1 = 8Bh [POR] B[7:0] -> Soft start setting for Phase2 = 9Ch [POR] C[7:0] -> Soft start setting for Phase3 = 96h [POR] D[7:0] -> Duration setting = 0Fh [POR] Bit Description of each byte: A[6:0] / B[6:0] / C[6:0]: <table border="1" data-bbox="1045 537 1500 873"> <thead> <tr> <th>Bit[6:4]</th> <th>Driving Strength Selection</th> </tr> </thead> <tbody> <tr><td>000</td><td>1(Weakest)</td></tr> <tr><td>001</td><td>2</td></tr> <tr><td>010</td><td>3</td></tr> <tr><td>011</td><td>4</td></tr> <tr><td>100</td><td>5</td></tr> <tr><td>101</td><td>6</td></tr> <tr><td>110</td><td>7</td></tr> <tr><td>111</td><td>8(Strongest)</td></tr> </tbody> </table> <table border="1" data-bbox="1045 896 1500 1444"> <thead> <tr> <th>Bit[3:0]</th> <th>Min Off Time Setting of GDR [Time unit]</th> </tr> </thead> <tbody> <tr><td>0000 ~ 0011</td><td>NA</td></tr> <tr><td>0100</td><td>2.6</td></tr> <tr><td>0101</td><td>3.2</td></tr> <tr><td>0110</td><td>3.9</td></tr> <tr><td>0111</td><td>4.6</td></tr> <tr><td>1000</td><td>5.4</td></tr> <tr><td>1001</td><td>6.3</td></tr> <tr><td>1010</td><td>7.3</td></tr> <tr><td>1011</td><td>8.4</td></tr> <tr><td>1100</td><td>9.8</td></tr> <tr><td>1101</td><td>11.5</td></tr> <tr><td>1110</td><td>13.8</td></tr> <tr><td>1111</td><td>16.5</td></tr> </tbody> </table> D[5:0]: duration setting of phase D[5:4]: duration setting of phase 3 D[3:2]: duration setting of phase 2 D[1:0]: duration setting of phase 1 <table border="1" data-bbox="1045 1568 1500 1769"> <thead> <tr> <th>Bit[1:0]</th> <th>Duration of Phase [Approximation]</th> </tr> </thead> <tbody> <tr><td>00</td><td>10ms</td></tr> <tr><td>01</td><td>20ms</td></tr> <tr><td>10</td><td>30ms</td></tr> <tr><td>11</td><td>40ms</td></tr> </tbody> </table>	Bit[6:4]	Driving Strength Selection	000	1(Weakest)	001	2	010	3	011	4	100	5	101	6	110	7	111	8(Strongest)	Bit[3:0]	Min Off Time Setting of GDR [Time unit]	0000 ~ 0011	NA	0100	2.6	0101	3.2	0110	3.9	0111	4.6	1000	5.4	1001	6.3	1010	7.3	1011	8.4	1100	9.8	1101	11.5	1110	13.8	1111	16.5	Bit[1:0]	Duration of Phase [Approximation]	00	10ms	01	20ms	10	30ms	11	40ms
Bit[6:4]	Driving Strength Selection																																																																			
000	1(Weakest)																																																																			
001	2																																																																			
010	3																																																																			
011	4																																																																			
100	5																																																																			
101	6																																																																			
110	7																																																																			
111	8(Strongest)																																																																			
Bit[3:0]	Min Off Time Setting of GDR [Time unit]																																																																			
0000 ~ 0011	NA																																																																			
0100	2.6																																																																			
0101	3.2																																																																			
0110	3.9																																																																			
0111	4.6																																																																			
1000	5.4																																																																			
1001	6.3																																																																			
1010	7.3																																																																			
1011	8.4																																																																			
1100	9.8																																																																			
1101	11.5																																																																			
1110	13.8																																																																			
1111	16.5																																																																			
Bit[1:0]	Duration of Phase [Approximation]																																																																			
00	10ms																																																																			
01	20ms																																																																			
10	30ms																																																																			
11	40ms																																																																			
0	1		1	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																																																										
0	1		1	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀																																																										
0	1		1	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀																																																										
0	1		0	0	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀																																																										

Command Table											Command	Description								
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0										
0	0	0F	0	0	0	0	1	1	1	1	Gate scan start position	Set the scanning start position of the gate driver. The valid range is from 0 to 295. A[8:0] = 000h [POR] When TB=0: SCN [8:0] = A[8:0] When TB=1: SCN [8:0] = 295 - A[8:0]								
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀										
0	1		0	0	0	0	0	0	0	A ₈										
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>A[1:0] :</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>Normal Mode [POR]</td> </tr> <tr> <td>01</td> <td>Enter Deep Sleep Mode 1</td> </tr> <tr> <td>11</td> <td>Enter Deep Sleep Mode 2</td> </tr> </tbody> </table> After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high. Remark: To Exit Deep Sleep mode, User required to send HWRESET to the driver	A[1:0] :	Description	00	Normal Mode [POR]	01	Enter Deep Sleep Mode 1	11	Enter Deep Sleep Mode 2
A[1:0] :	Description																			
00	Normal Mode [POR]																			
01	Enter Deep Sleep Mode 1																			
11	Enter Deep Sleep Mode 2																			
0	1		0	0	0	0	0	0	A ₁	A ₀										
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A[2:0] = 011 [POR] A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.								
0	1		0	0	0	0	0	A ₂	A ₁	A ₀										
0	0	12	0	0	0	1	0	0	1	0	SW RESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode During operation, BUSY pad will output high. Note: RAM are unaffected by this command.								

Command Table											Command	Description														
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0																
0	0	14	0	0	0	1	0	1	0	0	HV Ready Detection	HV ready detection A[7:0] = 00h [POR] The command required CLKEN=1 and ANALOGEN=1. Refer to Register 0x22 for detail. After this command initiated, HV Ready detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).														
0	1		0	A ₆	A ₅	A ₄	0	A ₂	A ₁	A ₀			A[6:4]=n for cool down duration: 10ms x (n+1) A[2:0]=m for number of Cool Down Loop to detect. The max HV ready duration is 10ms x (n+1) x (m) HV ready detection will be trigger after each cool down time. The detection will be completed when HV is ready. For 1 shot HV ready detection, A[7:0] can be set as 00h.													
0	0	15	0	0	0	1	0	1	0	1	VCI Detection	VCI Detection A[2:0] = 100 [POR] , Detect level at 2.3V A[2:0] : VCI level Detect <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>A[2:0]</th> <th>VCI level</th> </tr> </thead> <tbody> <tr> <td>011</td> <td>2.2V</td> </tr> <tr> <td>100</td> <td>2.3V</td> </tr> <tr> <td>101</td> <td>2.4V</td> </tr> <tr> <td>110</td> <td>2.5V</td> </tr> <tr> <td>111</td> <td>2.6V</td> </tr> <tr> <td>Other</td> <td>NA</td> </tr> </tbody> </table>	A[2:0]	VCI level	011	2.2V	100	2.3V	101	2.4V	110	2.5V	111	2.6V	Other	NA
A[2:0]	VCI level																									
011	2.2V																									
100	2.3V																									
101	2.4V																									
110	2.5V																									
111	2.6V																									
Other	NA																									
0	1		0	0	0	0	0	A ₂	A ₁	A ₀	The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. After this command initiated, VCI detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).															
0	0	18	0	0	0	1	1	0	0	0	Temperature Sensor Control	Temperature Sensor Selection A[7:0] = 48h [POR], external temperature sensor A[7:0] = 80h Internal temperature sensor														
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[11:0] = 7FFh [POR]														
0	1		A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄																
0	1		A ₃	A ₂	A ₁	A ₀	0	0	0	0																

Command Table											Command	Description												
RW#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0														
0	0	1B	0	0	0	1	1	0	1	1	Temperature Sensor Control (Read from temperature register)	Read from temperature register.												
1	1		A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄														
1	1		A ₃	A ₂	A ₁	A ₀	0	0	0	0														
0	0	1C	0	0	0	1	1	1	0	0	Temperature Sensor Control (Write Command to External temperature sensor)	Write Command to External temperature sensor. A[7:0] = 00h [POR], B[7:0] = 00h [POR], C[7:0] = 00h [POR], A[7:6] <table border="1"> <tr> <td>A[7:6]</td> <td>Select no of byte to be sent</td> </tr> <tr> <td>00</td> <td>Address + pointer</td> </tr> <tr> <td>01</td> <td>Address + pointer + 1st parameter</td> </tr> <tr> <td>10</td> <td>Address + pointer + 1st parameter + 2nd pointer</td> </tr> <tr> <td>11</td> <td>Address</td> </tr> </table> A[5:0] – Pointer Setting B[7:0] – 1 st parameter C[7:0] – 2 nd parameter The command required CLKEN=1. Refer to Register 0x22 for detail. After this command initiated, Write Command to external temperature sensor starts. BUSY pad will output high during operation.	A[7:6]	Select no of byte to be sent	00	Address + pointer	01	Address + pointer + 1st parameter	10	Address + pointer + 1st parameter + 2nd pointer	11	Address		
A[7:6]	Select no of byte to be sent																							
00	Address + pointer																							
01	Address + pointer + 1st parameter																							
10	Address + pointer + 1st parameter + 2nd pointer																							
11	Address																							
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀														
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀														
0	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀														
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h. BUSY pad will output high during operation. User should not interrupt this operation to avoid corruption of panel images.												
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	RAM content option for Display Update A[7:0] = 00h [POR] A[7:4] Red RAM option <table border="1"> <tr> <td>0000</td> <td>Normal</td> </tr> <tr> <td>0100</td> <td>Bypass RAM content as 0</td> </tr> <tr> <td>1000</td> <td>Inverse RAM content</td> </tr> </table> A[3:0] BW RAM option <table border="1"> <tr> <td>0000</td> <td>Normal</td> </tr> <tr> <td>0100</td> <td>Bypass RAM content as 0</td> </tr> <tr> <td>1000</td> <td>Inverse RAM content</td> </tr> </table>	0000	Normal	0100	Bypass RAM content as 0	1000	Inverse RAM content	0000	Normal	0100	Bypass RAM content as 0	1000	Inverse RAM content
0000	Normal																							
0100	Bypass RAM content as 0																							
1000	Inverse RAM content																							
0000	Normal																							
0100	Bypass RAM content as 0																							
1000	Inverse RAM content																							
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀														
0	1																							

Command Table											Command	Description																									
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0																											
0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation A[7:0]= FFh (POR)																									
0	1		A7	A6	A5	A4	A3	A2	A1	A0			<table border="1"> <thead> <tr> <th>Operating sequence</th> <th>Parameter (in Hex)</th> </tr> </thead> <tbody> <tr> <td>Enable clock signal</td> <td>80</td> </tr> <tr> <td>Disable clock signal</td> <td>01</td> </tr> <tr> <td>Enable clock signal → Enable Analog</td> <td>C0</td> </tr> <tr> <td>Disable Analog → Disable clock signal</td> <td>03</td> </tr> <tr> <td>Enable clock signal → Load LUT with DISPLAY Mode 1 → Disable clock signal</td> <td>91</td> </tr> <tr> <td>Enable clock signal → Load LUT with DISPLAY Mode 2 → Disable clock signal</td> <td>99</td> </tr> <tr> <td>Enable clock signal → Load temperature value → Load LUT with DISPLAY Mode 1 → Disable clock signal</td> <td>B1</td> </tr> <tr> <td>Enable clock signal → Load temperature value → Load LUT with DISPLAY Mode 2 → Disable clock signal</td> <td>B9</td> </tr> <tr> <td>Enable clock signal → Enable Analog → Display with DISPLAY Mode 1 → Disable Analog → Disable OSC</td> <td>C7</td> </tr> <tr> <td>Enable clock signal → Enable Analog → Display with DISPLAY Mode 2 → Disable Analog → Disable OSC</td> <td>CF</td> </tr> <tr> <td>Enable clock signal → Enable Analog → Load temperature value → DISPLAY with DISPLAY Mode 1 → Disable Analog → Disable OSC</td> <td>F7</td> </tr> <tr> <td>Enable clock signal → Enable Analog → Load temperature value → DISPLAY with DISPLAY Mode 2 → Disable Analog → Disable OSC</td> <td>FF</td> </tr> </tbody> </table>	Operating sequence	Parameter (in Hex)	Enable clock signal	80	Disable clock signal	01	Enable clock signal → Enable Analog	C0	Disable Analog → Disable clock signal	03	Enable clock signal → Load LUT with DISPLAY Mode 1 → Disable clock signal	91	Enable clock signal → Load LUT with DISPLAY Mode 2 → Disable clock signal	99	Enable clock signal → Load temperature value → Load LUT with DISPLAY Mode 1 → Disable clock signal	B1	Enable clock signal → Load temperature value → Load LUT with DISPLAY Mode 2 → Disable clock signal	B9	Enable clock signal → Enable Analog → Display with DISPLAY Mode 1 → Disable Analog → Disable OSC	C7	Enable clock signal → Enable Analog → Display with DISPLAY Mode 2 → Disable Analog → Disable OSC	CF	Enable clock signal → Enable Analog → Load temperature value → DISPLAY with DISPLAY Mode 1 → Disable Analog → Disable OSC	F7
Operating sequence	Parameter (in Hex)																																				
Enable clock signal	80																																				
Disable clock signal	01																																				
Enable clock signal → Enable Analog	C0																																				
Disable Analog → Disable clock signal	03																																				
Enable clock signal → Load LUT with DISPLAY Mode 1 → Disable clock signal	91																																				
Enable clock signal → Load LUT with DISPLAY Mode 2 → Disable clock signal	99																																				
Enable clock signal → Load temperature value → Load LUT with DISPLAY Mode 1 → Disable clock signal	B1																																				
Enable clock signal → Load temperature value → Load LUT with DISPLAY Mode 2 → Disable clock signal	B9																																				
Enable clock signal → Enable Analog → Display with DISPLAY Mode 1 → Disable Analog → Disable OSC	C7																																				
Enable clock signal → Enable Analog → Display with DISPLAY Mode 2 → Disable Analog → Disable OSC	CF																																				
Enable clock signal → Enable Analog → Load temperature value → DISPLAY with DISPLAY Mode 1 → Disable Analog → Disable OSC	F7																																				
Enable clock signal → Enable Analog → Load temperature value → DISPLAY with DISPLAY Mode 2 → Disable Analog → Disable OSC	FF																																				

Command Table												Command	Description
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0			
0	0	24	0	0	1	0	0	1	0	0	Write RAM (Black White) / RAM 0x24	After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly For Write pixel: Content of Write RAM(BW) = 1 For Black pixel: Content of Write RAM(BW) = 0	
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED) / RAM 0x26	After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly. For Red pixel: Content of Write RAM(RED) = 1 For non-Red pixel [Black or White]: Content of Write RAM(RED) = 0	
0	0	27	0	0	1	0	0	1	1	1	Read RAM	After this command, data read on the MCU bus will fetch data from RAM. According to parameter of Register 41h to select reading RAM0x24/ RAM0x26, until another command is written. Address pointers will advance accordingly. The 1 st byte of data read is dummy data.	
0	0	28	0	0	1	0	1	0	0	0	VCOM Sense	Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value. The sensed VCOM voltage is stored in register The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. BUSY pad will output high during operation.	
0	0	29	0	0	1	0	1	0	0	1	VCOM Sense Duration	Stabling time between entering VCOM sensing mode and reading acquired. A[3:0] = 09h [POR], duration = 10s. VCOM sense duration = (A[3:0]+1) sec	
0	1		0	1	0	0	A ₃	A ₂	A ₁	A ₀			
0	0	2A	0	0	1	0	1	0	1	0	Program VCOM OTP	Program VCOM register into OTP The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.	

Command Table											Command	Description					
RW#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0							
0	0	2B	0	0	1	0	1	0	1	1	Write Register for VCOM Control	This command is used to reduce glitch when ACVCOM toggle. Two data bytes D04h and D63h should be set for this command.					
0	1		0	0	0	0	0	1	0	0							
0	1		0	1	1	0	0	0	1	1							
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Write VCOM register from MCU interface A[7:0] = 00h [POR]					
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀							
														A[7:0]	VCOM	A[7:0]	VCOM
														08h	-0.2	44h	-1.7
														0Ch	-0.3	48h	-1.8
														10h	-0.4	4Ch	-1.9
														14h	-0.5	50h	-2
														18h	-0.6	54h	-2.1
														1Ch	-0.7	58h	-2.2
														20h	-0.8	5Ch	-2.3
														24h	-0.9	60h	-2.4
														28h	-1	64h	-2.5
														2Ch	-1.1	68h	-2.6
														30h	-1.2	6Ch	-2.7
														34h	-1.3	70h	-2.8
											38h	-1.4	74h	-2.9			
											3Ch	-1.5	78h	-3			
											40h	-1.6	Other	NA			

0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read for Display Option	Read Register for Display Option: A[7:0]: VCOM OTP Selection (Command 0x37, Byte A) B[7:0]: VCOM Register (Command 0x2C) C[7:0]~G[7:0]: Display Mode (Command 0x37, Byte B to Byte F) [5 bytes] H[7:0]~K[7:0]: Waveform Version (Command 0x37, Byte G to Byte J) [4 bytes]
1	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
1	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
1	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		
1	1		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
1	1		E ₇	E ₆	E ₅	E ₄	E ₃	E ₂	E ₁	E ₀		
1	1		F ₇	F ₆	F ₅	F ₄	F ₃	F ₂	F ₁	F ₀		
1	1		G ₇	G ₆	G ₅	G ₄	G ₃	G ₂	G ₁	G ₀		
1	1		H ₇	H ₆	H ₅	H ₄	H ₃	H ₂	H ₁	H ₀		
1	1		I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀		
1	1		J ₇	J ₆	J ₅	J ₄	J ₃	J ₂	J ₁	J ₀		
1	1	K ₇	K ₆	K ₅	K ₄	K ₃	K ₂	K ₁	K ₀			

0	0	2E	0	0	1	0	1	1	1	0	User ID Read	Read 10 Byte User ID stored in OTP: A[7:0]~J[7:0]: UserID (R38, Byte A and Byte J) [10 bytes]
1	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
1	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
1	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		
1	1		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
1	1		E ₇	E ₆	E ₅	E ₄	E ₃	E ₂	E ₁	E ₀		
1	1		F ₇	F ₆	F ₅	F ₄	F ₃	F ₂	F ₁	F ₀		
1	1		G ₇	G ₆	G ₅	G ₄	G ₃	G ₂	G ₁	G ₀		
1	1		H ₇	H ₆	H ₅	H ₄	H ₃	H ₂	H ₁	H ₀		
1	1		I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀		
1	1		J ₇	J ₆	J ₅	J ₄	J ₃	J ₂	J ₁	J ₀		

Command Table											Command	Description
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0		
0	0	2F	0	0	1	0	1	1	1	1	Status Bit Read	Read IC status Bit [POR 0x01] A[5]: HV Ready Detection flag [POR=0] 0: Ready 1: Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1: VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01] Remark: A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively.
1	1		0	0	A ₅	A ₄	0	A ₂	A ₁	A ₀		
0	0	30	0	0	1	1	0	0	0	0	Program WS OTP	Program OTP of Waveform Setting The contents should be written into RAM before sending this command. The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	31	0	0	1	1	0	0	0	1	Load WS OTP	Load OTP of Waveform Setting The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [100 bytes], which contains the content of VS [nX-LUT], TP #[nX], RP#[n] Refer to Session 6.7 Waveform Setting
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	1		:	:	:	:	:	:	:	:		
0	1			
0	0	34	0	0	1	1	0	1	0	0	CRC calculation	CRC calculation command For details, please refer to SSD1675B application note. BUSY pad will output high during operation.
0	0	35	0	0	1	1	0	1	0	1	CRC Status Read	CRC Status Read A[15:0] is the CRC read out value
1	1		A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈		
1	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	36	0	0	1	1	0	1	1	0	Program OTP selection	<p>Program OTP Selection according to the OTP Selection Control [R37h and R38h]</p> <p>The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.</p>
0	0	37	0	0	1	1	0	1	1	1	Write Register for Display Option	<p>Write Register for Display Option</p> <p>B[7:0] Display Mode for WS[7:0] C[7:0] Display Mode for WS[15:8] D[7:0] Display Mode for WS[23:16] E[7:0] Display Mode for WS[31:24] F[3:0] Display Mode for WS[35:32] 0: Display Mode 1 [POR] 1: Display Mode 2</p> <p>F[6]: PingPong for Display Mode 2 0: RAM ping-pong disable [POR] 1: RAM ping-pong enable</p> <p>G[7:0]~J[7:0] module ID /waveform version.</p> <p>Remarks: 1) A[7:0]~J[7:0] can be stored in OTP 2) RAM ping-pong function is not support for Display Mode 1</p>
0	1		0	0	0	0	0	0	0	0		
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		
0	1		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
0	1		E ₇	E ₆	E ₅	E ₄	E ₃	E ₂	E ₁	E ₀		
0	1		0	F ₆	0	0	F ₃	F ₂	F ₁	F ₀		
0	1		G ₇	G ₆	G ₅	G ₄	G ₃	G ₂	G ₁	G ₀		
0	1		H ₇	H ₆	H ₅	H ₄	H ₃	H ₂	H ₁	H ₀		
0	1		I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀		
0	1		J ₇	J ₆	J ₅	J ₄	J ₃	J ₂	J ₁	J ₀		
0	0	38	0	0	1	1	1	0	0	0	Write Register for User ID	<p>Write Register for User ID A[7:0]~J[7:0]: UserID [10 bytes]</p> <p>Remarks: A[7:0]~J[7:0] can be stored in OTP</p>
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		
0	1		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
0	1		E ₇	E ₆	E ₅	E ₄	E ₃	E ₂	E ₁	E ₀		
0	1		F ₇	F ₆	F ₅	F ₄	F ₃	F ₂	F ₁	F ₀		
0	1		G ₇	G ₆	G ₅	G ₄	G ₃	G ₂	G ₁	G ₀		
0	1		H ₇	H ₆	H ₅	H ₄	H ₃	H ₂	H ₁	H ₀		
0	1		I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀		
0	1		J ₇	J ₆	J ₅	J ₄	J ₃	J ₂	J ₁	J ₀		
0	0	39	0	0	1	1	1	0	0	1	OTP program mode	<p>OTP program mode A[1:0] = 00: Normal Mode [POR] A[1:0] = 11: Internal generated OTP programming voltage</p> <p>Remark: User is required to EXACTLY follow the reference code sequences</p>
0	1		0	0	0	0	0	0	A ₁	A ₀		

Command Table												
RW#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	3A	0	0	1	1	1	0	1	0	Set dummy line period	Set number of dummy line period A[6:0] = 30h [POR] A[6:0]: Number of dummy line period in term of TGate Available setting 0 to 127.
0	1		0	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		

0	0	3B	0	0	1	1	1	0	1	1	Set Gate line width	Set Gate line width (TGate) A[3:0] = 1010 [POR] Remark: Default value will give 50Hz Frame frequency under 48 dummy line pulse setting.
0	1		0	0	0	0	A ₃	A ₂	A ₁	A ₀		

Resolution 128x296			Resolution 104x212			Resolution 152x152		
Frame Frequency	Parameter of 0x3A	Parameter of 0x3B	Frame Frequency	Parameter of 0x3A	Parameter of 0x3B	Frame Frequency	Parameter of 0x3A	Parameter of 0x3B
25	0x2A	0x0D	25	0x29	0x0E	25	0x65	0x0E
30	0x52	0x0C	30	0x46	0x0D	30	0x3A	0x0E
35	0x1C	0x0C	35	0x1E	0x0D	35	0x1C	0x0E
40	0x47	0x0B	40	0x48	0x0C	40	0x06	0x0E
45	0x1E	0x0B	45	0x28	0x0C	45	0x24	0x0D
50	0x30	0x0A	50	0x0F	0x0C	50	0x11	0x0D
55	0x11	0x0A	55	0x37	0x0B	55	0x02	0x0D
60	0x25	0x09	60	0x21	0x0B	60	0x25	0x0C
65	0x0B	0x09	65	0x0E	0x0B	65	0x16	0x0C
70	0x2C	0x08	70	0x22	0x0A	70	0x0A	0x0C
75	0x15	0x08	75	0x11	0x0A	75	0x2C	0x0B
80	0x01	0x08	80	0x03	0x0A	80	0x1F	0x0B
85	0x1E	0x07	85	0x17	0x09	85	0x15	0x0B
90	0x0C	0x07	90	0x0A	0x09	90	0x0B	0x0B
95	0x36	0x06	95	0x26	0x08	95	0x02	0x0B
100	0x25	0x06	100	0x1A	0x08	100	0x14	0x0A
105	0x15	0x06	105	0x0E	0x08	105	0x0C	0x0A
110	0x07	0x06	110	0x04	0x08	110	0x04	0x0A
115	0x26	0x05	115	0x1D	0x07	115	0x15	0x09
120	0x18	0x05	120	0x13	0x07	120	0x0E	0x09
125	0x0B	0x05	125	0x0A	0x07	125	0x08	0x09
130	0x35	0x04	130	0x01	0x07	130	0x01	0x09
135	0x28	0x04	135	0x22	0x06	135	0x18	0x08
140	0x1C	0x04	140	0x1A	0x06	140	0x12	0x08
145	0x11	0x04	145	0x11	0x06	145	0x0C	0x08
150	0x07	0x04	150	0x0A	0x06	150	0x06	0x08
155	0x2B	0x03	155	0x03	0x06	155	0x01	0x08
160	0x20	0x03	160	0x1C	0x05	160	0x15	0x07
165	0x16	0x03	165	0x15	0x05	165	0x10	0x07
170	0x0D	0x03	170	0x0E	0x05	170	0x0B	0x07
175	0x04	0x03	175	0x07	0x05	175	0x06	0x07
180	0x33	0x02	180	0x01	0x05	180	0x02	0x07
185	0x29	0x02	185	0x21	0x04	185	0x1C	0x06
190	0x20	0x02	190	0x1B	0x04	190	0x17	0x06
195	0x18	0x02	195	0x15	0x04	195	0x12	0x06
200	0x10	0x02	200	0x0F	0x04	200	0x0E	0x06

Remark: Frame rate setting depends on resolution.

Command Table											Command	Description																														
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0																																
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A[7:0] = C0h [POR], set VBD as HiZ. A [7:6] :Select VBD option <table border="1"> <tr> <td>A[7:6]</td> <td>Select VBD as</td> </tr> <tr> <td>00</td> <td>GS Transition, Defined in A[1:0]</td> </tr> <tr> <td>01</td> <td>Fix Level, Defined in A[5:4]</td> </tr> <tr> <td>10</td> <td>VCOM</td> </tr> <tr> <td>11[POR]</td> <td>HiZ</td> </tr> </table> A [5:4] Fix Level Setting for VBD <table border="1"> <tr> <td>A[5:4]</td> <td>VBD level</td> </tr> <tr> <td>00[POR]</td> <td>VSS</td> </tr> <tr> <td>01</td> <td>VSH1</td> </tr> <tr> <td>10</td> <td>VSL</td> </tr> <tr> <td>11</td> <td>VSH2</td> </tr> </table> A [1:0] GS Transition setting for VBD <table border="1"> <tr> <td>A[1:0]</td> <td>VBD Transition</td> </tr> <tr> <td>00[POR]</td> <td>LUT0</td> </tr> <tr> <td>01</td> <td>LUT1</td> </tr> <tr> <td>10</td> <td>LUT2</td> </tr> <tr> <td>11</td> <td>LUT3</td> </tr> </table>	A[7:6]	Select VBD as	00	GS Transition, Defined in A[1:0]	01	Fix Level, Defined in A[5:4]	10	VCOM	11[POR]	HiZ	A[5:4]	VBD level	00[POR]	VSS	01	VSH1	10	VSL	11	VSH2	A[1:0]	VBD Transition	00[POR]	LUT0	01	LUT1	10	LUT2	11	LUT3
A[7:6]	Select VBD as																																									
00	GS Transition, Defined in A[1:0]																																									
01	Fix Level, Defined in A[5:4]																																									
10	VCOM																																									
11[POR]	HiZ																																									
A[5:4]	VBD level																																									
00[POR]	VSS																																									
01	VSH1																																									
10	VSL																																									
11	VSH2																																									
A[1:0]	VBD Transition																																									
00[POR]	LUT0																																									
01	LUT1																																									
10	LUT2																																									
11	LUT3																																									
0	1		A ₇	A ₆	A ₅	A ₄	0	0	A ₁	A ₀																																
0	0	41	0	1	0	0	0	0	0	1	Read RAM Option	Read RAM Option A[0]= 0 [POR] 0 : Read RAM corresponding to RAM0x24 1 : Read RAM corresponding to RAM0x26																														
0	1		0	0	0	0	0	0	0	A ₀																																
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit for RAM A[5:0]: XSA[5:0], XStart, POR = 00h B[5:0]: XEA[5:0], XEnd, POR = 13h																														
0	1		0	0	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																																
0	1		0	0	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀																																
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit for RAM A[8:0]: YSA[8:0], YStart, POR = 000h B[8:0]: YEA[8:0], YEnd, POR = 127h																														
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																																
0	1		0	0	0	0	0	0	0	A ₈																																
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀																																
0	1		0	0	0	0	0	0	0	B ₈																																

Command Table											Command	Description																																							
RW#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0																																									
0	0	46	0	1	0	0	0	1	1	0	Auto Write RED RAM for Regular Pattern	Auto Write RED RAM for Regular Pattern A[7:0] = 00h [POR]																																							
0	1		A ₇	A ₆	A ₅	A ₄	0	A ₂	A ₁	A ₀			A[7]: The 1st step value, POR = 0 A[6:4]: Step Height, POR= 000 Step of alter RAM in Y-direction according to Gate <table border="1"> <thead> <tr> <th>A[6:4]</th> <th>Height</th> <th>A[6:4]</th> <th>Height</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>8</td> <td>100</td> <td>128</td> </tr> <tr> <td>001</td> <td>16</td> <td>101</td> <td>256</td> </tr> <tr> <td>010</td> <td>32</td> <td>110</td> <td>296</td> </tr> <tr> <td>011</td> <td>64</td> <td>111</td> <td>NA</td> </tr> </tbody> </table> A[2:0]: Step Width, POR= 000 Step of alter RAM in X-direction according to Source <table border="1"> <thead> <tr> <th>A[2:0]</th> <th>Width</th> <th>A[2:0]</th> <th>Width</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>8</td> <td>100</td> <td>128</td> </tr> <tr> <td>001</td> <td>16</td> <td>101</td> <td>160</td> </tr> <tr> <td>010</td> <td>32</td> <td>110</td> <td>NA</td> </tr> <tr> <td>011</td> <td>64</td> <td>111</td> <td>NA</td> </tr> </tbody> </table> BUSY pad will output high during operation.	A[6:4]	Height	A[6:4]	Height	000	8	100	128	001	16	101	256	010	32	110	296	011	64	111	NA	A[2:0]	Width	A[2:0]	Width	000	8	100	128	001	16	101	160	010	32	110	NA	011	64
A[6:4]	Height	A[6:4]	Height																																																
000	8	100	128																																																
001	16	101	256																																																
010	32	110	296																																																
011	64	111	NA																																																
A[2:0]	Width	A[2:0]	Width																																																
000	8	100	128																																																
001	16	101	160																																																
010	32	110	NA																																																
011	64	111	NA																																																
0	0	47	0	1	0	0	0	1	1	1	Auto Write B/W RAM for Regular Pattern	Auto Write B/W RAM for Regular Pattern A[7:0] = 00h [POR]																																							
0	1		A ₇	A ₆	A ₅	A ₄	0	A ₂	A ₁	A ₀			A[7]: The 1st step value, POR = 0 A[6:4]: Step Height, POR= 000 Step of alter RAM in Y-direction according to Gate <table border="1"> <thead> <tr> <th>A[6:4]</th> <th>Height</th> <th>A[6:4]</th> <th>Height</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>8</td> <td>100</td> <td>128</td> </tr> <tr> <td>001</td> <td>16</td> <td>101</td> <td>256</td> </tr> <tr> <td>010</td> <td>32</td> <td>110</td> <td>296</td> </tr> <tr> <td>011</td> <td>64</td> <td>111</td> <td>NA</td> </tr> </tbody> </table> A[2:0]: Step Width, POR= 000 Step of alter RAM in X-direction according to Source <table border="1"> <thead> <tr> <th>A[2:0]</th> <th>Width</th> <th>A[2:0]</th> <th>Width</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>8</td> <td>100</td> <td>128</td> </tr> <tr> <td>001</td> <td>16</td> <td>101</td> <td>160</td> </tr> <tr> <td>010</td> <td>32</td> <td>110</td> <td>NA</td> </tr> <tr> <td>011</td> <td>64</td> <td>111</td> <td>NA</td> </tr> </tbody> </table> During operation, BUSY pad will output high.	A[6:4]	Height	A[6:4]	Height	000	8	100	128	001	16	101	256	010	32	110	296	011	64	111	NA	A[2:0]	Width	A[2:0]	Width	000	8	100	128	001	16	101	160	010	32	110	NA	011	64
A[6:4]	Height	A[6:4]	Height																																																
000	8	100	128																																																
001	16	101	256																																																
010	32	110	296																																																
011	64	111	NA																																																
A[2:0]	Width	A[2:0]	Width																																																
000	8	100	128																																																
001	16	101	160																																																
010	32	110	NA																																																
011	64	111	NA																																																

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[5:0]: 00h [POR].
0	1		0	0	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: 000h [POR].
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	1		0	0	0	0	0	0	0	A ₈		
0	0	74	0	1	1	1	0	1	0	0	Set Analog Block Control	A[7:0]: 54h [POR]
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	0	7E	0	1	1	1	1	1	1	0	Set Digital Block Control	A[7:0]: 3Bh [POR]
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	0	7F	0	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read Commands.

8 COMMAND DESCRIPTION

8.1 Driver Output Control (01h)

This triple byte command has multiple configurations and each bit setting is described as follows:

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0
	POR	0	0	1	1	1	1	1	1
W	1								MUX8
	POR								1
W	1						GD	SM	TB
	POR						0	0	0

MUX[8:0]: Specify number of lines for the driver: MUX[8:0] + 1. Multiplex ratio (MUX ratio) from 16 MUX to 296MUX.

GD: Selects the 1st output Gate

This bit is made to match the GATE layout connection on the panel. It defines the first scanning line.

SM: Change scanning order of gate driver.

When SM is set to 0, left and right interlaced is performed.

When SM is set to 1, no splitting odd / even of the GATE signal is performed,

Output pin assignment sequence is shown as below (for 296 MUX ratio):

Driver	SM=0 GD=0	SM=0 GD=1	SM=1 GD=0	SM=1 GD=1
G0	ROW0	ROW1	ROW0	ROW148
G1	ROW1	ROW0	ROW148	ROW0
G2	ROW2	ROW3	ROW1	ROW149
G3	ROW3	ROW2	ROW149	ROW1
:	:	:	:	:
G146	ROW146	ROW147	ROW73	ROW222
G147	ROW147	ROW146	ROW222	ROW73
G148	ROW148	ROW149	ROW74	ROW223
G149	ROW149	ROW148	ROW223	ROW74
:	:	:	:	:
G292	ROW292	ROW293	ROW146	ROW294
G293	ROW293	ROW292	ROW294	ROW146
G294	ROW294	ROW295	ROW147	ROW295
G295	ROW295	ROW294	ROW295	ROW147

See "Scan Mode Setting" on next page.

TB: Change scanning direction of gate driver.

This bit defines the scanning direction of the gate for flexible layout of signals in module either from up to down (TB = 0) or from bottom to up (TB = 1).

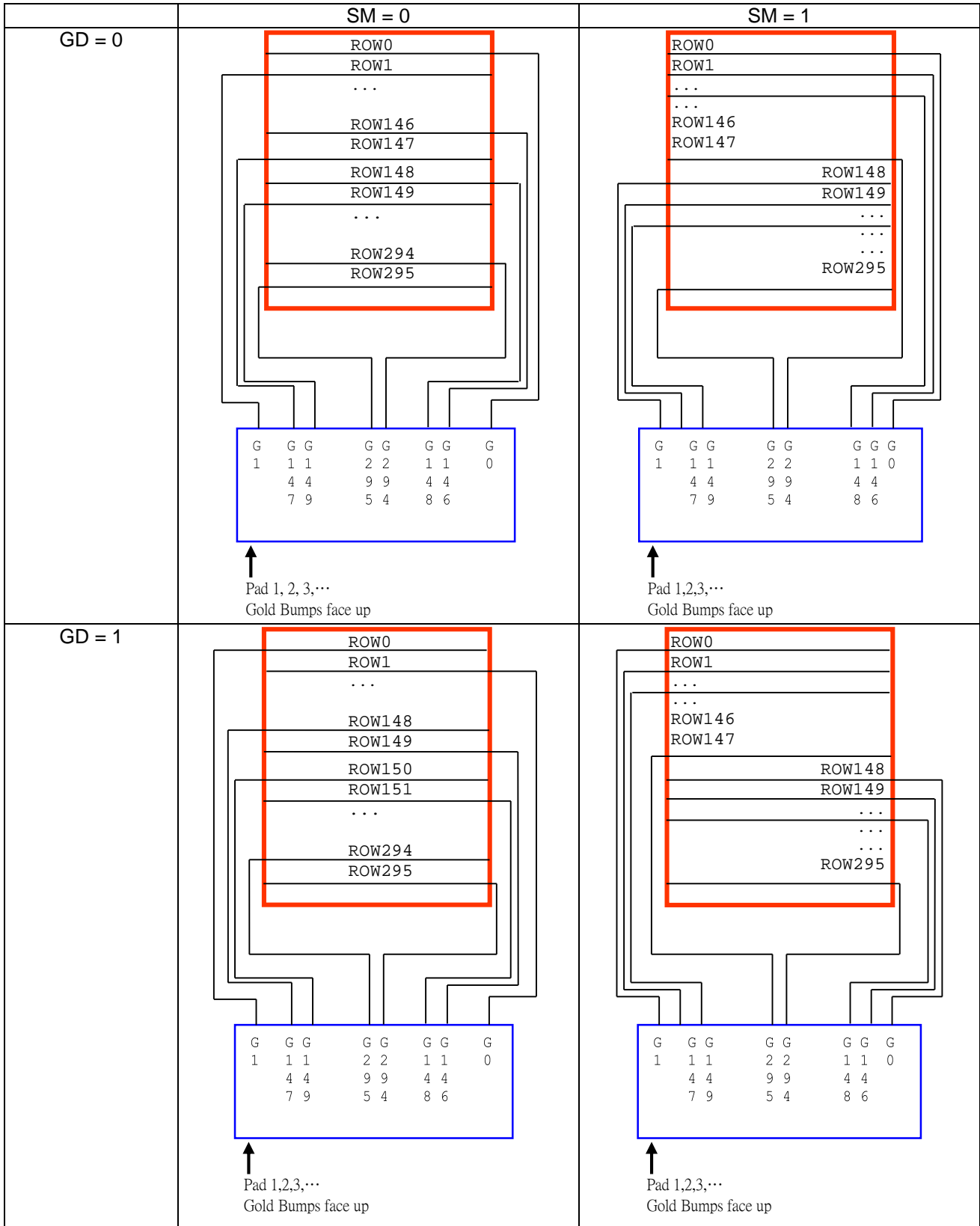





Figure 8-1: Output pin assignment on different Scan Mode Setting

8.2 Gate Scan Start Position (0Fh)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
POR		0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	0	SCN8
POR		0	0	0	0	0	0	0	0

This command is to set Gate Start Position for determining the starting gate of display RAM by selecting a value from 0 to 295. Figure 8-2 shows an example using this command of this command when MUX ratio= 295 and MUX ratio= 148 “ROW” means the graphic display data RAM row.

Figure 8-2: Example of Set Display Start Line with no Remapping

GATE Pin	MUX ratio (01h) = 127h	MUX ratio (01h) = 093h	MUX ratio (01h) = 095h
	Gate Start Position (0Fh) = 000h	Gate Start Position (0Fh) = 000h	Gate Start Position (0Fh) = 04Ah
G0	ROW0	ROW0	-
G1	ROW1	ROW1	-
G2	ROW2	ROW2	-
G3	ROW3	ROW3	-
⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮
G72	⋮	⋮	-
G73	⋮	⋮	-
G74	⋮	⋮	ROW74
G75	⋮	⋮	ROW75
⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮
G146	ROW146	ROW146	⋮
G147	ROW147	ROW147	⋮
G148	ROW148	-	⋮
G149	ROW149	-	⋮
⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮
G220	⋮	⋮	⋮
G221	⋮	⋮	⋮
G222	⋮	⋮	ROW222
G223	⋮	⋮	ROW223
⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮
G292	ROW292	-	-
G293	ROW293	-	-
G294	ROW294	-	-
G295	ROW295	-	-
Display Example			

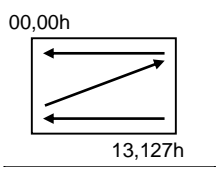
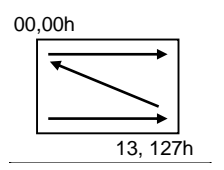
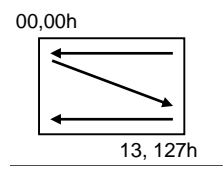
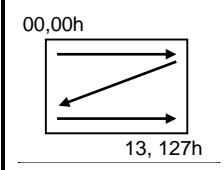
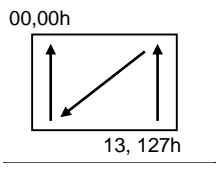
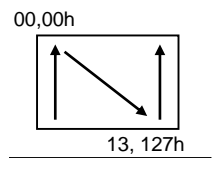
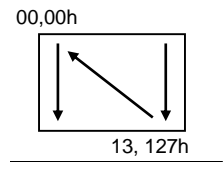
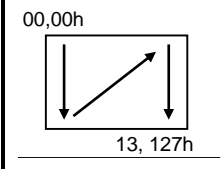
8.3 Data Entry Mode Setting (11h)

This command has multiple configurations and each bit setting is described as follows:

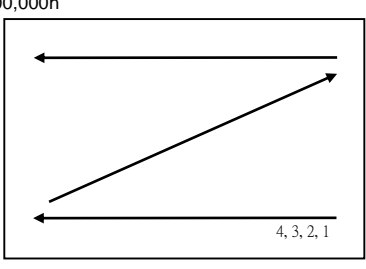
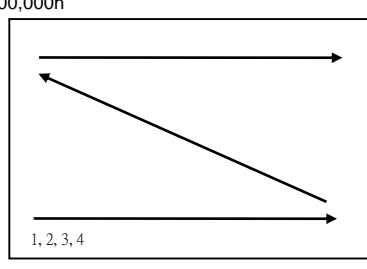
R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1						AM	ID1	ID0
POR		0	0	0	0	0	0	1	1

ID[1:0]: The address counter is automatically incremented by 1, after data is written to the RAM when ID[1:0] = "01". The address counter is automatically decremented by 1, after data is written to the RAM when ID[1:0] = "00". The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. The direction of the address when data is written to the RAM is set by AM bits.

AM: Set the direction in which the address counter is updated automatically after data are written to the RAM. When AM = "0", the address counter is updated in the X direction. When AM = "1", the address counter is updated in the Y direction. When window addresses are selected, data are written to the RAM area specified by the window addresses in the manner specified with ID[1:0] and AM bits.

	ID [1:0]="00" X: decrement Y: decrement	ID [1:0]="01" X: increment Y: decrement	ID [1:0]="10" X: decrement Y: increment	ID [1:0]="11" X: increment Y: increment
AM="0" X-mode				
AM="1" Y-mode				

The pixel sequence is defined by the ID [0],

	ID[1:0]="00" X: decrement Y: decrement	ID[1:0]="01" X: increment Y: decrement
AM="0" X-mode		

8.4 Set RAM X - Address Start / End Position (44h)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1				XSA4	XSA3	XSA2	XSA1	XSA0
POR		0	0	0	0	0	0	0	0
W	1				XEA4	XEA3	XEA2	XEA1	XEA0
POR		0	0	0	1	0	0	1	1

XSA[4:0]/XEA[4:0]: Specify the start/end positions of the window address in the X direction by 8 times address unit. Data is written to the RAM within the area determined by the addresses specified by XSA [4:0] and XEA [4:0]. These addresses must be set before the RAM write.

It allows on $XEA [4:0] \leq XSA [4:0]$. The settings follow the condition on $00h \leq XSA [4:0]$, $XEA [4:0] \leq 13h$. The windows is followed by the control setting of Data Entry Setting (R11h)

8.5 Set RAM Y - Address Start / End Position (45h)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	YSA7	YSA6	YSA5	YSA4	YSA3	YSA2	YSA1	YSA0
POR		0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	0	YSA8
POR		0	0	0	0	0	0	0	0
W	1	YEA7	YEA6	YEA5	YEA4	YEA3	YEA2	YEA1	YEA0
POR		0	0	1	0	0	1	1	1
W	1	0	0	0	0	0	0	0	YEA8
POR		0	0	0	0	0	0	0	1

YSA[8:0]/YEA[8:0]: Specify the start/end positions of the window address in the Y direction by an address unit. Data is written to the RAM within the area determined by the addresses specified by YSA [8:0] and YEA [8:0]. These addresses must be set before the RAM write.

It allows $YEA [8:0] \leq YSA [8:0]$. The settings follow the condition on $00h \leq YSA [8:0]$, $YEA [8:0] \leq 127h$. The windows is followed by the control setting of Data Entry Setting (R11h)

8.6 Set RAM Address Counter (4Eh-4Fh)

Reg#	R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
4Eh	W	1				XAD4	XAD3	XAD2	XAD1	XAD0
	POR		0	0	0	0	0	0	0	0
4Fh	W	1	YAD7	YAD6	YAD5	YAD4	YAD3	YAD2	YAD1	YAD0
	POR		0	0	0	0	0	0	0	0
	W	1								YAD8
	POR									

XAD[4:0]: Make initial settings for the RAM X address in the address counter (AC).

YAD[8:0]: Make initial settings for the RAM Y address in the address counter (AC).

After RAM data is written, the address counter is automatically updated according to the settings with AM, ID bits and setting for a new RAM address is not required in the address counter. Therefore, data is written consecutively without setting an address. The address counter is not automatically updated when data is read out from the RAM. RAM address setting cannot be made during the standby mode. The address setting should be made within the area designated with window addresses which is controlled by the Data Entry Setting (R11h) {AM, ID[1:0]} ; RAM Address XStart / XEnd Position (R44h) and RAM Address Ystart /Yend Position (R45h). Otherwise undesirable image will be displayed on the Panel.

9 Operation Flow and Code Sequence

9.1 General operation flow to drive display panel

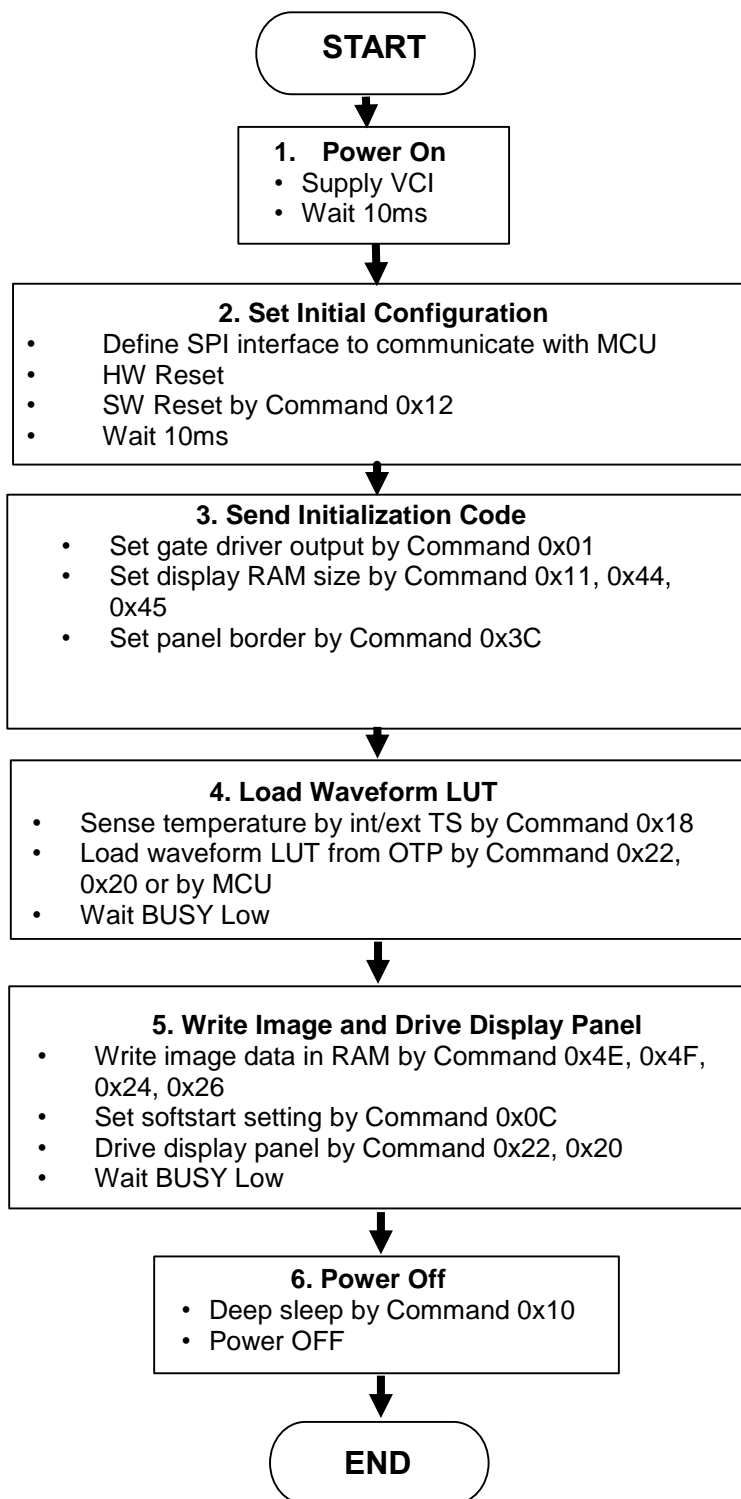


Figure 9-1: Operation flow to drive display panel

10 Absolute Maximum Rating

Table 10-1 : Maximum Ratings

Symbol	Parameter	Rating	Unit
V _{CI}	Logic supply voltage	-0.5 to +6.0	V
V _{IN}	Logic Input voltage	-0.5 to V _{DDIO} +0.5	V
V _{OUT}	Logic Output voltage	-0.5 to V _{DDIO} +0.5	V
T _{OPR}	Operation temperature range	-40 to +85	°C
T _{STG}	Storage temperature range	-65 to +150	°C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{CI} be constrained to the range V_{SS} < V_{CI}. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DDIO}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

11 Electrical Characteristics

The following specifications apply for: V_{SS}=0V, V_{CI}=3.0V, V_{DD}=1.8V, T_{OPR}=25°C.

Table 11-1: DC Characteristics

Symbol	Parameter	Applicable pin	Test Condition	Min.	Typ.	Max.	Unit
V _{CI}	V _{CI} operation voltage	V _{CI}		2.2	3.0	3.7	V
V _{DD}	V _{DD} operation voltage	V _{DD}		1.7	1.8	1.9	V
V _{COM_DC}	V _{COM_DC} output voltage	V _{COM}		-3.0		-0.2	V
dV _{COM_DC}	V _{COM_DC} output voltage deviation	V _{COM}		-200		200	mV
V _{COM_AC}	V _{COM_AC} output voltage	V _{COM}		V _{SL} + V _{COM_DC}	V _{COM_DC}	V _{SH1} + V _{COM_DC}	V
V _{GATE}	Gate output voltage	G0~G295		-20		+20	V
V _{GATE(p-p)}	Gate output peak to peak voltage	G0~G295				40	V
V _{SH1}	Positive Source output voltage	V _{SH1}		+2.4	+15	+17	V
dV _{SH1}	V _{SH1} output voltage deviation	V _{SH1}	From 2.4V to 8.8V	-100		100	mV
			From 9.0V to 17V	-200		200	mV
V _{SH2}	Positive Source output voltage	V _{SH2}		+2.4	+5	+17	V
dV _{SH2}	V _{SH2} output voltage deviation	V _{SH2}	From 2.4V to 8.8V	-100		100	mV
			From 9.0V to 17V	-200		200	mV
V _{SL}	Negative Source output voltage	V _{SL}		-17	-15	-9	V
dV _{SL}	V _{SL} output voltage deviation	V _{SL}		-200		200	mV
V _{IH}	High level input voltage	SDA, SCL, CS#, D/C#, RES#, BS1, M/S#, EXT _{VDD} , CL		0.8V _{DDIO}			V
V _{IL}	Low level input voltage					0.2V _{DDIO}	V
V _{OH}	High level output voltage	SDA, BUSY, CL	I _{OH} = -100uA	0.9V _{DDIO}			V
V _{OL}	Low level output voltage		I _{OL} = 100uA			0.1V _{DDIO}	V
V _{PP}	OTP Program voltage	V _{PP}		7.25	7.5	7.75	V

Symbol	Parameter	Applicable pin	Test Condition	Min.	Typ.	Max.	Unit
Isip_VCI	Sleep mode current	VCI	- DC/DC off - No clock - No output load - MCU interface access - RAM data access		20	35	uA
Idslp_VCI1	Current of deep sleep mode 1	VCI	- DC/DC off - No clock - No output load - No MCU interface access - Retain RAM data but cannot access the RAM		1	3	uA
Idslp_VCI2	Current of deep sleep mode 2	VCI	- DC/DC off - No clock - No output load - No MCU interface access - Cannot retain RAM data		0.7	3	uA
Iopr_VCI	Operating Mode current	VCI	VCI=3.0V		1000		uA
V _{GH}	Operating Mode Output Voltage	VGH	Enable Clock and Analog by Master Activation Command VGH=20V VGL=-VGH VSH1=15V VSH2=5V VSL=-15V VCOM = -2V	19.5	20	20.5	V
V _{SH1}		VSH1		14.8	15	15.2	V
V _{SH2}		VSH2		4.9	5	5.1	V
V _{SL}		VSL		-15.2	-15	-14.8	V
V _{COM}		VCOM		-2.2	-2	-1.8	V
					No waveform transitions. No loading. No RAM read/write No OTP read /write		

Table 11-2: Regulators Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
IVSH	VSH1 current	VSH1 = +15V	VSH1			800	uA
IVSH1	VSH2 current	VSH2 = +5V	VSH2			800	uA
IVSL	VSL current	VSL = -15V	VSL			800	uA
IVCOM	VCOM current	VCOM = -2V	VCOM			100	uA

12 AC Characteristics

12.1.1 Serial Peripheral Interface

The following specifications apply for: VDDIO - VSS = 2.2V to 3.7V, T_{OPR} = 25°C, CL=20pF

Table 12-1 : Serial Peripheral Interface Timing Characteristics

Write mode

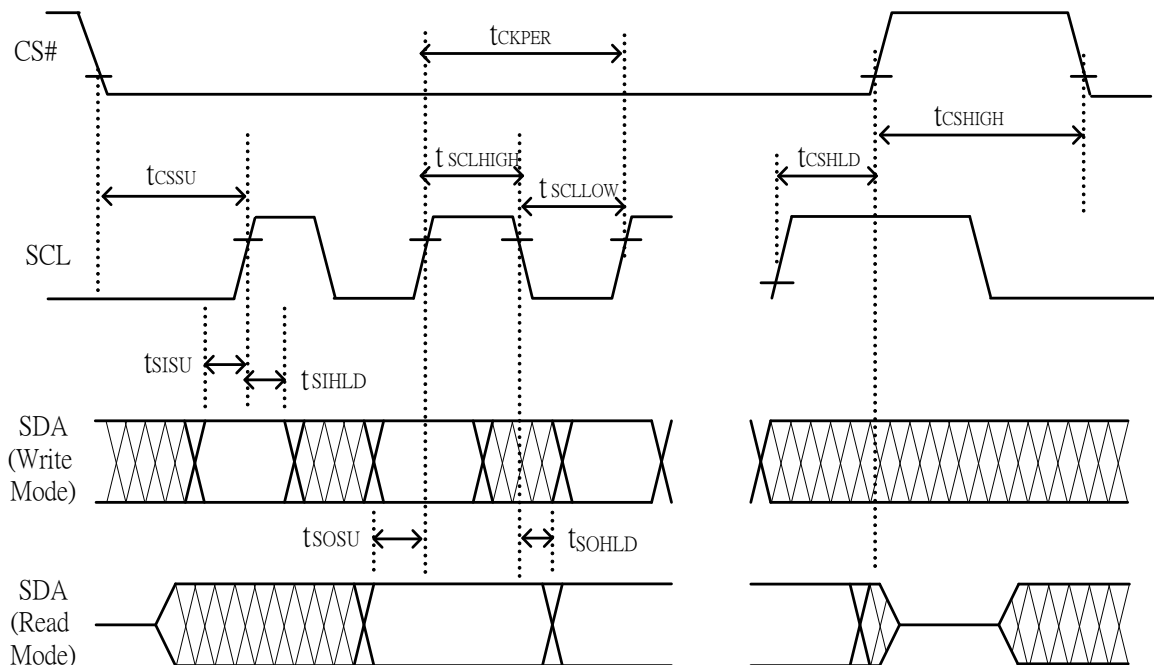
Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL frequency (Write Mode)			20	MHz
t _{CSSU}	Time CS# has to be low before the first rising edge of SCLK	20			ns
t _{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	20			ns
t _{CSHIGH}	Time CS# has to remain high between two transfers	100			ns
t _{SCLHIGH}	Part of the clock period where SCL has to remain high	25			ns
t _{SCLLOW}	Part of the clock period where SCL has to remain low	25			ns
t _{SISU}	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
t _{SIHLD}	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL frequency (Read Mode)			2.5	MHz
t _{CSSU}	Time CS# has to be low before the first rising edge of SCLK	100			ns
t _{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	50			ns
t _{CSHIGH}	Time CS# has to remain high between two transfers	250			ns
t _{SCLHIGH}	Part of the clock period where SCL has to remain high	180			ns
t _{SCLLOW}	Part of the clock period where SCL has to remain low	180			ns
t _{SOSU}	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
t _{SOHLD}	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

Note: All timings are based on 20% to 80% of VDDIO-VSS

Figure 12-1: SPI timing diagram



13 Application Circuit

Figure 13-1: Schematic of SSD1675B application circuit

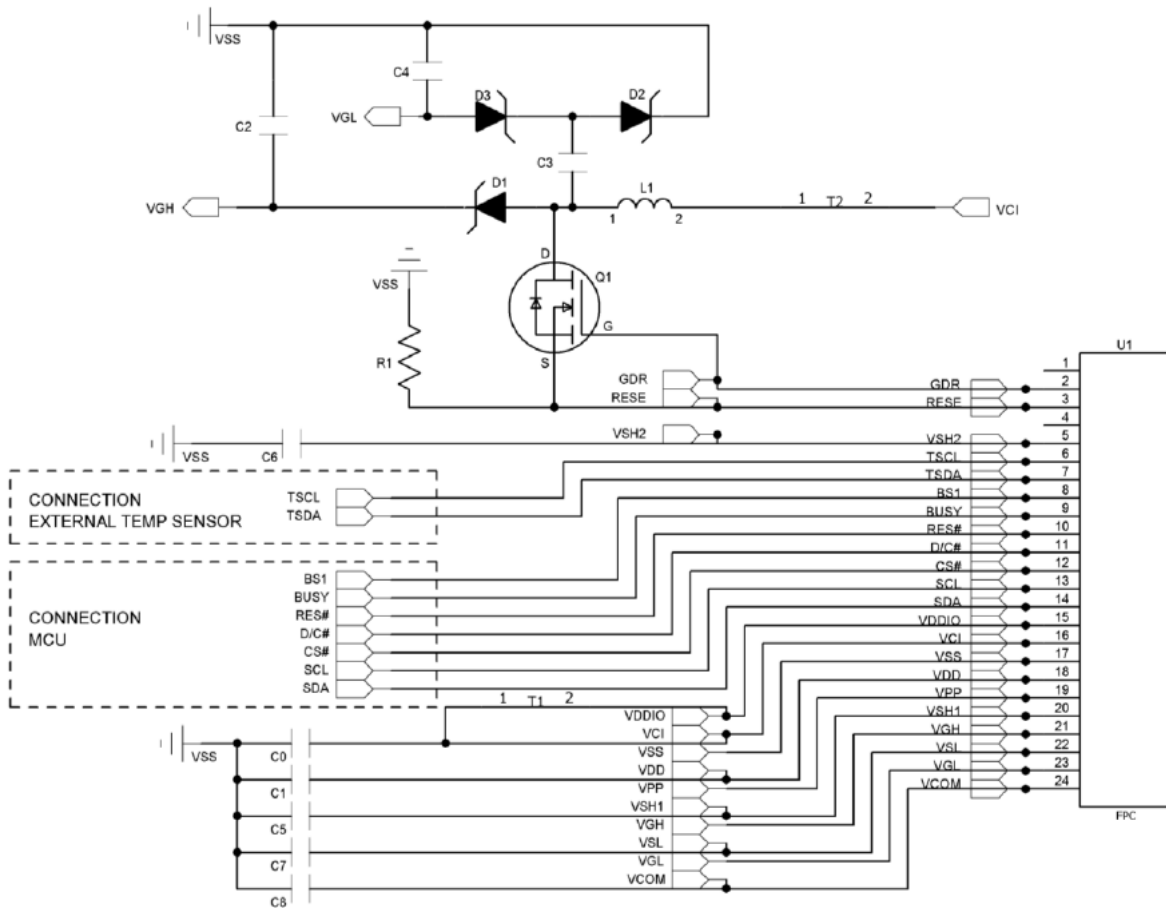


Table 13-1: Component list for SSD1675B application circuit

Part Name	Value	Requirements/Reference part
C0-C1	1uF	0603; X5R/X7R; Voltage Rating: 6V or 25V
C2-C7	1uF	0805; X5R/X7R; Voltage Rating: 25V
C8	1uF	0805; X7R; Voltage Rating: 25V 0603: 1) Samsung - CL10B105KA8NNNC 2) Taiyo – TMK107BJ105KA-T 3) TDK - C1608X7R1E105K7L Note: Effective capacitance > 0.35uF @ 18V DC bias
R1	2.2 Ohm	0805; 1%
D1-D3	Diode	MBR0530 1) Reverse DC voltage = 30V (Max) 2) Io = 500mA 3) Forward voltage = 430mV (Max)
Q1	NMOS	Si1304BDL/NX3008NBK 1) Drain-Source breakdown voltage = 30V(min) 2) Vgs(th) = 0.9V (Typ), 1.3V (Max) 3) Rds on ≤ 2.1Ω @ Vgs = 2.5V
L1	47uH	CDRH2D18/ LDNP-470NC Io = 500 (Max)
U1	0.5mm ZIF socket	24pins, 0.5mm pitch

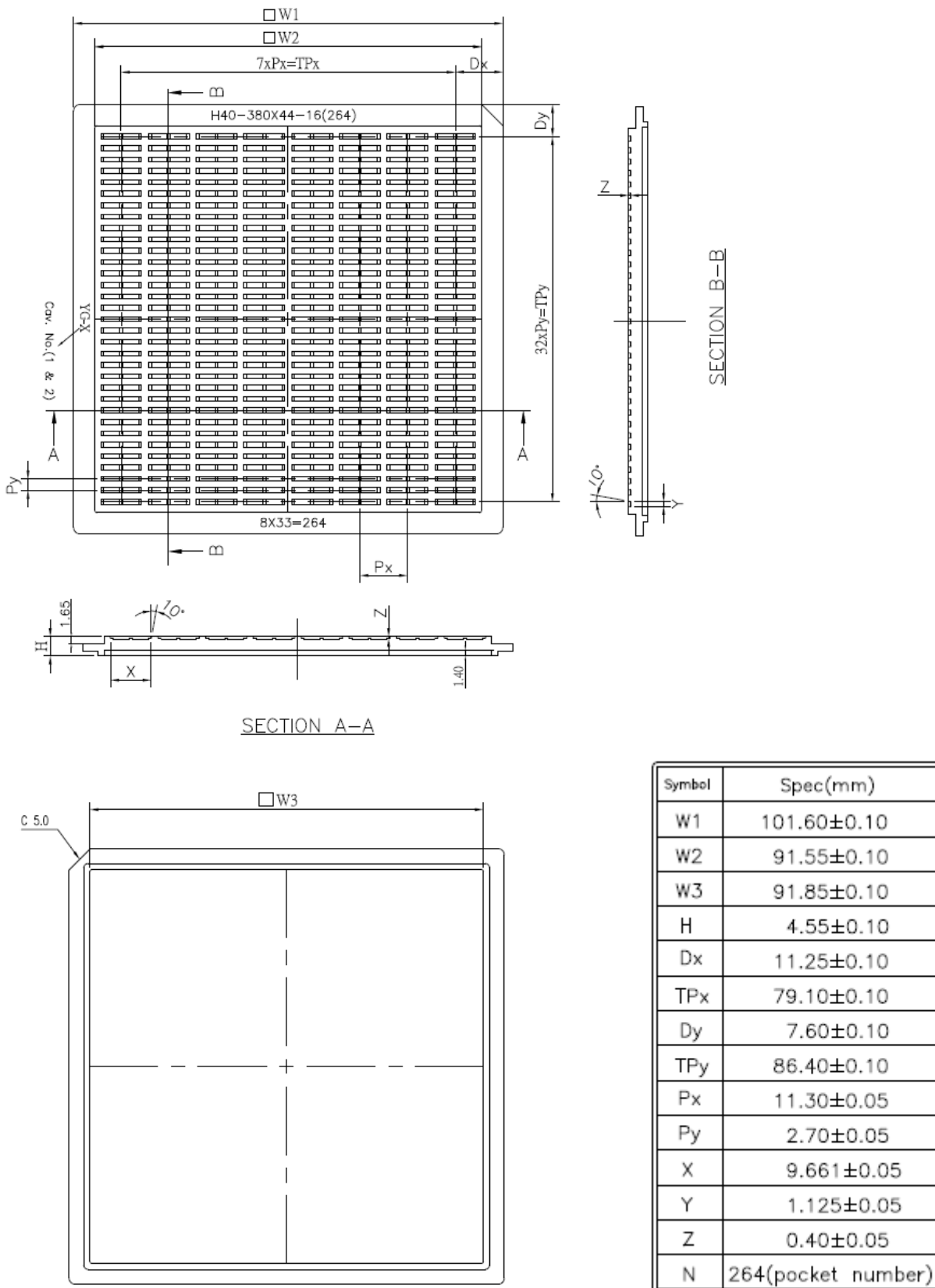
Remarks:

- 1) The recommended component value and reference part in Table 13-1 is subject to change depending on panel loading.
- 2) Customer is required to review if the selected component value and part is suitable for their application.

14 Package Information

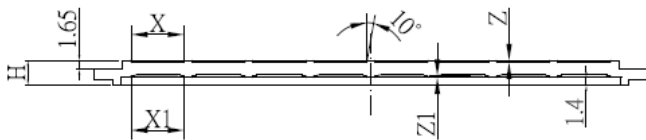
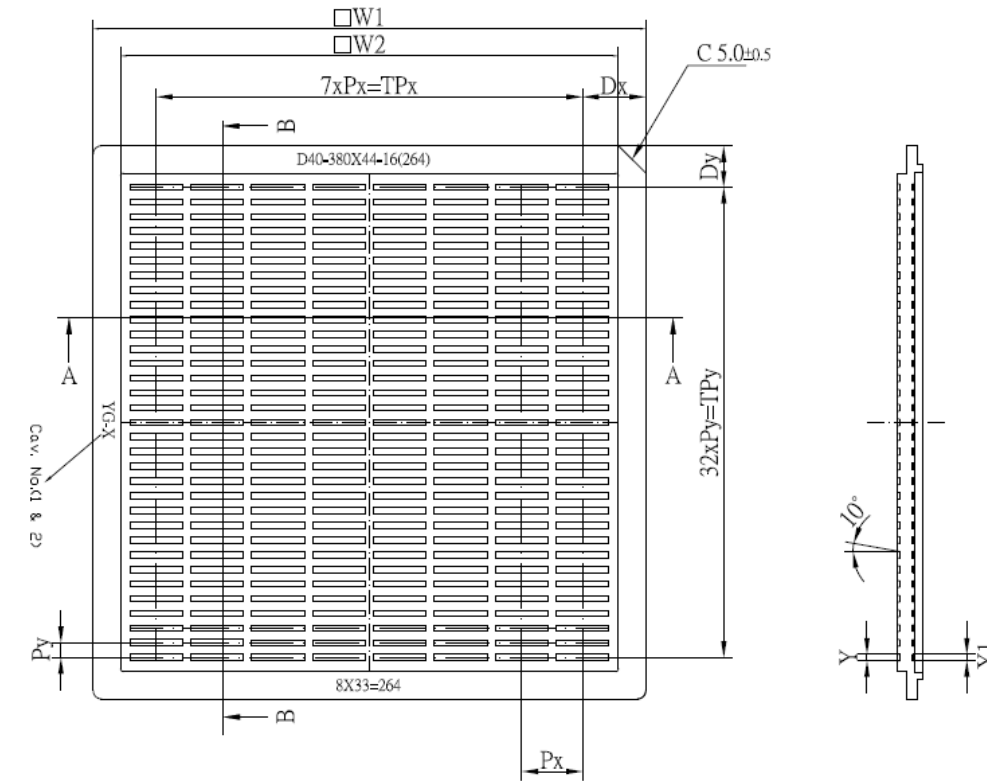
14.1.1 Die Tray Dimensions for SSD1675BZ

Figure 14-1 : SSD1675BZ die tray information (unit: mm)

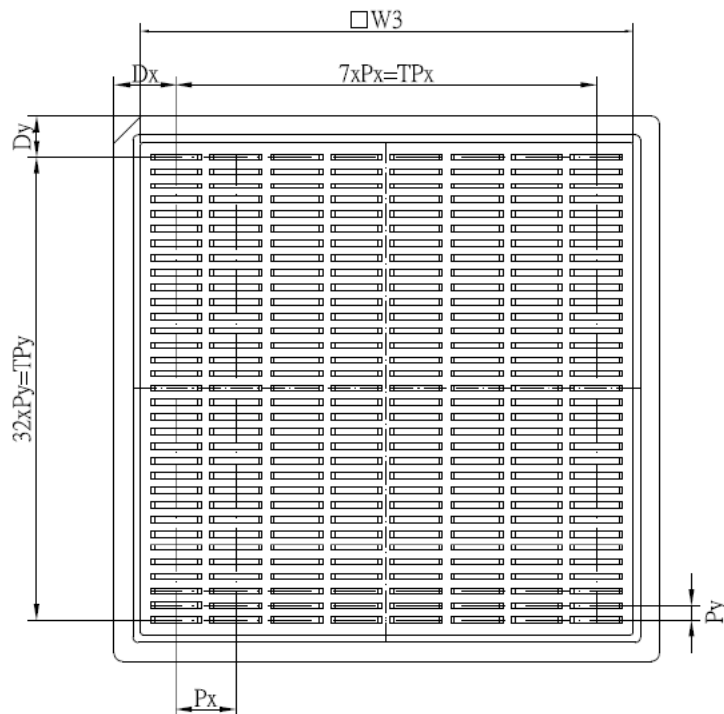


14.1.2 Die Tray Dimensions for SSD1675BZ8

Figure 14-2 : SSD1675BZ8 die tray information (unit: mm)



SECTION A-A



Symbol	Spec (mm)
W1	101.60±0.10
W2	91.55±0.10
W3	91.75±0.10
H	4.55±0.10
Px	11.20±0.05
Py	2.70±0.05
Dx	11.60±0.05
TPx	78.40±0.10
Dy	7.60±0.05
TPy	86.40±0.10
X	9.661±0.05
Y	1.125±0.05
Z	0.40±0.05
X1	9.661±0.05
Y1	1.125±0.05
Z1	0.35±0.05
N	8x33=264 (pocket number)

Solomon Systech reserves the right to make changes without notice to any products herein. Solomon Systech makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Solomon Systech assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any, and all, liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typical" must be validated for each customer application by the customer's technical experts. Solomon Systech does not convey any license under its patent rights nor the rights of others. Solomon Systech products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Solomon Systech product could create a situation where personal injury or death may occur. Should Buyer purchase or use Solomon Systech products for any such unintended or unauthorized application, Buyer shall indemnify and hold Solomon Systech and its offices, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Solomon Systech was negligent regarding the design or manufacture of the part.



The product(s) listed in this datasheet comply with Directive 2011/65/EU of the European Parliament and of the council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People's Republic of China Electronic Industry Standard GB/T 26572-2011 "Requirements for concentration limits for certain hazardous substances in electronic information products (电子电器产品中限用物質的限用要求)". Hazardous Substances test report is available upon request.

<http://www.solomon-systech.com>