SSD1677

Advance Information

960 Source x 680 Gate Red/Black/White Active Matrix EPD Display Driver with Controller

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FIGURES

1 General Description

The SSD1677 is an Active Matrix EPD Display Driver with Controller which can support Red/Black/White.
It consists of 960 source outputs, 680 gate outputs, 1 VCOM and 1 VBD for border that can support a maximum display resolution 960x680.

The SSD1677 embeds booster, regulators and oscillator. Data/Commands are sent from general MCU through the hardware selectable Serial peripheral.

2 Features

- Design for dot matrix type active matrix EPD display
- Support Red/Black/White mono color
- Resolution: 960 source outputs; 680 gate outputs; 1 VCOM; 1VBD for border
- Power supply:
  - VCI: 2.2 to 3.3V
  - VDDIO: Connect to VCI
  - VDD: 1.8V, regulate from VCI supply
- On chip display RAM
  - Mono B/W: 960x680 bits
  - Mono Red: 960x680 bits
- On-chip booster and regulator for generating VCOM, Gate and Source driving voltage
- Gate driving output voltage:
  - 2 levels output (VGH, VGL)
  - Max 40Vp-p
  - VGH: 15V to 20V; VGL: -VGH
  - Voltage adjustment step: 500mV
- Source / VBD driving output voltage:
  - 4 levels output (VSH1, VSS, VSL, and VSH2)

• VSH1: 9V to 17V (200mV for 9V to 17V) • VSH2: 2.4V to 17V (Voltage step: 100mV for 2.4V to 8.8V, 200mV for 8.8V to 17V) • VSL: -9V to -17V (Voltage step: 500mV)
•

  - VCOM output voltage

DCVCOM	ACVCOM
-4V to -0.1V in 100mV resolution	• 3 levels output ➢ VSH1+DCVCOM, DCVCOM, VSL+DCVCOM

- VGH, VGL, VSH1, VSH2, VSL can be connected to external power supply
- Built-in VCOM sensing
- On-chip oscillator
- Programmable output waveform:
  - 40 phases (4 phases/group, 10 groups with repeat function)
  - 1 to 256 times for repeat count
  - Max. 255 frame/phase
- On-chip OTP to store the waveform settings and parameters:
  - 34 sets of waveform setting (WS) including waveform LUT, gate/source voltage and frame rate
  - 34 sets of Temperature Range (TR)
  - VCOM value
  - Waveform version
  - Module identification/User ID
- Embedded OTP to store the initial code setting

- External or internal generated voltage for burning OTP
- Read OTP function and Built-in CRC checking method for waveform setting and temperature range in OTP
- Support Low voltage detect for supply voltage
- Support High voltage ready detect for driving voltage with looping
- Support black/white mono dithering feature
- Support panel break diagnostic
- Support display partial update
- Auto write RAM command for regular pattern
- Internal Temperature Sensor, -25 to 50 degC: accuracy +/- 2degC / 9- bit status
- I2C Single Master Interface to communicate with external temperature sensor
- MCU interface: SPI serial peripheral, Maximum 20MHz for write
- Low current consumption for operation and sleep mode
- Available in COG package

3 ORDERING INFORMATION

Table 3-1 : Ordering Information

Ordering Part Number	Package Form	Remark
SSD1677Z	Gold Bump Die	Bump Face Up On Waffle pack Die thickness: 300um Bump height: 12um
SSD1677Z8	Gold Bump Die	Bump Face Down On Waffle pack Die thickness: 300um Bump height: 12um

4 Block Diagram

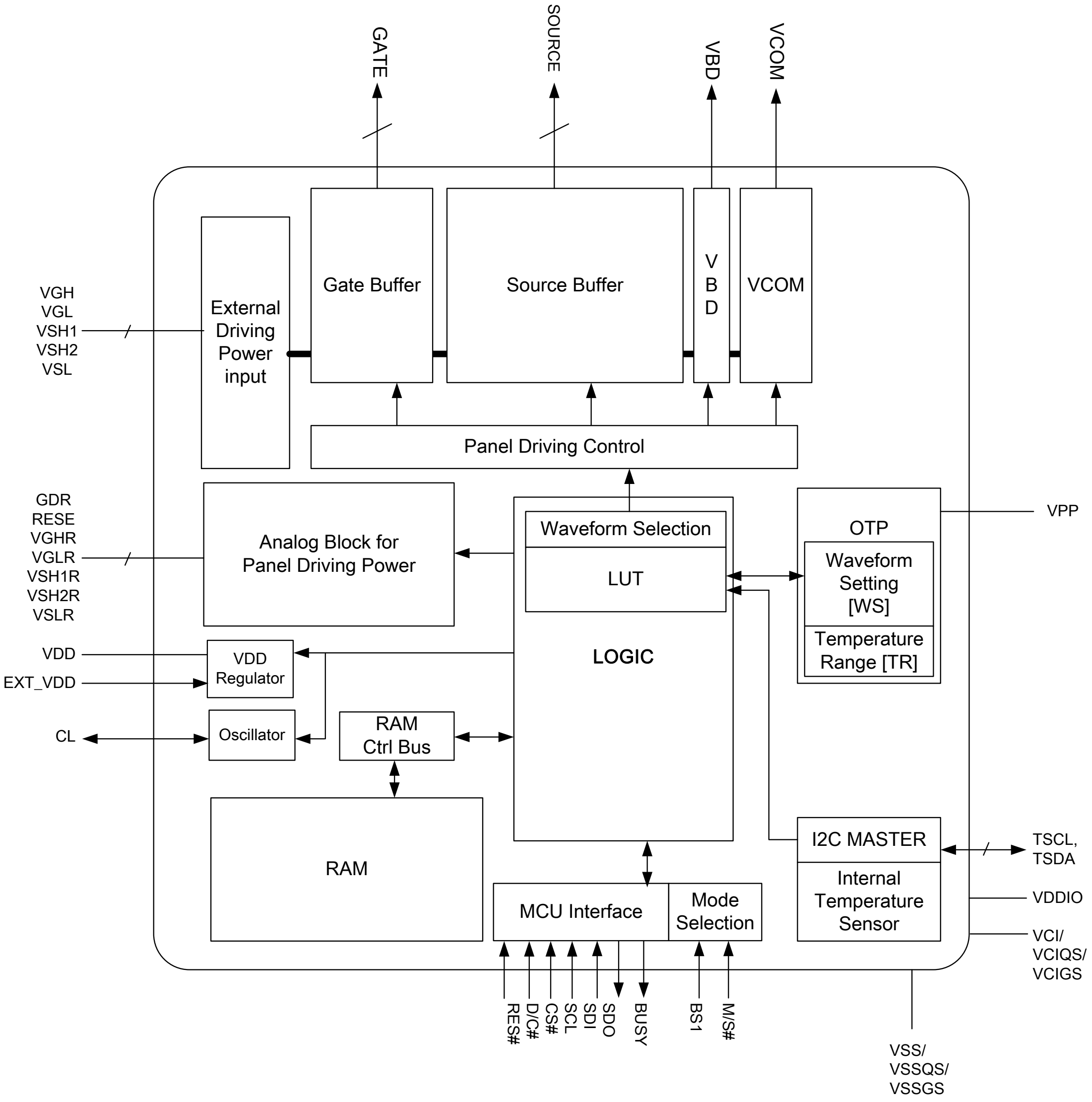


Figure 4-1 : SSD1677 Block Diagram

5 PIN DESCRIPTION

Key:

I = Input
O =Output
IO = Bi-directional (input/output)
P = Power pin
C = Capacitor Pin
NC = Not Connected

Table 5-1: Power Supply Pins

Name	Type	Connect to	Function	Description	When not in use
VCI	P	Power Supply	Power Supply	This pin is Power input pin for the chip.	-
VCIGS	P	Power Supply	Power Supply	This pin is Power input pin for the chip. - Connect to VCI in the application circuit.	-
VCIQS	P	Power Supply	Power Supply	This pin is Power input pin for the chip. - Connect to VCI in the application circuit.	-
VDDIO	P	Power Supply	Power for interface logic pins	This pin is Power input pin for the Interface. - Connect to VCI in the application circuit.	-
VDD	P	Capacitor	Regulator output	This pin is Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS under all circumstances.	-
EXTVDD	I	VSS	Regulator bypass	This pin is VDD regulator bypass pin. EXTVDD should be connected to VSS in the application circuit.	-
VSS	P	VSS	GND	This pin is Ground pin	-
VSSGS	P	VSS	GND	This pin is Ground pin. - Connect to VSS in the application circuit.	-
VSSQS	P	VSS	GND	This pin is Ground pin. - Connect to VSS in the application circuit.	-
VPP	P	Power Supply	OTP power	This pin is Power Supply for OTP Programming.	Open

Table 5-2: Interface Logic Pins

<table>
<tr><th>Name</th><th>Type</th><th>Connect to</th><th>Function</th><th>Description</th><th>When not in use</th></tr>
<tr><td>SCL</td><td>I</td><td>MPU</td><td>Data Bus</td><td>This pin is Serial clock pin for interface:
Refer to Session 6.1 - MCU Interface.</td><td>-</td></tr>
<tr><td>SDI</td><td>I</td><td rowspan="2">MPU</td><td rowspan="2">Data Bus</td><td rowspan="2">This pin is Serial data pin for interface:
Refer to Session 6.1 - MCU Interface.</td><td>-</td></tr>
<tr><td>SDO</td><td>O</td><td>Open</td></tr>
<tr><td>CS#</td><td>I</td><td>MPU</td><td>Logic Control</td><td>This pin is the chip select input connecting to the MCU.
Refer to Session 6.1 - MCU Interface.</td><td>VDDIO or VSS</td></tr>
<tr><td>D/C#</td><td>I</td><td>MPU</td><td>Logic Control</td><td>This pin is Data/Command control pin connecting to the MCU. Refer to Session 6.1- MCU Interface.</td><td>VDDIO or VSS</td></tr>
<tr><td>RES#</td><td>I</td><td>MPU</td><td>System Reset</td><td>This pin is reset signal input.
Active Low.</td><td>-</td></tr>
<tr><td>BUSY</td><td>O</td><td>MPU</td><td>Device Busy Signal</td><td>This pin is Busy state output pin
When Busy is High, the operation of the chip should not be interrupted, and command should not be sent.
For example., The chip would put Busy pin High when
- Outputting display waveform; or
- Programming with OTP
- Communicating with digital temperature sensor</td><td>Open</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>BS1</td><td>I</td><td>VDDIO/VSS</td><td>MCU Interface Mode Selection</td><td>This pin is for selecting 3-wire or 4-wire SPI bus.
<table>
<tr><td>BS1</td><td>MCU Interface</td></tr>
<tr><td>L</td><td>4-wire SPI</td></tr>
<tr><td>H</td><td>3-wire SPI(9 bits SPI)</td></tr>
</table></td><td>-</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>M/S#</td><td>I</td><td>VDDIO</td><td>Reserved for Testing</td><td>This pin is reserved pin and should be connected to VDDIO.</td><td>-</td></tr>
<tr><td>CL</td><td>I/O</td><td>NC</td><td>Clock signal</td><td>This is the clock signal pin. It should be left open in application.</td><td>Open</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>TSDA</td><td>I/O</td><td>Temperature sensor SDA</td><td>Interface to Digital Temp. Sensor</td><td>This pin is I^2C Interface to digital temperature sensor Data pin.
External pull up resistor is required when connecting to I^2C slave.</td><td>Open</td></tr>
<tr><td>TSCL</td><td>O</td><td>Temperature sensor SCL</td><td>Interface to Digital Temp. Sensor</td><td>This pin is I^2C Interface to digital temperature sensor Clock pin.
External pull up resistor is required when connecting to I^2C slave.</td><td>Open</td></tr>
</table>

Table 5-3: Analog Pins

Name	Type	Connect to	Function	Description	When not in use
GDR	O	POWER MOSFET Driver Control	VGHR, VGLR Generation	This pin is N-Channel MOSFET gate drive control pin.	-
RESE	I	Booster Control Input		This pin is Current sense input pin for the control Loop.	-
VGHR	C	Stabilizing capacitor		This pin is Positive Gate driving voltage regulation. Connect a stabilizing capacitor between VGHR and VSS in the application circuit.	Open
VGLR	C	Stabilizing capacitor		This pin is Negative Gate driving voltage regulation. Connect a stabilizing capacitor between VGLR and VSS in the application circuit.	Open
VSH1R	C	Stabilizing capacitor	VSH1R, VSH2R, VSLR Generation	This pin is Positive Source driving voltage regulation - VSH1R. Connect a stabilizing capacitor between VSH1R and VSS in the application circuit.	Open
VSH2R	C	Stabilizing capacitor		This pin is Positive Source driving voltage regulation – VSH2R. Connect a stabilizing capacitor between VSH2R and VSS in the application circuit.	Open
VSLR	C	Stabilizing capacitor		This pin is Negative Source driving voltage regulation. Connect a stabilizing capacitor between VSLR and VSS in the application circuit.	Open
VGH	P	VGH supply		This pin is Positive Gate driving voltage.	VGHR
VGL	P	VGL supply		This pin is Negative Gate driving voltage.	VGLR
VSH1	P	VSH1 supply		This pin is Positive Source driving voltage - VSH1.	VSH1R
VSH2	P	VSH2 supply		This pin is Positive Source driving voltage - VSH2.	VSH2R
VSL	P	VSL supply		This pin is Negative Source driving voltage.	VSLR

Table 5-4: External Power Supply Pins

Name	Type	Connect to	Function	Description	When not in use
VGH	P	VGH supply	Analog Pins for External Power Supply	This pin is Positive Gate driving voltage.	VGHR
VGL	P	VGL supply		This pin is Negative Gate driving voltage.	VGLR
VSH1	P	VSH1 supply		This pin is Positive Source driving voltage - VSH1.	VSH1R
VSH2	P	VSH2 supply		This pin is Positive Source driving voltage - VSH2.	VSH2R
VSL	P	VSL supply		This pin is Negative Source driving voltage.	VSLR

Table 5-5: Driver Output Pins

Name	Type	Connect to	Function	Description	When not in use
S [959:0]	O	Panel	Source driving signal	These pins are Source output pin.	Open
G [679:0]	O	Panel	Gate driving signal	These pins are Gate output pin.	Open
VBD	O	Panel	Border driving signal	This pin is Border output pin.	Open
VCOM	C	Panel/ Stabilizing capacitor	VCOM Generation	This pin is VCOM driving voltage Connect a stabilizing capacitor between VCOM and VSS in the application circuit.	-

Table 5-6: Miscellaneous Pins

Name	Type	Connect to	Function	Description	When not in use
RSV	NC	NC	Reserved	This pin is a reserved pin, keep floating	Open
DP[0:33]	I	VSS	Reserved	These pins are reserved pins, connect to VSS.	VSS
TP1,TP2, TP3,TP4, TP5,TP6, TP7,TP8, TP9	NC	NC	Reserved for Testing	Reserved pins. - Keep open. - Don’t connect to other NC pins and test pins including TP1,TP2,TP3,TP4,TP5,TP6, TP7,TP8 and TP9	Open
TIN	I	NC	Reserved for Testing	Reserved pins. - Keep open.	Open
TPE	O	NC			Open

6 Functional Block Description

6.1 MCU Interface

6.1.1 MCU Interface selection

SSD1677 can support 4-wire or 3-wire serial peripheral MCU interface, which is pin selectable by BS1 pin. The interface pin assignment for different MCU interfaces is shown in Table 6-1.

Table 6-1: Interface pin assignment for different MCU interfaces

	Pin Name						
MCU Interface	**BS1**	**RES#**	**CS#**	**D/C#**	**SCL**	**SDI**	**SDO**
4-wire serial peripheral interface (SPI)	L	RES#	CS#	DC#	SCL	SDA	
3-wire serial peripheral interface (SPI) – 9 bits SPI	H	RES#	CS#	L	SCL	SDA	

Note:
(1) L is connected to V_{SS} and H is connected to V_{DDIO}
(2) SDI and SDO are connected to be SDA pin for bi-directional data access

6.1.2 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data input SDI, D/C# and CS#. The control pins status in 4-wire SPI in writing command/data is shown in Table 6-2 and the write procedure in 4-wire SPI is shown in Figure 6-1.

Table 6-2 : Control pins status of 4-wire SPI

Function	**SCL pin**	**SDI pin**	**D/C# pin**	**CS# pin**
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

Note:
(1) L is connected to V_{SS} and H is connected to V_{DDIO}
(2) ↑ stands for rising edge of signal

SDI is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

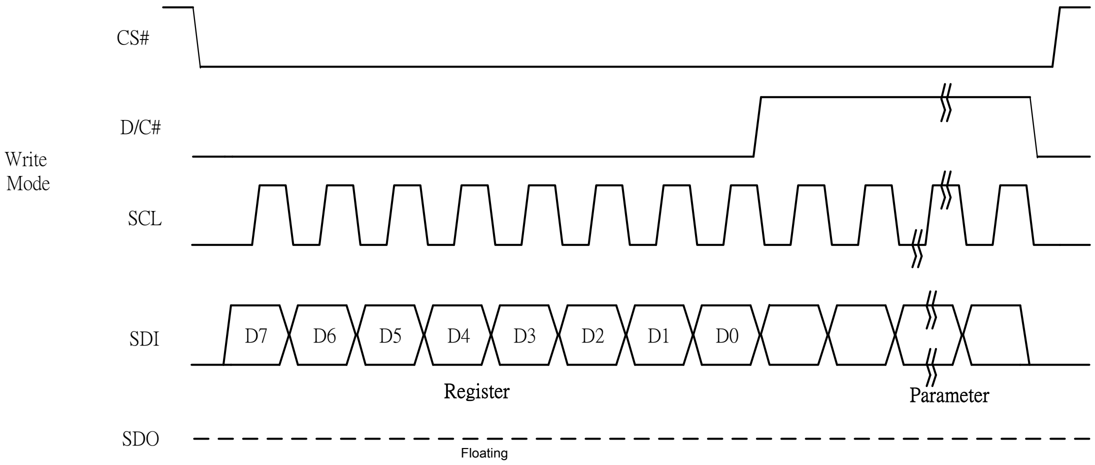


Figure 6-1 : Write procedure in 4-wire SPI mode

In the read operation, after CS# is pulled low, the first byte sent is command byte, D/C# is pulled low. After command byte sent, the following byte(s) read are data byte(s), so D/C# bit is then pulled high. An 8-bit data will be shifted out on every clock falling edge. The serial data output SDO bit shifting sequence is D7, D6, to D0 bit. Figure 6-2 shows the read procedure in 4-wire SPI.

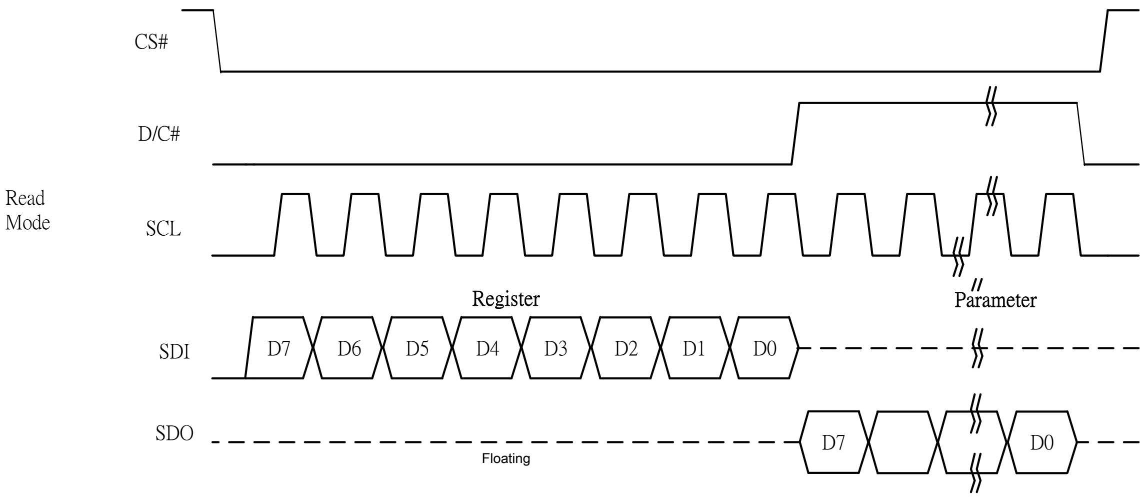


Figure 6-2 : Read procedure in 4-wire SPI mode

6.1.3 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data input SDI, and CS#. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 6-3.

In the write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1, the following byte is data. Table 6-3 shows the write procedure in 3-wire SPI

Table 6-3 : Control pins status of 3-wire SPI

Function	SCL pin	SDI pin	D/C# pin	CS# pin
Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

Note:

(1) L is connected to V_{SS} and H is connected to V_{DDIO}

(2) ↑ stands for rising edge of signal

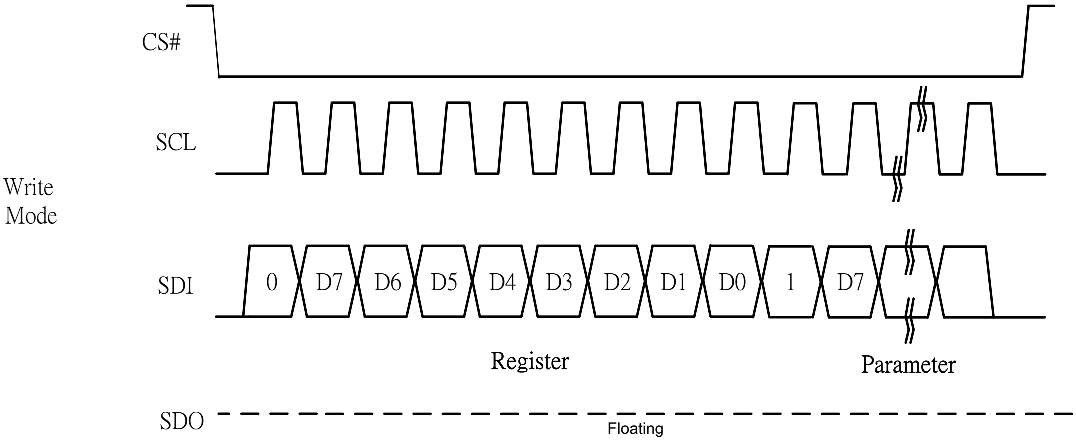


Figure 6-3 : Write procedure in 3-wire SPI

In the read operation, serial data are transferred in the unit of 9 bits. After CS# pull low, the first byte is command byte, the D/C# bit is as 0 and following with the register byte. After command byte send, the following byte(s) are data byte(s), with D/C# bit is 1. After D/C# bit sending from MCU, an 8-bit data will be shifted out on every clock falling edge. The serial data output SDO bit shifting sequence is D7, D6, to D0 bit. Figure 6-4 shows the read procedure in 3-wire SPI.

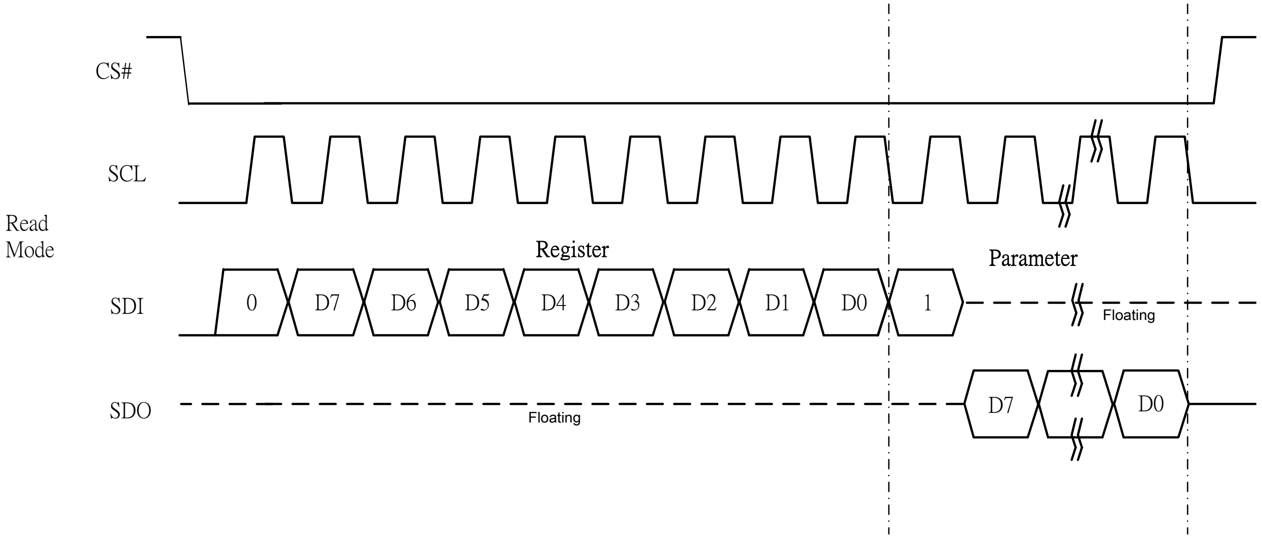


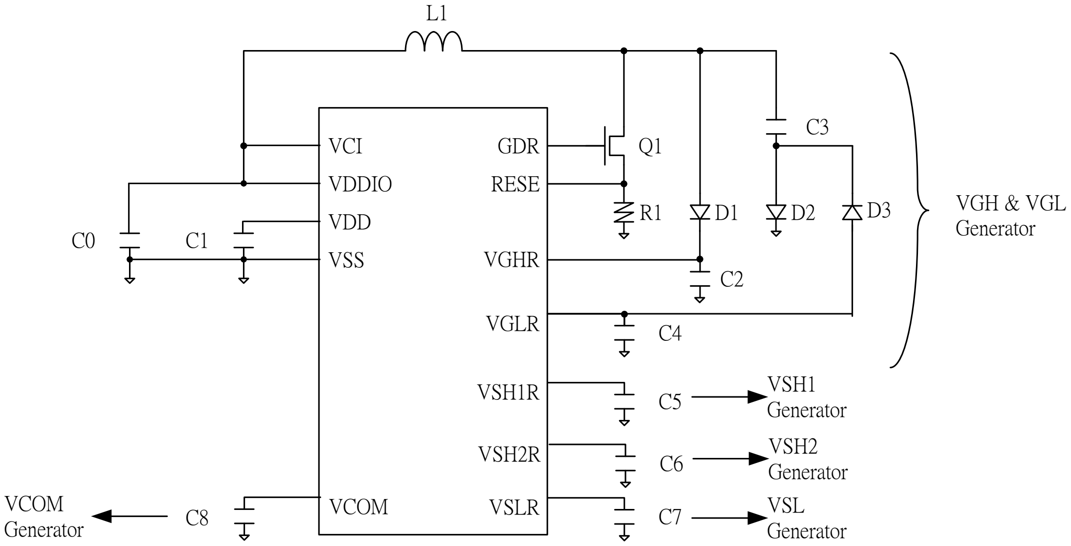
Figure 6-4 : Read procedure in 3-wire SPI mode

6.2 Oscillator

The oscillator module generates the clock reference for waveform timing and analog operations.

6.3 Booster & Regulator

A voltage generation system is included in the driver. It provides all necessary driving voltages required for an AMEPD panel including VGHR, VGLR, VSH1R, VSH2R, VSLR and VCOM. External application circuit is needed to make the on-chip booster & regulator circuit work properly.



With internal power mode, it needs connecting VGHR to VGH, VGLR to VGL, VSH1R to VSH1, VSH2R to VSH2 and VSLR to VSL.

SSD1677 support external Gate power [VGH/VGL] and Source power [VSH1/VSH2/VSL]. When external power is connected, VGHR, VGLR, VSH1R, VSH2R and VSL are floating.

6.4 VCOM Sensing

This functional block provides the scheme to sense and set VCOM. The sensed value can also be programmed into OTP.

6.5 RAM

The on-chip display RAM is holding the image data.
1 set of RAM is built for Mono B/W. The RAM size is 960x680 bits.
1 set of RAM is built for Mono Red. The RAM size is 960x680 bits.

Table 6-4 : RAM bit and LUT mapping for 3-color display

Data bit in R RAM	Data bit in B/W RAM	Image Color	LUT
0	0	Black	LUT 0 for driving Black
0	1	White	LUT 1 for driving White
1	0	Red	LUT 2 for driving Red
1	1	Red	LUT 3 = LUT2

Table 6-5 : RAM bit and LUT mapping for black/white display

Data bit in R RAM	Data bit in B/W RAM	Image Color	LUT
0	0	Black	LUT 0 for driving Black
0	1	White	LUT 1 for driving White
1	0	Black	LUT 2 = LUT0
1	1	White	LUT 3 = LUT1

6.6 Programmable Waveform for Gate, Source and VCOM

SSD1677 provides a high flexibility to program the driving waveform. Figure 6-5 illustrates the programmable waveform format for Gate, Source and VCOM.

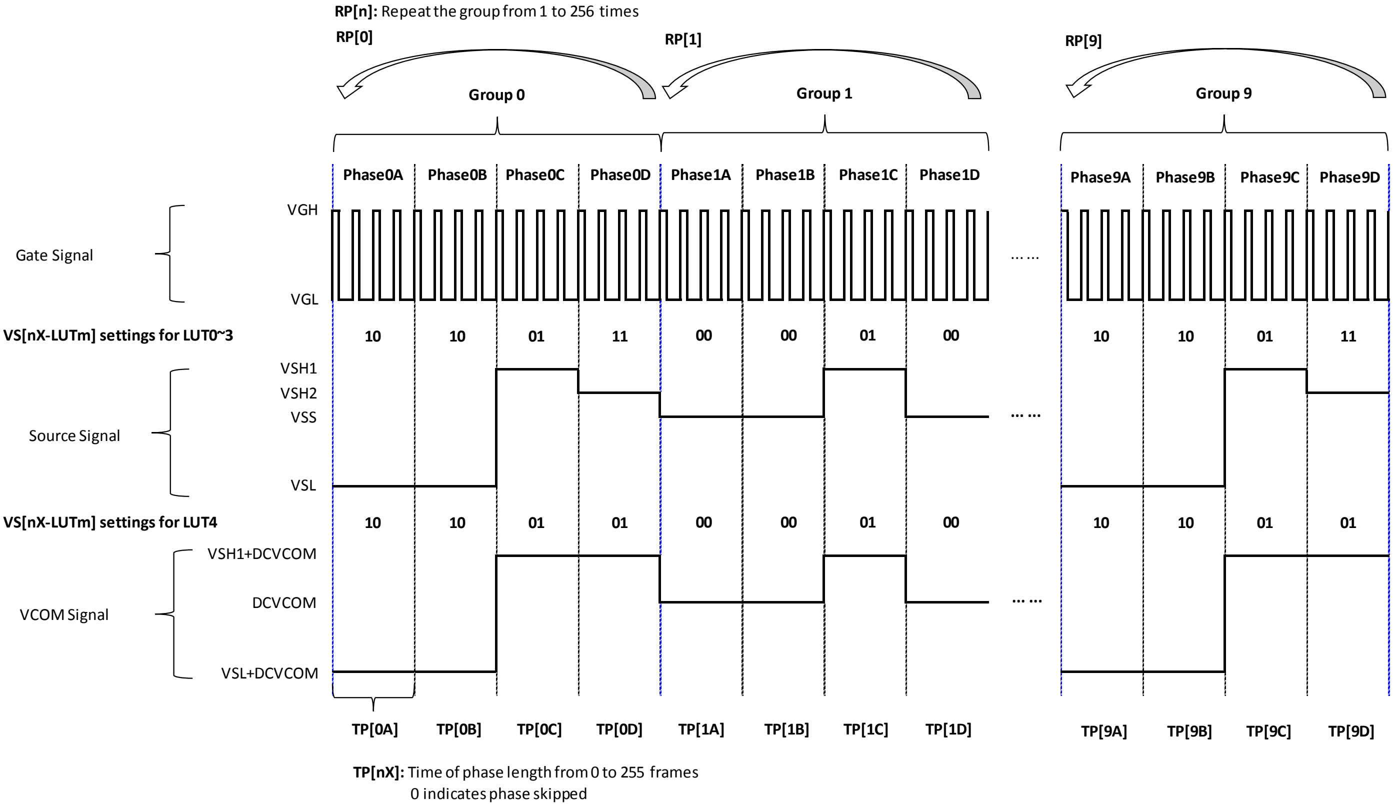


Figure 6-5 : Gate waveform and Programmable Source and VCOM waveform illustration

In the programmable waveform for Source and VCOM, there are 10 groups (Group0 to Group9) and each group has 4 phases (Phase A to Phase D). Totally, there are 40 phases. In addition, in each phase, the phase length (TP[nX]) can be set by number of frame from 0 to 255 frames. Also, each group can be repeated with repeat counting number (RP[n]) from 1 to 256 times. For the voltage, there is four levels for Source voltage (VSS, VSH1, VSH2, VSL) and three levels for VCOM voltage (DCVCOM, VSH1+DCVCOM, VSL+DCVOM).

The description of each parameter is as follows.

1) TP[nX] represents the phase length set by the number of frame.
- The range of TP[nX] is from 0 to 255.
- n represents the Group number from 0 to 9; X represents the phase number from A to D.
- When TP[nX] = 0, the phase is skipped. When TP[nX] = 1, the phase is 1 frame, and so on. The maximum phase length is 255 frame.

2) RP[n] represents the repeat counting number for the Group.
- The range of RP[n] is from 0 to 255.
- n represents the Group number from 0 to 9.
- RP[n] = 0 indicates that the repeat times =1, RP[n] = 1 indicates that the repeat times = 2, and so on. The maximum repeat times is 256.

3) VS[nX-LUTm] represents Source and VCOM voltage level which is used in each phase. Table 6-6 shows the voltage settings for source voltage and VCOM voltage.
- n represents the Group number from 0 to 9.
- m represents the LUT number from 0-4.

Table 6-6 : VS[nX-LUTm] settings for Source voltage and VCOM voltage

VS[nX-LUTm]	Source voltage	VCOM voltage
00	VSS	DCVCOM
01	VSH1	VSH1 + DCVCOM
10	VSL	VSL + DCVCOM
11	VSH2	N/A

6.7 Waveform Lookup Table (LUT)

As described in Section 6.6, parameters TP[nX], RP[n] and VS[nX-LUTm] are used to define the driving waveform. In the SSD1677, there are 112 bytes in the waveform lookup table to store LUT0, LUT1, LUT2, LUT3 and LUT4, gate voltage, source voltage and frame rate. The waveform LUT of a particular temperature range can be loaded from OTP or written by MCU.

- WS byte 0~104, the content of VS [n-XY], TP [n#], RP[n] and frame rate are defined by Register 0x32
- WS byte 105, the content of gate level, is the parameter defined by Register 0x03.
- WS byte 106~108, the content of source level, is the parameter defined by Register 0x04.
- WS byte 109, the content of VCOM level, is the parameter defined by Register 0x2C.
- WS byte 110~111, the contents are reserved.

The SSD1677 waveform LUT is shown in Figure 6-6.

	D7	D6	D5	D4	D3	D2	D1	D0
0	VS[0A-L0]		VS[0B-L0]		VS[0C-L0]		VS[0D-L0]	
1	VS[1A-L0]		VS[1B-L0]		VS[1C-L0]		VS[1D-L0]	
2	VS[2A-L0]		VS[2B-L0]		VS[2C-L0]		VS[2D-L0]	
3	VS[3A-L0]		VS[3B-L0]		VS[3C-L0]		VS[3D-L0]	
4	VS[4A-L0]		VS[4B-L0]		VS[4C-L0]		VS[4D-L0]	
5	VS[5A-L0]		VS[5B-L0]		VS[5C-L0]		VS[5D-L0]	
6	VS[6A-L0]		VS[6B-L0]		VS[6C-L0]		VS[6D-L0]	
7	VS[7A-L0]		VS[7B-L0]		VS[7C-L0]		VS[7D-L0]	
8	VS[8A-L0]		VS[8B-L0]		VS[8C-L0]		VS[8D-L0]	
9	VS[9A-L0]		VS[9B-L0]		VS[9C-L0]		VS[9D-L0]	
10	VS[0A-L1]		VS[0B-L1]		VS[0C-L1]		VS[0D-L1]	
11	VS[1A-L1]		VS[1B-L1]		VS[1C-L1]		VS[1D-L1]	
…								
19	VS[9A-L1]		VS[9B-L1]		VS[9C-L1]		VS[9D-L1]	
20	VS[0A-L2]		VS[0B-L2]		VS[0C-L2]		VS[0D-L2]	
21	VS[1A-L2]		VS[1B-L2]		VS[1C-L2]		VS[1D-L2]	
…								
29	VS[9A-L2]		VS[9B-L2]		VS[9C-L2]		VS[9D-L2]	
…								
…								
40	VS[0A-L4]		VS[0B-L4]		VS[0C-L4]		VS[0D-L4]	
41	VS[1A-L4]		VS[1B-L4]		VS[1C-L4]		VS[1D-L4]	
…								
49	VS[9A-L4]		VS[9B-L4]		VS[9C-L4]		VS[9D-L4]	
50	TP[0A]							
51	TP[0B]							
52	TP[0C]							
53	TP[0D]							
54	RP[0]							
55	TP[1A]							
56	TP[1B]							
57	TP[1C]							
58	TP[1D]							
59	RP[1]							
…	…							
…	…							
95	TP[9A]							
96	TP[9B]							
97	TP[9C]							
98	TP[9D]							
99	RP[9]							
100	5 bytes for frame rate							
101								
102								
103								
104								
105	VGH							
106	VSH1							
107	VSH2							
108	VSL							
109	VCOM							
110	Reserve 1							
111	Reserve 2							

Figure 6-6 : Waveform LUT

6.8 Temperature Sensing

The SSD1677 has internal temperature sensor to detect the environment temperature or can communicate with the external temperature sensor by I2C single master interface or can communicate with the external MCU to get the temperature value through SPI. In the SSD1677, there is a dedicated format for the temperature value so that the driver IC can understand it. The format of temperature value is described in Section 6.8.3.

6.8.1 Internal Temperature Sensor

The internal temperature sensor can be selected by command register. The accuracy of it is ±2degC from -25degC to 50degC.

6.8.2 External Temperature Sensor I2C Single Master Interface

The driver IC can communicate with the external temperature sensor through I2C single master interface (TSDA and TSCL). TSDA will be SDA and TSCL will be SCL. TSDA and TSCL are required to connect with external pull-up resistor. Temperature register value of external temperature sensor can be read by command register.

6.8.3 Format of temperature value

The temperature value is defined by 12-bit binary. The rules are shown as below.

- If the Temperature value MSByte bit D11 = 0, then
  the temperature is positive and value (DegC) = + (Temperature value) / 16
- If the Temperature value MSByte bit D11 = 1, then
  the temperature is negative and value (DegC) = - (2's complement of Temperature value) / 16

Table 6-7 shows some examples of 12-bit binary temperature value:

Table 6-7 : Example of 12-bit binary temperature settings for temperature ranges

12-bit binary (2's complement)	Hexadecimal Value	TR Value [DegC]
0111 1111 1111	7FF	128
0111 1111 1111	7FF	127.9
0110 0100 0000	640	100
0101 0000 0000	500	80
0100 1011 0000	4B0	75
0011 0010 0000	320	50
0001 1001 0000	190	25
0000 0000 0100	4	0.25
0000 0000 0000	0	0
1111 1111 1100	FFC	-0.25
1110 0111 0000	E70	-25
1100 1001 0000	C90	-55

6.9 Waveform LUT Searching Mechanism

As mentioned in Section 6.7, the SSD1677 OTP can store waveform LUT settings and temperature range. If waveform LUT settings and temperature range are programmed in OTP memory, corresponding waveform LUT can be selected according to the sensed temperature to drive the display. The waveform LUT searching mechanism by driver IC is as follows.

1) Read temperature value by command register in the format of 12-bit binary.
2) According to read temperature and display mode selection, search LUT in OTP from TR0 to TR33 in sequence. The last match will be selected, then, the corresponding WS will be loaded in the LUT register to drive the display.

Remark: Waveform LUT selection criteria is "Lower temperature bound < Sensed temperature ≤ Upper temperature bound".

Table 6-8 shows an example for the waveform LUT searching from OTP:

- If the read temperature is 25degC, then, WS4 will be selected.
- If the read temperature is 34degC, then, WS7 will be selected. Although 34degC is also in the temperature range TR6, according to searching mechanism, the last match should be selected. Therefore, WS7 is selected.

Table 6-8 : Example of waveform settings selection based on temperature ranges.

Waveform LUT in OTP	Temperature Range in OTP	TR Lower Limit [Hex]	TR Upper Limit [Hex]	Temperature range in OTP
WS0	TR0	800	050	-128 DegC < Temperature ≤ 5 DegC
WS1	TR1	050	0A0	5 DegC < Temperature ≤ 10DegC
WS2	TR2	0A0	0F0	10 DegC < Temperature ≤ 15DegC
WS3	TR3	0F0	140	15 DegC < Temperature ≤ 20DegC
WS4	TR4	140	190	20 DegC < Temperature ≤ 25DegC
WS5	TR5	190	1E0	25 DegC < Temperature ≤ 30DegC
WS6	TR6	1E0	230	30 DegC < Temperature ≤ 35DegC
WS7	TR7	210	7FF	33 DegC < Temperature ≤ 127.9DegC
Others	Others	000	000	

Precaution:
Please ensure the temperature range covers whole range of application temperatures, display will not be updated if no suitable temperature range matches the sensed temperature.

6.10 One Time Programmable (OTP) Memory

In the SSD1677, there is an embedded OTP memory which is designed to store the waveform settings of different temperature range and some variables/parameters. The OTP memory can store 34 sets of waveform LUT settings (WS), 34 sets of temperature range (TR), VCOM value, display mode selection, waveform version and user ID. Figure 6-7 shows the address mapping of the 34 waveform setting (WS0 to WS33) and temperature range (TR0 to TR33).

	D7	D6	D5	D4	D3	D2	D1	D0
0	WS0							
…								
111								
112	WS1							
…								
223								
224	WS2							
…								
335								
336	WS3							
…								
447								
	…							
3584	WS32							
…								
3695								
3696	WS33							
…								
3807								
3808	TR0							
3809								
3810								
3811	TR1							
3812								
3813								
3814	TR2							
3815								
3816								
3817	TR3							
3818								
3819								
3820	TR4							
3821								
3822								
	…							
3904	TR32							
3905								
3906								
3907	TR33							
3908								
3909								

Figure 6-7 : The Waveform setting mapping in OTP for waveform setting and temperature range

6.10.1 The Format for Temperature Range (TR)

The format of TR Lower limit and Upper limit as shown in Figure 6-8 which temp_L[11:0] is the lower limit and temp_H[11:0] is the upper limit of the temperature range. There has 34sets of TR for waveform LUT searching.

D7	D6	D5	D4	D3	D2	D1	D0
temp_L[7:0]							
temp_H[3:0]				temp_L[11:8]			
temp_H[11:4]							

Figure 6-8 : Format of Temperature Range (TR) in OTP

6.11 VCI Detection

The VCI detection function is used to detect the VCI level when it is lower than Vlow, threshold voltage set by register.

In the SSD1677, there is a command to execute the VCI detection function. When the VCI detection command is issued, the VCI detection will be executed. During the detection period, BUSY output is at high level. BUSY output is at low level when the detection is completed. Then, user can issue the Status Bit Read command to check the status bit for the result of VCI, which 0 is normal, 1 is VCI<Vlow.

6.12 HV Ready Detection

The HV Ready detection function is used for checking if driving voltage is ready before driven the EPD panel.

In the SSD1677, it has the flexibility to set the number of detection and the detection duration for each HV ready detection operation. And, during the detection period, BUSY output is at high level until the operation is completed. After BUSY become to low level, the detection result can be read from Status register.

7 COMMAND TABLE

Table 7-1: Command Table

<table>
<tr><th colspan="13">Command Table</th></tr>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>01</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="4">Driver Output control</td><td rowspan="4">Gate setting
A[9:0]= 2A7h [POR], 680 MUX
MUX Gate lines setting as (A[9:0] + 1).

B[2:0] = 000 [POR].
Gate scanning sequence and direction

B[2]: GD
Selects the 1st output Gate
GD=0 [POR],
G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, …
GD=1,
G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, …

B[1]: SM
Change scanning order of gate driver.
SM=0 [POR],
G0, G1, G2, G3…679 (left and right gate interlaced)
SM=1,
G0, G2, G4 …G678, G1, G3, …G679

B[0]: TB
TB = 0, Scan from G0 to G679
TB = 1, Reserved</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_9</td><td>A_8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>03</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td rowspan="2">Gate Driving voltage Control</td><td rowspan="2">Set Gate driving voltage
A[4:0] = 00h [POR]
VGH setting from 12V to 20V
<table>
<tr><td>A[4:0]</td><td>VGH</td><td>A[4:0]</td><td>VGH</td></tr>
<tr><td>00h</td><td>20</td><td>10h</td><td>16.5</td></tr>
<tr><td>07h</td><td>12</td><td>11h</td><td>17</td></tr>
<tr><td>08h</td><td>12.5</td><td>12h</td><td>17.5</td></tr>
<tr><td>09h</td><td>13</td><td>13h</td><td>18</td></tr>
<tr><td>0Ah</td><td>13.5</td><td>14h</td><td>18.5</td></tr>
<tr><td>0Bh</td><td>14</td><td>15h</td><td>19</td></tr>
<tr><td>0Ch</td><td>14.5</td><td>16h</td><td>19.5</td></tr>
<tr><td>0Dh</td><td>15</td><td>17h</td><td>20</td></tr>
<tr><td>0Eh</td><td>15.5</td><td>Other</td><td>NA</td></tr>
<tr><td>0Fh</td><td>16</td><td></td><td></td></tr>
</table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
</table>

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source driving voltage A[7:0] = 41h [POR], VSH1 at 15V B[7:0] = A8h [POR], VSH2 at 5V. C[7:0] = 32h [POR], VSL at -15V
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		

B[7] = 1,
VSH2 voltage setting from 2.4V to 8.8V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
8Eh	2.4	AFh	5.7
8Fh	2.5	B0h	5.8
90h	2.6	B1h	5.9
91h	2.7	B2h	6
92h	2.8	B3h	6.1
93h	2.9	B4h	6.2
94h	3	B5h	6.3
95h	3.1	B6h	6.4
96h	3.2	B7h	6.5
97h	3.3	B8h	6.6
98h	3.4	B9h	6.7
99h	3.5	BAh	6.8
9Ah	3.6	BBh	6.9
9Bh	3.7	BCh	7
9Ch	3.8	BDh	7.1
9Dh	3.9	BEh	7.2
9Eh	4	BFh	7.3
9Fh	4.1	C0h	7.4
A0h	4.2	C1h	7.5
A1h	4.3	C2h	7.6
A2h	4.4	C3h	7.7
A3h	4.5	C4h	7.8
A4h	4.6	C5h	7.9
A5h	4.7	C6h	8
A6h	4.8	C7h	8.1
A7h	4.9	C8h	8.2
A8h	5	C9h	8.3
A9h	5.1	CAh	8.4
AAh	5.2	CBh	8.5
ABh	5.3	CCh	8.6
ACh	5.4	CDh	8.7
ADh	5.5	CEh	8.8
AEh	5.6	Other	NA

A[7]/B[7] = 0,
VSH1/VSH2 voltage setting from 9V to 17V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
23h	9	3Ch	14
24h	9.2	3Dh	14.2
25h	9.4	3Eh	14.4
26h	9.6	3Fh	14.6
27h	9.8	40h	14.8
28h	10	41h	15
29h	10.2	42h	15.2
2Ah	10.4	43h	15.4
2Bh	10.6	44h	15.6
2Ch	10.8	45h	15.8
2Dh	11	46h	16
2Eh	11.2	47h	16.2
2Fh	11.4	48h	16.4
30h	11.6	49h	16.6
31h	11.8	4Ah	16.8
32h	12	4Bh	17
33h	12.2	Other	NA
34h	12.4		
35h	12.6		
36h	12.8		
37h	13		
38h	13.2		
39h	13.4		
3Ah	13.6		
3Bh	13.8		

C[7] = 0,
VSL setting from -9V to -17V

C[7:0]	VSL
1Ah	-9
1Ch	-9.5
1Eh	-10
20h	-10.5
22h	-11
24h	-11.5
26h	-12
28h	-12.5
2Ah	-13
2Ch	-13.5
2Eh	-14
30h	-14.5
32h	-15
34h	-15.5
36h	-16
38h	-16.5
3Ah	-17
Other	NA

Remark:
VSH1> VSH2

Command Table

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>08</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Initial Code Setting OTP Program</td><td>Program Initial Code Setting

The command required CLKEN=1.
Refer to Register 0x22 for detail.
BUSY pad will output high during operation.</td></tr>
<tr><td>0</td><td>0</td><td>09</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td rowspan="5">Write Register for Initial Code Setting</td><td rowspan="5">Write Register for Initial Code Setting Selection
A[7:0] ~ D[7:0]: Reserved
Details refer to Application Notes of Initial Code Setting</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B_7</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>C_7</td><td>C_6</td><td>C_5</td><td>C_4</td><td>C_3</td><td>C_2</td><td>C_1</td><td>C_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>D_7</td><td>D_6</td><td>D_5</td><td>D_4</td><td>D_3</td><td>D_2</td><td>D_1</td><td>D_0</td></tr>
<tr><td>0</td><td>0</td><td>0A</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Read Register for Initial Code Setting</td><td>Read Register for Initial Code Setting</td></tr>
<tr><td>0</td><td>0</td><td>0C</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td rowspan="6">Booster Soft-start Control</td><td rowspan="6">This command is used to control the inrush current for the booster.

Two level of strengths can be selected for the booster
<table>
<tr><th></th><th colspan="5">Data bytes</th></tr>
<tr><td></td><td>A[7:0]</td><td>B[7:0]</td><td>C[7:0]</td><td>D[7:0]</td><td>E[7:0]</td></tr>
<tr><td>Level 1</td><td>AE</td><td>C7</td><td>C3</td><td>C0</td><td>40</td></tr>
<tr><td>Level 2</td><td>AE</td><td>C7</td><td>C3</td><td>C0</td><td>80</td></tr>
</table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B_7</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>C_7</td><td>C_6</td><td>C_5</td><td>C_4</td><td>C_3</td><td>C_2</td><td>C_1</td><td>C_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>D_7</td><td>D_6</td><td>D_5</td><td>D_4</td><td>D_3</td><td>D_2</td><td>D_1</td><td>D_0</td></tr>
<tr><td></td><td></td><td></td><td>E_7</td><td>E_6</td><td>E_5</td><td>E_4</td><td>E_3</td><td>E_2</td><td>E_1</td><td>E_0</td></tr>
<tr><td>0</td><td>0</td><td>10</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">Deep Sleep mode</td><td rowspan="2">Deep Sleep mode Control:
<table>
<tr><th>A[1:0] :</th><th>Description</th></tr>
<tr><td>00</td><td>Normal Mode [POR]</td></tr>
<tr><td>11</td><td>Enter Deep Sleep Mode</td></tr>
</table>
After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high.
Remark:
To Exit Deep Sleep mode, User required to send HWRESET to the driver</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_1</td><td>A_0</td></tr>
</table>

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A[2:0] = 011 [POR] A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	A_2	A_1	A_0		
0	0	12	0	0	0	1	0	0	1	0	SW RESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode During operation, BUSY pad will output high. Note: RAM are unaffected by this command.
0	0	14	0	0	0	1	0	1	0	0	HV Ready Detection	HV ready detection A[6:0] = 00h [POR] The command required CLKEN=1 and ANALOGEN=1. Refer to Register 0x22 for detail. After this command initiated, HV Ready detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).
0	1		0	A_6	A_5	A_4	0	A_2	A_1	A_0		A[6:4]=n for cool down duration: 10ms x (n+1) A[2:0]=m for number of Cool Down Loop to detect. The max HV ready duration is 10ms x (n+1) x (m) HV ready detection will be trigger after each cool down time. The detection will be completed when HV is ready. For 1 shot HV ready detection, A[7:0] can be set as 00h.

<table>
<tr><th colspan="13">Command Table</th></tr>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>15</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td rowspan="2">VCI Detection</td><td rowspan="2">VCI Detection
A[2:0] = 100 [POR] , Detect level at 2.3V
A[2:0] : VCI level Detect
<table>
<tr><td>A[2:0]</td><td>VCI level</td></tr>
<tr><td>011</td><td>2.2V</td></tr>
<tr><td>100</td><td>2.3V</td></tr>
<tr><td>101</td><td>2.4V</td></tr>
<tr><td>110</td><td>2.5V</td></tr>
<tr><td>111</td><td>2.6V</td></tr>
<tr><td>Other</td><td>NA</td></tr>
</table>
The command required CLKEN=1 and ANALOGEN=1
Refer to Register 0x22 for detail.

After this command initiated, VCI detection starts.
BUSY pad will output high during detection.
The detection result can be read from the Status Bit Read (Command 0x2F).</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>18</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td rowspan="2">Temperature Sensor Control</td><td rowspan="2">Temperature Sensor Selection
A[7:0] = 48h [POR], external temperatrure sensor
A[7:0] = 80h Internal temperature sensor</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>1A</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td rowspan="3">Temperature Sensor Control (Write to temperature register)</td><td rowspan="3">Write to temperature register.
A[11:0] = 7FFh [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_{11}</td><td>A_{10}</td><td>A_9</td><td>A_8</td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>1B</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td rowspan="3">Temperature Sensor Control (Read from temperature register)</td><td rowspan="3">Read from temperature register.</td></tr>
<tr><td>1</td><td>1</td><td></td><td>A_{11}</td><td>A_{10}</td><td>A_9</td><td>A_8</td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td></tr>
<tr><td>1</td><td>1</td><td></td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>

<table>
<tr><th colspan="13">Command Table</th></tr>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>1C</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td rowspan="4">Temperature Sensor Control (Write Command to External temperature sensor)</td><td rowspan="4">Write Command to External temperature sensor.
A[7:0] = 00h [POR],
B[7:0] = 00h [POR],
C[7:0] = 00h [POR],

A[7:6]
<table>
<tr><td>A[7:6]</td><td>Select no of byte to be sent</td></tr>
<tr><td>00</td><td>Address + pointer</td></tr>
<tr><td>01</td><td>Address + pointer + 1st parameter</td></tr>
<tr><td>10</td><td>Address + pointer + 1st parameter + 2nd pointer</td></tr>
<tr><td>11</td><td>Address</td></tr>
</table>
A[5:0] – Pointer Setting
B[7:0] – 1st parameter
C[7:0] – 2nd parameter
The command required CLKEN=1.
Refer to Register 0x22 for detail.

After this command initiated, Write Command to external temperature sensor starts. BUSY pad will output high during operation.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B_7</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>C_7</td><td>C_6</td><td>C_5</td><td>C_4</td><td>C_3</td><td>C_2</td><td>C_1</td><td>C_0</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>20</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Master Activation</td><td>Activate Display Update Sequence

The Display Update Sequence Option is located at R22h.

BUSY pad will output high during operation. User should not interrupt this operation to avoid corruption of panel images.</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>21</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="2">Display Update Control 1</td><td rowspan="2">RAM content option for Display Update
A[7:0] = 00h [POR]

A[7:4] Red RAM option
<table>
<tr><td>0000</td><td>Normal</td></tr>
<tr><td>0100</td><td>Bypass RAM content as 0</td></tr>
<tr><td>1000</td><td>Inverse RAM content</td></tr>
</table>
A[3:0] BW RAM option
<table>
<tr><td>0000</td><td>Normal</td></tr>
<tr><td>0100</td><td>Bypass RAM content as 0</td></tr>
<tr><td>1000</td><td>Inverse RAM content</td></tr>
</table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
</table>

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation A[7:0]= FFh (POR)
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Operating sequence	Parameter (in Hex)
Enable clock signal	80
Disable clock signal	01
Enable clock signal ➔ Enable Analog	C0
Disable Analog ➔ Disable clock signal	03
Enable clock signal ➔ Load LUT with DISPLAY Mode 1 ➔ Disable clock signal	91
Enable clock signal ➔ Load LUT with DISPLAY Mode 2 ➔ Disable clock signal	99
Enable clock signal ➔ Load temperature value from I2C Single Master Interface ➔ Load LUT with DISPLAY Mode 1 ➔ Disable clock signal	B1
Enable clock signal ➔ Load temperature value from I2C Single Master Interface ➔ Load LUT with DISPLAY Mode 2 ➔ Disable clock signal	B9
Enable clock signal ➔ Enable Analog ➔ Display with DISPLAY Mode 1 ➔ Disable Analog ➔ Disable OSC	C7
Enable clock signal ➔ Enable Analog ➔ Display with DISPLAY Mode 2 ➔ Disable Analog ➔Disable OSC	CF
Enable clock signal ➔Enable Analog ➔ Load temperature value from I2C Single Master Interface ➔ Load temperature value from I2C Single Master Interface ➔ DISPLAY with DISPLAY Mode 1 ➔ Disable Analog ➔ Disable OSC	F7
Enable clock signal ➔Enable Analog ➔ Load temperature value from I2C Single Master Interface ➔ Load temperature value from I2C Single Master Interface ➔ DISPLAY with DISPLAY Mode 2 ➔ Disable Analog ➔ Disable OSC	FF

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	24	0	0	1	0	0	1	0	0	Write RAM (Black White) / RAM 0x24	After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly For White pixel: Content of Write RAM(BW) = 1 For Black pixel: Content of Write RAM(BW) = 0
0	0	25	0	0	1	0	0	1	0	1	Write RAM (Dithering)	After this command, data entries will be written into the dithering engine.
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED) / RAM 0x26	After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly. For Red pixel: Content of Write RAM(RED) = 1 For non-Red pixel [Black or White]: Content of Write RAM(RED) = 0
0	0	27	0	0	1	0	0	1	1	1	Read RAM	After this command, data read on the MCU bus will fetch data from RAM [According to parameter of Register 41h to select reading RAM(BW) / RAM(RED)], until another command is written. Address pointers will advance accordingly. The 1st byte of data read is dummy data.
0	0	28	0	0	1	0	1	0	0	0	VCOM Sense	Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value. The sensed VCOM voltage is stored in register The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	29	0	0	1	0	1	0	0	1	VCOM Sense Duration	Stabling time between entering VCOM sensing mode and reading acquired. A[6]=1, Normal Mode A[6]=0, Reserve A[3:0] = 09h, duration = 10s. VCOM sense duration = Setting + 1 Seconds
0	1		0	A_6	0	0	A_3	A_2	A_1	A_0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	2A	0	0	1	0	1	0	1	0	Program VCOM OTP	Program VCOM register into OTP The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	2B	0	0	1	0	1	0	1	1	Write Register for VCOM Control	This command is used to reduce glitch when ACVCOM toggle. Two data bytes D04h and D63h should be set for this command.
0	1		0	0	0	0	0	1	0	0		
0	1		0	1	1	0	0	0	1	1		
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Write VCOM register from MCU interface A[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

A[7:0]	VCOM	A[7:0]	VCOM
08h	-0.2	58h	-2.2
0Ch	-0.3	5Ch	-2.3
10h	-0.4	60h	-2.4
14h	-0.5	64h	-2.5
18h	-0.6	68h	-2.6
1Ch	-0.7	6Ch	-2.7
20h	-0.8	70h	-2.8
24h	-0.9	74h	-2.9
28h	-1	78h	-3
2Ch	-1.1	7Ch	-3.1
30h	-1.2	80h	-3.2
34h	-1.3	84h	-3.2
38h	-1.4	88h	-3.4
3Ch	-1.5	8Ch	-3.5
40h	-1.6	90h	-3.6
44h	-1.7	94h	-3.7
48h	-1.8	98h	-3.8
4Ch	-1.9	9Ch	-3.9
50h	-2	A0h	-4
54h	-2.1	Others	Reserved

0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read for Display Option	Read Register for Display Option: A[7:0]: VCOM OTP Selection (Command 0x37, Byte A) B[7:0]: VCOM Register (Command 0x2C) C[7:0]~G[7:0]: Display Mode (Command 0x37, Byte B to Byte F) [5 bytes] H[7:0]~K[7:0]: Waveform Version (Command 0x37, Byte G to Byte J) [4 bytes]
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
1	1		F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
1	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
1	1		H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
1	1		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
1	1		J_7	J_6	J_5	J_4	J_3	J_2	J_1	J_0		
1	1		K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	2E	0	0	1	0	1	1	1	0	User ID Read	Read 10 Byte User ID stored in OTP: A[7:0]]~J[7:0]: UserID (R38, Byte A and Byte J) [10 bytes]
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
1	1		F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
1	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
1	1		H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
1	1		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
1	1		J_7	J_6	J_5	J_4	J_3	J_2	J_1	J_0		
0	0	2F	0	0	1	0	1	1	1	1	Status Bit Read	Read IC status Bit [POR 0x01] A[5]: HV Ready Detection flag [POR=0] 0: Ready 1: Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1: VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01] Remark: A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively.
1	1		0	0	A_5	A_4	0	0	A_1	A_0		
0	0	30	0	0	1	1	0	0	0	0	Program WS OTP	Program OTP of Waveform Setting The contents should be written into RAM before sending this command. The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	31	0	0	1	1	0	0	0	1	Load WS OTP	Load OTP of Waveform Setting The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [105 bytes], which contains the content of VS [nX-LUT], TP #[nX], RP#[n]).
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		:	:	:	:	:	:	:	:		
0	1		.	..	.	.	.	.	.	.		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	34	0	0	1	1	0	1	0	0	CRC calculation	CRC calculation command BUSY pad will output high during operation.
0	0	35	0	0	1	1	0	1	0	1	CRC Status Read	CRC Status Read A[15:0] is the CRC read out value
1	1		A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8		
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	36	0	0	1	1	0	1	1	0	Program OTP selection	Program OTP Selection according to the OTP Selection Control [R37h and R38h] The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	37	0	0	1	1	0	1	1	1	Write Register for Display Option	Write Register for Display Option B[7:0] Display Mode for WS[7:0] C[7:0] Display Mode for WS[15:8] D[7:0] Display Mode for WS[23:16] E[7:0] Display Mode for WS[31:24] F[3:0] Display Mode for WS[35:32] 0: Display Mode 1 1: Display Mode 2 F[6]: RAM Ping-Pong for Display Mode 2 1: RAM ping-pong enable 0: RAM ping-pong disable G[7:0]~J[7:0] module ID /waveform version. Remarks: 1) A[7:0]~J[7:0] can be stored in OTP 2) RAM ping-pong function is not support for Display Mode 1
0	1		0	0	0	0	0	0	0	0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
0	1		0	F_6	0	0	F_3	F_2	F_1	F_0		
0	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
0	1		H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
0	1		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
0	1		J_7	J_6	J_5	J_4	J_3	J_2	J_1	J_0		
0	0	38	0	0	1	1	1	0	0	0	Write Register for User ID	Write Register for User ID A[7:0]]~J[7:0]: UserID [10 bytes] Remarks: A[7:0]~J[7:0] can be stored in OTP
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
0	1		F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
0	1		G_7	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
0	1		H_7	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
0	1		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
0	1		J_7	J_6	J_5	J_4	J_3	J_2	J_1	J_0		

<table>
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<tr><td>0</td><td>0</td><td>39</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td rowspan="2">OTP program mode</td><td rowspan="2">OTP program mode
A[1:0] = 00: Normal Mode [POR]
A[1:0] = 11: Internal generated OTP programming voltage

Remark: User is required to EXACTLY follow the reference code sequences</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_1</td><td>A_0</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>3A</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>3B</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>3C</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td rowspan="2">Border Waveform Control</td><td rowspan="2">Select border waveform for VBD
A[7:0] = C0h [POR], set VBD as HIZ.

A [7:6] :Select VBD option
<table>
<tr><th>A[7:6]</th><th>Select VBD as</th></tr>
<tr><td>00</td><td>GS Transition, Defined in A[1:0]</td></tr>
<tr><td>01</td><td>Fix Level, Defined in A[5:4]</td></tr>
<tr><td>10</td><td>VCOM</td></tr>
<tr><td>11[POR]</td><td>HiZ</td></tr>
</table>

A [5:4] Fix Level Setting for VBD
<table>
<tr><th>A[5:4]</th><th>VBD level</th></tr>
<tr><td>00[POR]</td><td>VSS</td></tr>
<tr><td>01</td><td>VSH1</td></tr>
<tr><td>10</td><td>VSL</td></tr>
<tr><td>11</td><td>VSH2</td></tr>
</table>

A [1:0] GS Transition setting for VBD
<table>
<tr><th>A[1:0]</th><th>VBD Transition</th></tr>
<tr><td>00[POR]</td><td>LUT0</td></tr>
<tr><td>01</td><td>LUT1</td></tr>
<tr><td>10</td><td>LUT2</td></tr>
<tr><td>11</td><td>LUT3</td></tr>
</table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>0</td><td>0</td><td>A_1</td><td>A_0</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>41</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="2">Read RAM Option</td><td rowspan="2">Read RAM Option
A[0]= 0 [POR]
0: Read RAM corresponding to RAM 0x24
1: Read RAM corresponding to RAM 0x26</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_0</td></tr>
</table>

<table>
<tr><th colspan="13">Command Table</th></tr>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>44</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td rowspan="5">Set RAM X - address Start / End position</td><td rowspan="5">Specify the start/end positions of the window address in the X direction by an address unit for RAM

A[9:0]: XSA[9:0], XStart, POR = 000h
B[9:0]: XEA[9:0], XEnd, POR = 3BFh</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_8</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>A_9</td><td>A_8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>B_9</td><td>B_8</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>45</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td rowspan="5">Set RAM Y- address Start / End position</td><td rowspan="5">Specify the start/end positions of the window address in the Y direction by an address unit for RAM

A[9:0]: YSA[9:0], YStart, POR = 000h
B[9:0]: YEA[9:0], YEnd, POR = 2A7h</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>A_9</td><td>A_8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B_7</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>B_9</td><td>B_8</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>46</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td rowspan="2">Auto Write RED RAM for Regular Pattern</td><td rowspan="2">Auto Write RED RAM for Regular Pattern
A[7:0] = 00h [POR]

A[7]: The 1st step value, POR = 0
A[6:4]: Step Height, POR= 000
Step of alter RAM in Y-direction according to Gate
<table>
<tr><th>A[6:4]</th><th>Height</th><th>A[6:4]</th><th>Height</th></tr>
<tr><td>000</td><td>8</td><td>100</td><td>128</td></tr>
<tr><td>001</td><td>16</td><td>101</td><td>256</td></tr>
<tr><td>010</td><td>32</td><td>110</td><td>512</td></tr>
<tr><td>011</td><td>64</td><td>111</td><td>680</td></tr>
</table>
A[2:0]: Step Width, POR= 000
Step of alter RAM in X-direction according to Source
<table>
<tr><th>A[2:0]</th><th>Width</th><th>A[2:0]</th><th>Width</th></tr>
<tr><td>000</td><td>8</td><td>100</td><td>128</td></tr>
<tr><td>001</td><td>16</td><td>101</td><td>256</td></tr>
<tr><td>010</td><td>32</td><td>110</td><td>512</td></tr>
<tr><td>011</td><td>64</td><td>111</td><td>960</td></tr>
</table>
BUSY pad will output high during operation.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>0</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
</table>

<table>
<tr><th colspan="13">Command Table</th></tr>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>47</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td rowspan="2">Auto Write B/W RAM for Regular Pattern</td><td rowspan="2">Auto Write B/W RAM for Regular Pattern
A[7:0] = 00h [POR]

A[7]: The 1st step value, POR = 0
A[6:4]: Step Hieght, POR= 000
Step of alter RAM in Y-direction according to Gate
<table>
<tr><th>A[6:4]</th><th>Height</th><th>A[6:4]</th><th>Height</th></tr>
<tr><td>000</td><td>8</td><td>100</td><td>128</td></tr>
<tr><td>001</td><td>16</td><td>101</td><td>256</td></tr>
<tr><td>010</td><td>32</td><td>110</td><td>512</td></tr>
<tr><td>011</td><td>64</td><td>111</td><td>680</td></tr>
</table>
A[2:0]: Step Width, POR= 000
Step of alter RAM in X-direction according to Source
<table>
<tr><th>A[2:0]</th><th>Width</th><th>A[2:0]</th><th>Width</th></tr>
<tr><td>000</td><td>8</td><td>100</td><td>128</td></tr>
<tr><td>001</td><td>16</td><td>101</td><td>256</td></tr>
<tr><td>010</td><td>32</td><td>110</td><td>512</td></tr>
<tr><td>011</td><td>64</td><td>111</td><td>960</td></tr>
</table>
During operation, BUSY pad will output high.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>0</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>4D</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td rowspan="5">Dithering engine Start/Stop</td><td rowspan="5">This command is used for start and stop dithering function, start commands should be sent before Command 0x25 and stop commands should be sent after the data bytes of command 0x25
<table>
<tr><th rowspan="2"></th><th colspan="4">Data byte</th></tr>
<tr><th>A[7:0]</th><th>B[7:0]</th><th>C[7:0]</th><th>D[7:0]</th></tr>
<tr><td>Start Sierra Lite</td><td>80</td><td>00</td><td>78</td><td>00</td></tr>
<tr><td>Start Floyd-Steinberg</td><td>83</td><td>00</td><td>78</td><td>00</td></tr>
<tr><td>Stop dithering</td><td>00</td><td>00</td><td>78</td><td>00</td></tr>
</table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B_7</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>C_7</td><td>C_6</td><td>C_5</td><td>C_4</td><td>C_3</td><td>C_2</td><td>C_1</td><td>C_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>D_7</td><td>D_6</td><td>D_5</td><td>D_4</td><td>D_3</td><td>D_2</td><td>D_1</td><td>D_0</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>4E</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td rowspan="3">Set RAM X address counter</td><td rowspan="3">Make initial settings for the RAM X address in the address counter (AC)
A[9:0]: 000h [POR].</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_9</td><td>A_8</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>4F</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td rowspan="3">Set RAM Y address counter</td><td rowspan="3">Make initial settings for the RAM Y address in the address counter (AC)
A[9:0]: 000h [POR].</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_9</td><td>A_8</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>7F</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>NOP</td><td>This command is an empty command; it does not have any effect on the display module.
However, it can be used to terminate Frame Memory Write or Read Commands.</td></tr>
</table>

8 COMMAND DESCRIPTION

8.1 Driver Output Control (01h)

This triple byte command has multiple configurations and each bit setting is described as follows:

Table 8-1 : POR settings for Driver Output Control (Command 0x01)

R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0
W	1	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0
POR		1	0	1	0	0	1	1	1
W	1							MUX9	MUX8
POR								1	0
W	1						GD	SM	TB
POR							0	0	0

MUX[9:0]: Specify number of lines for the driver: MUX[9:0] + 1. Multiplex ratio (MUX ratio) from 300 MUX to 680MUX.

TB: This bit is set at “0” for scanning from gate 0. Option TB = 1 is reserved.

SM: Change scanning order of gate driver.
When SM is set to 0, left and right interlaced is performed.
When SM is set to 1, no splitting odd / even of the GATE signal is performed,
Output pin assignment sequence is shown as below (for 680 MUX ratio):

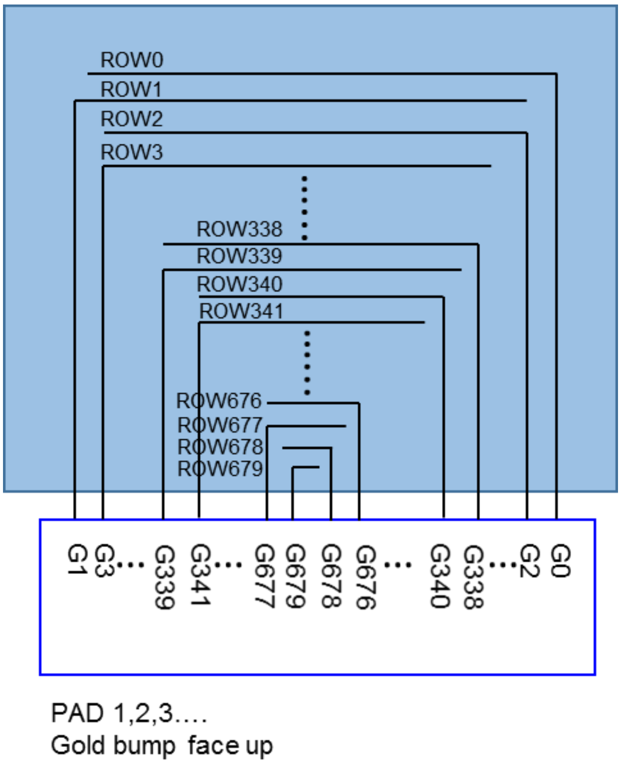
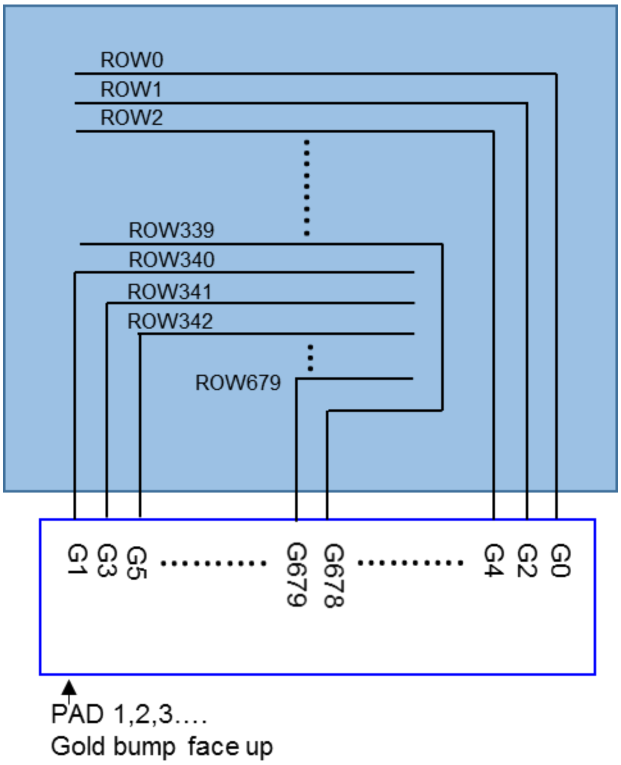
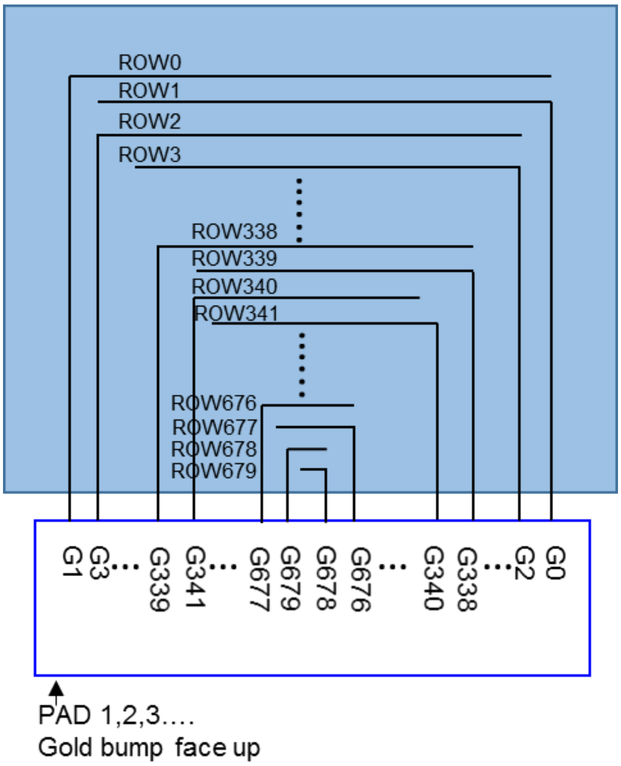
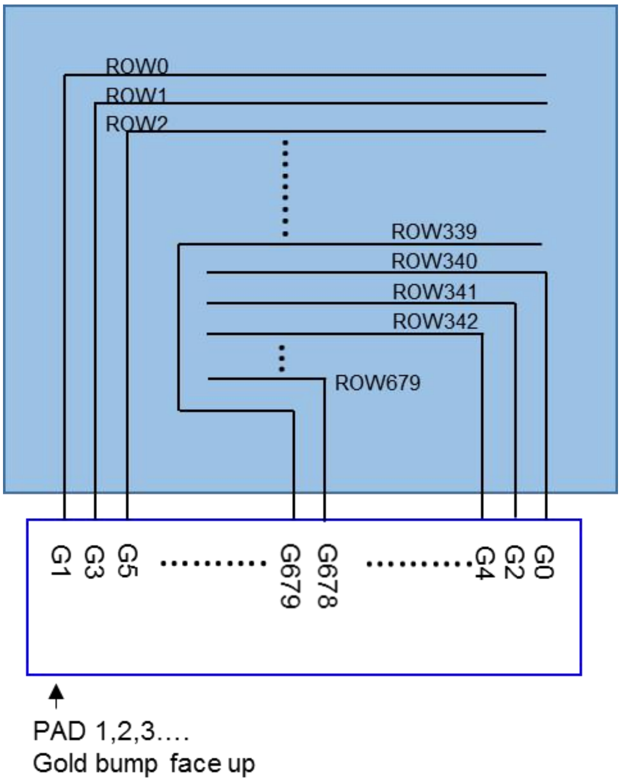
GD: Selects the 1st output Gate
This bit is made to match the GATE layout connection on the panel. It defines the first scanning line.

Table 8-2 and Figure 8-1 illustrate in details about GD and SM.

Table 8-2 : Output pin assignment sequence of SM and GD settings

	SM=0	SM=0	SM=1	SM=1
Driver	GD=0	GD=1	GD=0	GD=1
G0	ROW0	ROW1	ROW0	ROW340
G1	ROW1	ROW0	ROW340	ROW0
G2	ROW2	ROW3	ROW1	ROW341
G3	ROW3	ROW2	ROW341	ROW1
:	:	:	:	:
G338	ROW338	ROW339	ROW170	ROW510
G339	ROW339	ROW338	ROW510	ROW170
G340	ROW340	ROW341	ROW171	ROW511
G341	ROW341	ROW340	ROW511	ROW171
:	:	:	:	:
G676	ROW676	ROW677	ROW338	ROW678
G677	ROW677	ROW676	ROW678	ROW338
G678	ROW678	ROW679	ROW339	ROW679
G679	ROW679	ROW678	ROW679	ROW339

Figure 8-1: Output pin assignment on different setting of GD and SM

	SM = 0	SM = 1
GD = 0		
GD = 1		

8.2 Data Entry Mode Setting (11h)

This command has multiple configurations and each bit setting is described as follows:

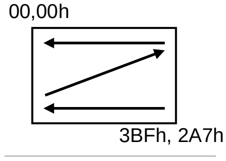
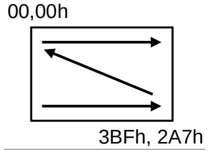
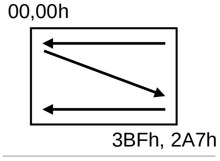
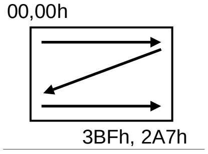
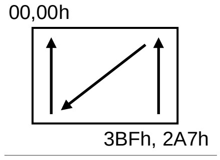
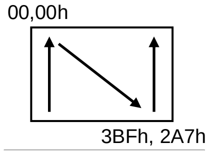
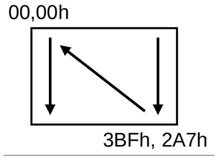
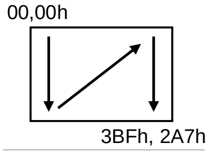
Table 8-3 : POR settings for Data Entry Mode Setting (Command 0x11)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1						AM	ID1	ID0
POR		0	0	0	0	0	0	1	1

ID[1:0]: The address counter is automatically incremented by 1, after data is written to the RAM when ID[1:0] = “01”. The address counter is automatically decremented by 1, after data is written to the RAM when ID[1:0] = “00”. The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. The direction of the address when data is written to the RAM is set by AM bits.

AM: Set the direction in which the address counter is updated automatically after data are written to the RAM. When AM = “0”, the address counter is updated in the X direction. When AM = “1”, the address counter is updated in the Y direction. When window addresses are selected, data are written to the RAM area specified by the window addresses in the manner specified with ID[1:0] and AM bits.

Table 8-4 : Address counter directions of ID and AM settings (Command 0x11)

	ID [1:0]="00” X: decrement Y: decrement	ID [1:0]="01” X: increment Y: decrement	ID [1:0]="10” X: decrement Y: increment	ID [1:0]="11” X: increment Y: increment
AM="0” X-mode				
AM="1” Y-mode				

8.3 Set RAM X - Address Start / End Position (44h)

This command is used to set the start/ end position of the window address in X-direction.

Table 8-5 : POR settings for Set RAM X - Address Start / End Position (Command 0x44)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	XSA7	XSA6	XSA5	XSA4	XSA3	XSA2	XSA1	XSA0
POR		0	0	0	0	0	0	0	0
W	1	-	-	-	-	-	-	XSA9	XSA8
POR		-	-	-	-	-	-	0	0
W	1	XEA7	XEA6	XEA5	XEA4	XEA3	XEA2	XEA1	XEA0
POR		1	0	1	1	1	1	1	1
W	1	-	-	-	-	-	-	XEA9	XEA8
POR		-	-	-	-	-	-	1	1

XSA[9:0]/XEA[9:0]: Specify the start/end positions of the window address in the X direction by an address unit. Data is written to the RAM within the area determined by the addresses specified by XSA [9:0] and XEA [9:0]. These addresses must be set before the RAM write.
It allows on XEA [9:0] ≤ XSA [9:0]. The settings follow the condition on 00h ≤ XSA [9:0], XEA [9:0] ≤ 3BFh.
The window is followed by the control setting of Data Entry Setting (R11h)

8.4 Set RAM Y - Address Start / End Position (45h)

This command is used to set the start/ end position of the window address in Y-direction.

Table 8-6 : POR settings for Set RAM Y - Address Start / End Position (Command 0x45)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	YSA7	YSA6	YSA5	YSA4	YSA3	YSA2	YSA1	YSA0
POR		0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	YSA9	YSA8
POR		0	0	0	0	0	0	0	0
W	1	YEA7	YEA6	YEA5	YEA4	YEA3	YEA2	YEA1	YEA0
POR		1	0	1	0	0	1	1	1
W	1	0	0	0	0	0	0	YEA9	YEA8
POR		0	0	0	0	0	0	1	0

YSA[9:0]/YEA[9:0]: Specify the start/end positions of the window address in the Y direction by an address unit. Data is written to the RAM within the area determined by the addresses specified by YSA [9:0] and YEA [9:0]. These addresses must be set before the RAM write.
It allows YEA [9:0] ≤ YSA [9:0]. The settings follow the condition on 00h ≤ YSA [9:0], YEA [9:0] ≤ 2A7h.
The window is followed by the control setting of Data Entry Setting (R11h)

8.5 Set RAM Address Counter (4Eh-4Fh)

These commands are used to set the start position of RAM address counter.

Table 8-7 : POR settings for Set RAM Address Counter (Command 0x4E~4F)

Reg#	R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
4Eh	W	1	XAD7	XAD6	XAD5	XAD4	XAD3	XAD2	XAD1	XAD0
	POR		0	0	0	0	0	0	0	0
	W	1	-	-	-	-	-	-	XAD9	XAD8
	POR		-	-	-	-	-	-	0	0
4Fh	W	1	YAD7	YAD6	YAD5	YAD4	YAD3	YAD2	YAD1	YAD0
	POR		0	0	0	0	0	0	0	0
	W	1	-	-	-	-	-	-	YAD9	YAD8
	POR		-	-	-	-	-	-	0	0

XAD[9:0]: Make initial settings for the RAM X address in the address counter (AC).
YAD[9:0]: Make initial settings for the RAM Y address in the address counter (AC).

After RAM data is written, the address counter is automatically updated according to the settings with AM, ID bits and setting for a new RAM address is not required in the address counter. Therefore, data is written consecutively without setting an address. The address counter is not automatically updated when data is read out from the RAM. RAM address setting cannot be made during the standby mode. The address setting should be made within the area designated with window addresses which is controlled by the Data Entry Setting (R11h) {AM, ID[1:0]} ; RAM Address XStart / XEnd Position (R44h) and RAM Address Ystart /Yend Position (R45h). Otherwise undesirable image will be displayed on the Panel.

9 Operation Flow and Code Sequence

9.1 General operation flow to drive display panel

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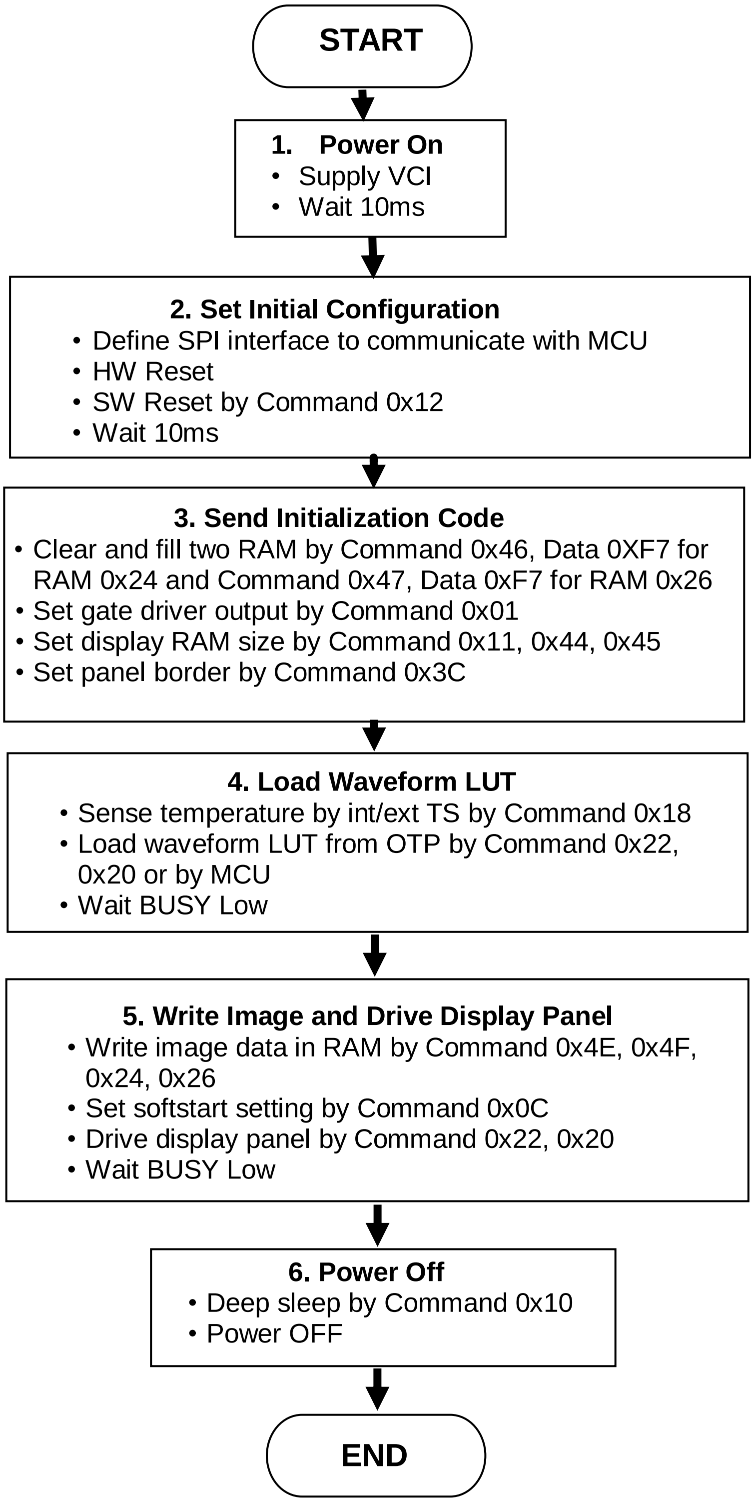


Figure 9-1: Operation flow to drive display panel

10 Absolute Maximum Rating

Table 10-1 : Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CI}	Logic supply voltage	-0.5 to +4.0	V
V_{IN}	Logic Input voltage	-0.5 to V_{DDIO}+0.5	V
V_{OUT}	Logic Output voltage	-0.5 to V_{DDIO}+0.5	V
T_{OPR}	Operation temperature range	-25 to 85	℃
T_{STG}	Storage temperature range	-65 to +150	℃

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{CI} be constrained to the range $V_{SS} < V_{CI}$. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DDIO}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

11 Electrical Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, VDD=1.8V, T_{OPR}=25℃.

Table 11-1: DC Characteristics

Symbol	Parameter	Applicable pin	Test Condition	Min.	Typ.	Max.	Unit
V_{CI}	VCI operation voltage	VCI		2.2	3.0	3.3	V
V_{DD}	VDD operation voltage	VDD		1.7	1.8	1.9	V
V_{COM_DC}	VCOM_DC output voltage	VCOM		-4.0		-0.1	V
dV_{COM_DC}	VCOM_DC output voltage deviation	VCOM		-100		100	mV
V_{COM_AC}	VCOM_AC output voltage	VCOM		V_{SL} + V_{COM_DC}	V_{COM_DC}	V_{SH1}+ V_{COM_DC}	V
V_{GATE}	Gate output voltage	G0~G679		-20		+20	V
$V_{GATE(p-p)}$	Gate output peak to peak voltage	G0~G679				40	V
V_{SH1R}	Positive Source output voltage	VSH1R		+9	+15	+17	V
dV_{SH1R}	VSH1R output voltage deviation	VSH1R		-200		200	mV
V_{SH2R}	Positive Source output voltage	VSH2R		+2.4	+5	+17	V
dV_{SH2R}	VSH2R output voltage deviation	VSH2R	2.4V to 8.8V	-100		100	mV
			8.8V to 17V	-200		200	mV
V_{SLR}	Negative Source output voltage	VSLR		-17	-15	-9	V
dV_{SLR}	VSLR output voltage deviation	VSLR		-200		200	mV
V_{IH}	High level input voltage	SDA, SCL, CS#, D/C#, RES#, BS1, M/S#, EXTVDD, CL		0.8V_{DDIO}			V
V_{IL}	Low level input voltage					0.2V_{DDIO}	V
V_{OH}	High level output voltage	SDA, BUSY, CL	IOH = -100uA	0.9V_{DDIO}			V
V_{OL}	Low level output voltage		IOL = 100uA			0.1V_{DDIO}	V

Symbol	Parameter	Applicable pin	Test Condition	Min.	Typ.	Max.	Unit
V_{PP}	OTP Program voltage	VPP		7.25	7.5	7.75	V
Islp_VCI	Sleep mode current	VCI	- DC/DC off - No clock - No output load - MCU interface access - RAM data access		25	40	uA
Idslp_VCI	Deep sleep mode current	VCI	- DC/DC off - No clock - No output load - No MCU interface access - Cannot retain RAM data		1	5	uA
Iopr_VCI	Operating Mode current	VCI	VCI=3.0V Enable Clock and Analog by Master Activation Command VGH=20V VGL=-VGH VSH1=15V VSH2=5V VSL=-15V VCOM = -2V No waveform transitions. No loading. No RAM read/write No OTP read /write		2.0		mA
V_{GH}	Operating Mode Output Voltage	VGH		19.5	20	20.5	V
V_{SH1}		VSH1		14.8	15	15.2	V
V_{SH2}		VSH2		4.9	5	5.1	V
V_{SL}		VSL		-15.2	-15	-14.8	V
V_{COM}		VCOM		-2.2	-2	-1.8	V

Table 11-2: Regulators Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
IVGH	VGH current	VGH = 20V	VGH			1000	uA
IVGL	VGL current	VGL = -VGH	VGL			1000	uA
IVSH	VSH1 current	VSH1 = +15V	VSH1			2000	uA
IVSH1	VSH2 current	VSH2 = +5V	VSH2			2000	uA
IVSL	VSL current	VSL = -15V	VSL			2000	uA
IVCOM	VCOM current	VCOM = -2V	VCOM			2000	uA

12 AC Characteristics

12.1 Serial Peripheral Interface

The following specifications apply for: VDDIO - VSS = 2.2V to 3.7V, $\mathbf{T}_{\mathbf{OPR}}$ = 25℃, CL=30pF

Table 12-1 : Serial Peripheral Interface Timing Characteristics

Write mode

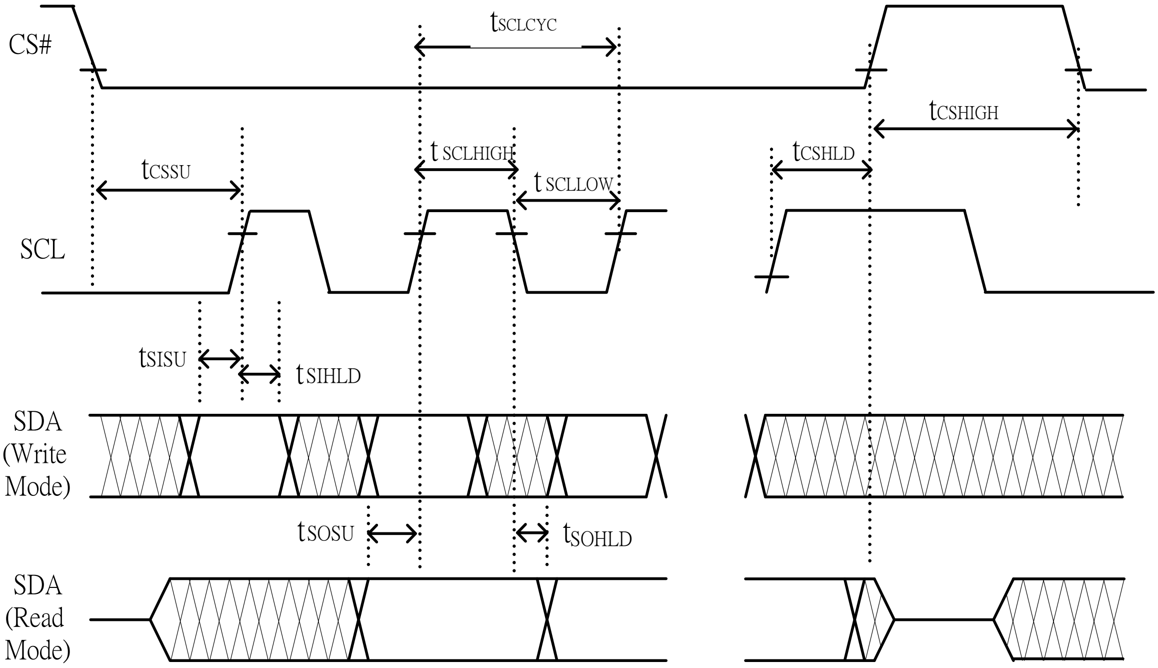
Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL frequency (Write Mode)			20	MHz
t_{CSSU}	Time CS# has to be low before the first rising edge of SCLK	20			ns
t_{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	20			ns
t_{CSHIGH}	Time CS# has to remain high between two transfers	100			ns
t_{SCLCYC}	SCL cycle time	50			ns
$t_{SCLHIGH}$	Part of the clock period where SCL has to remain high	25			ns
t_{SCLLOW}	Part of the clock period where SCL has to remain low	25			ns
t_{SISU}	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
t_{SIHLD}	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL frequency (Read Mode)			2.5	MHz
t_{CSSU}	Time CS# has to be low before the first rising edge of SCLK	100			ns
t_{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	50			ns
t_{CSHIGH}	Time CS# has to remain high between two transfers	250			ns
$t_{SCLHIGH}$	Part of the clock period where SCL has to remain high	180			ns
t_{SCLLOW}	Part of the clock period where SCL has to remain low	180			ns
t_{SOSU}	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
t_{SOHLD}	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

Note: All timings are based on 20% to 80% of VDDIO-VSS

Figure 12-1: SPI timing diagram



13 Application Circuit

Figure 13-1: Schematic of SSD1677 application circuit

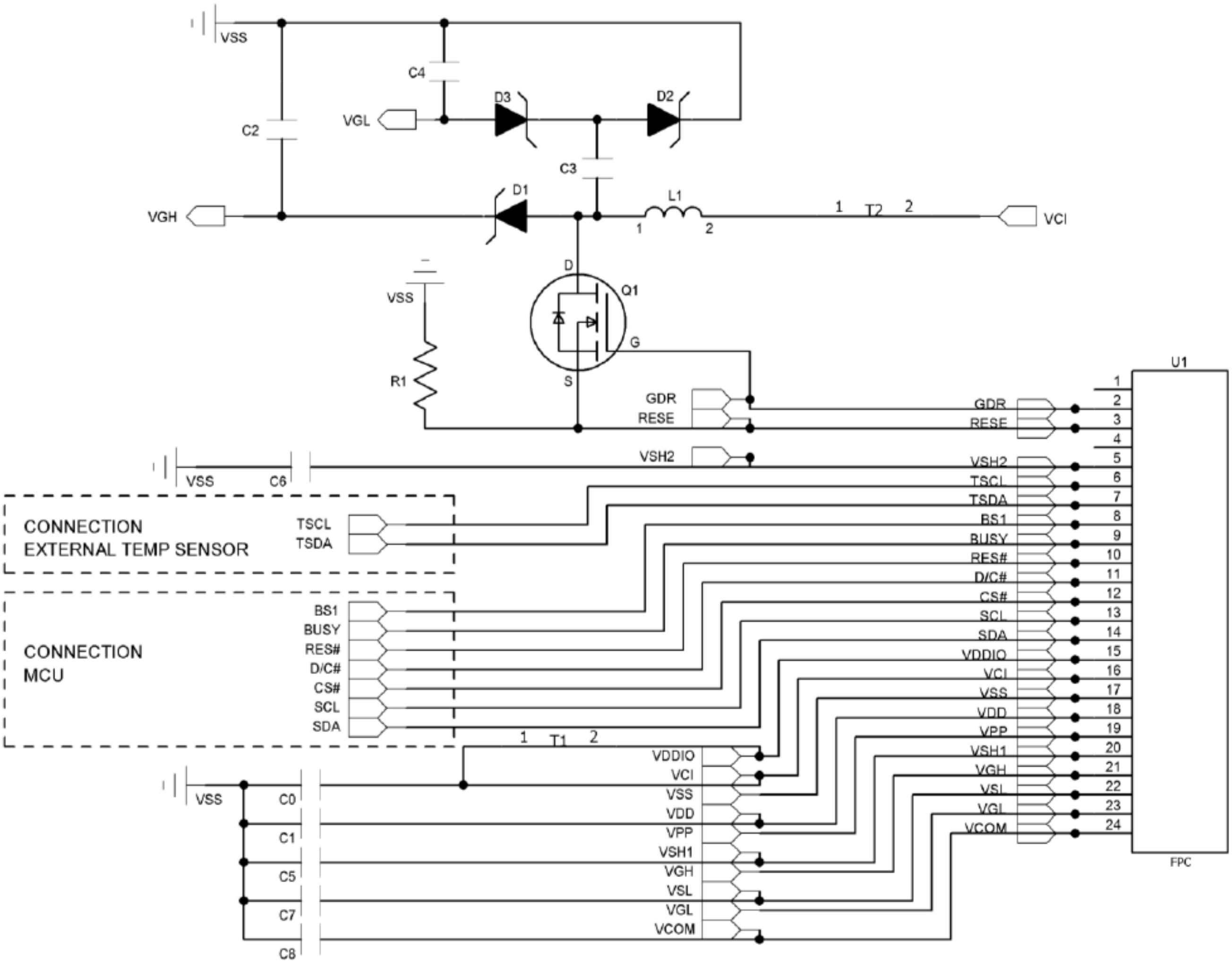


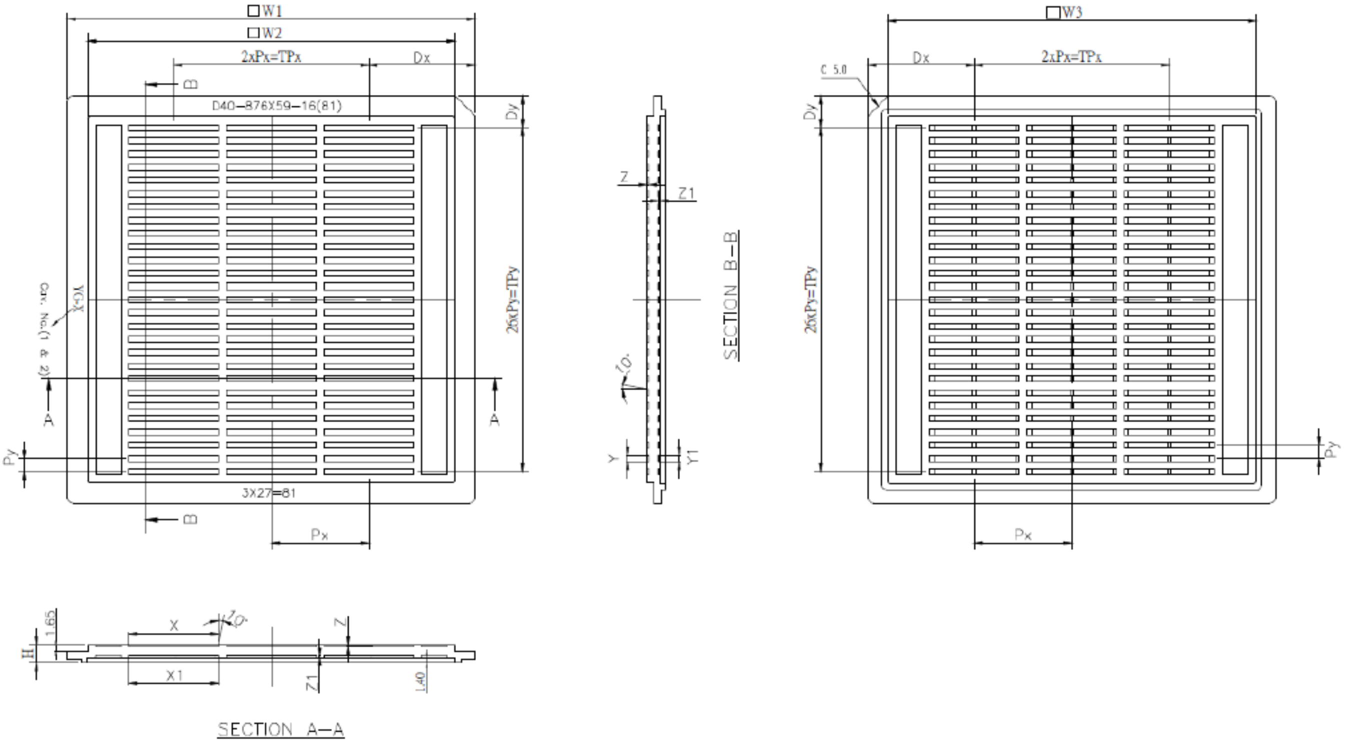
Table 13-1: Component list for SSD1677 application circuit

Part Name	Value	Reference Part/ Requirement
C0-C1	1uF	0603; X5R/X7R; Voltage Rating: 6V
C2-C7	4.7uF	0805; X5R/X7R; Voltage Rating: 25V
C8	1uF	0805; X7R; Voltage Rating: 25V
R1	2.2 Ohm	0805; 1%
D1-D3	Diode	MBR0530
Q1	NMOS	Si1304BDL
L1	47uH	CDRH2D18/ LDNP-470NC
U1	0.5mm ZIF socket	24pins, 0.5mm pitch

Remark: Component value is subjected to change and depends on panel loading.

14 Package Information

Figure 14-1 : SSD1677Z and SSD1677Z8 tray information



Symbol	Spec (mm)
W1	101.60±0.10
W2	91.55±0.10
W3	91.85±0.10
H	4.55±0.10
Dx	26.50±0.05
TPx	48.60±0.10
Dy	7.90±0.05
Tpy	85.80±0.10
Px	24.30±0.05
Py	3.30±0.05
X	22.25±0.05
Y	1.51±0.05
Z	0.40±0.05
X1	22.25±0.05
Y1	1.51±0.05
Z1	0.35±0.05
N	81 (pocket number)

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