HIGH-VOLTAGE MIXED-SIGNAL IC

UC8151

All-in-one driver IC w/ Timing Controller for
White/Black/Red Dot-Matrix Micro-Cup ESL

ES Specifications
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ULTRACHIP

The Coolest EPD Driver, Ever!

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UC8151

All-in-one driver IC with Timing Controller for White/Black/Red Dot-Matrix Micro-Cup ESL

INTRODUCTION

The UC8151 is an all-in-one driver with timing controller for ESL. Its output is of 1-bit white/black and 1-bit red resolution per pixel. The timing controller provides control signals for source driver and gate driver.

The DC-DC controller allows it to generate the source output voltage VDH/VDL (±6.4V~±15.0V) and VDHR (2.4V~11.0V). The chip also includes an output buffer for the supply of the COM electrode (AC-VCOM or DC-VCOM). The system is configurable through a 3-wire/4-wire (SPI) serial interface.

MAIN APPLICATIONS

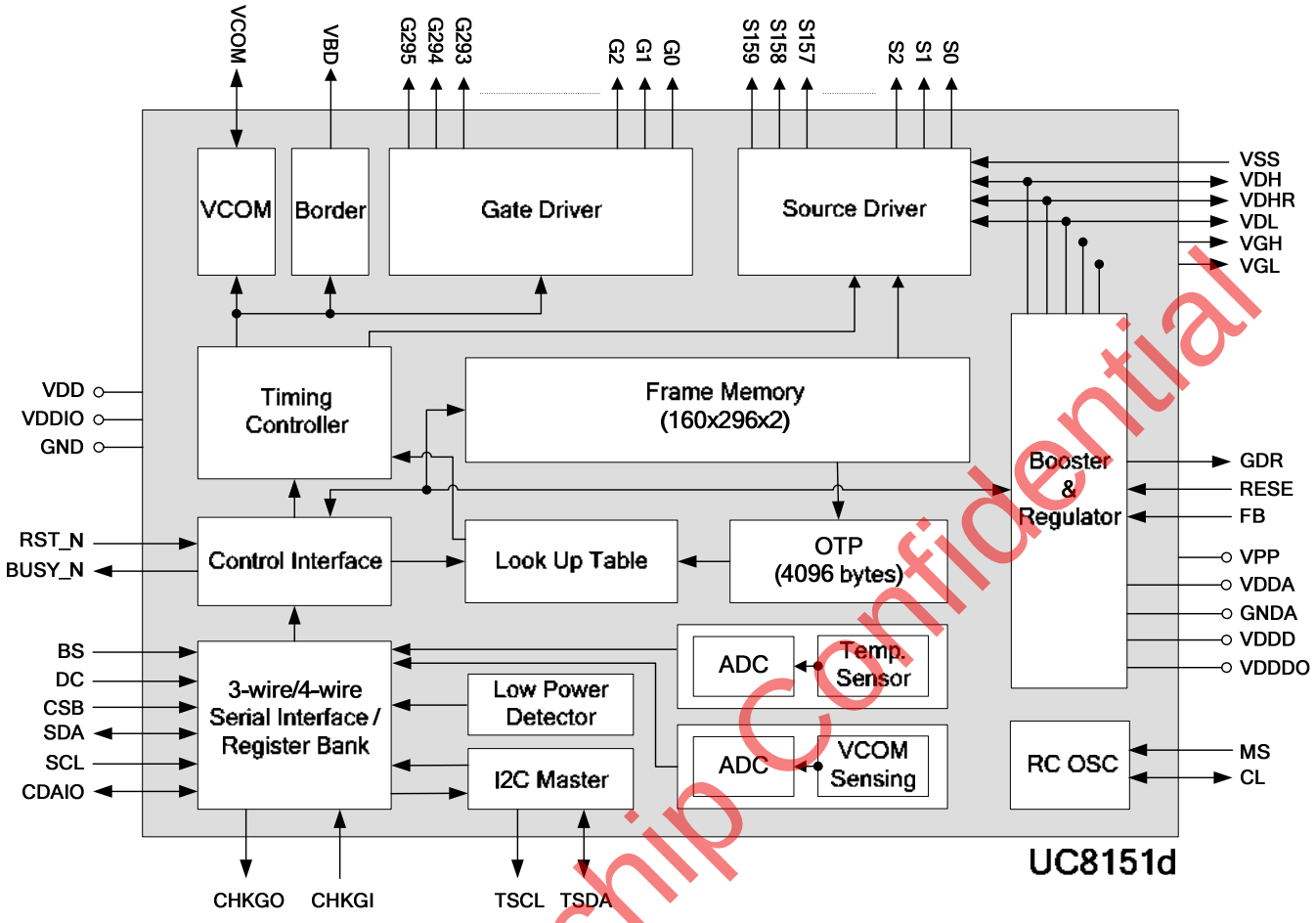
- E-tag application

FEATURE HIGHLIGHTS

- System-on-chip (SOC) for ESL
- Timing controller supports several resolutions
  - Up to 160 source x 296 gate resolution + 1 border + 1 VCOM
  - 1 bit for white/black and 1 bit for red per pixel
- Cascade: 2 or more chips cascade mode
- Memory (Max.): 160 x 296 x 2 bits SRAM
- 3-wire/4-wire (SPI) serial interface
  - Clock rate up to 20MHz
- Temperature sensor:
  - On-Chip: -25~50 ^{o}C ± 2.0^{o}C / 8-bit status
  - Off-Chip: -55~125^{o}C ± 2.0^{o}C /11-bit status (I^2C/LM75)
- Support LPD, Low Power Detection (V_{DD}<2.5V)
- OSC / PLL: On-chip RC oscillator
- VCOM:
  - AC-VCOM / DC-VCOM (by LUT)
  - Support VCOM sensing (6-bit digital status)
- Charge Pump: On-chip booster and regulator:
  - VGH: +20V
  - VGL: -20V
  - VDH: +6.4 ~ +15.0V (programmable, black/white)
  - VDL: -6.4 ~ -15.0V (programmable, black/white)
  - VDHR: +2.4 ~ +11.0V (programmable, red)
- Digital supply voltage: 2.3~ 3.6V
- OTP: 4K-byte OTP for LUTs and Settings
- Package: COG
- Source/Gate bump information
  - Bump pitch: 13 μM ± 2 μM
  - Bump space: 1 μM ± 3 μM
  - Bump surface: 1200 μM^2

Remark: Contact UltraChip for a visual inspection document (03-DOC-093).

BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Description
UC8151dHAB-U0P1-4	4-inch tray, wafer thickness 180uM
UC8151dHAB-U0P1-3	3-inch tray, wafer thickness 180uM
UC8151dHAB-U0X3-4	4-inch tray, wafer thickness 300uM
UC8151dHAB-U0X3-3	3-inch tray, wafer thickness 300uM

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

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PIN DESCRIPTION

Type: I: Input, O: Output, I/O: Input/Output, PWR: Power, C: Capacitor pin

Pin (Pad) Name	Pin Count	Type	Description
POWER SUPPLY PINS			
VDD	7	PWR	Digital power
VDDA	10	PWR	Analog power
VDDIO	10	PWR	IO power
VDDDO	4	PWR	Digital power output (1.8V)
VDDD (VDDI)	4	PWR	Digital power input (1.8V)
VPP	6	PWR	OTP program power (7.75V)
VDM	4	PWR	Analog Ground.
GND	18	PWR	Digital Ground.
GNDA	17	PWR	Analog Ground
LDO PINS			
VDH (VSH)	10	I/O	Positive source driver Voltage (+6.4V ~ +15V)
VDHR	8	I/O	Positive source driver voltage for Red (+2.4V ~ +11V)
VDL (VSL)	10	I/O	Negative source driver voltage (-6.4V ~ -15V)
CONTROL INTERFACE PINS			
BS	1	I	Bus Selection. Select 3-wire / 4-wire SPI interface L: 4-wire interface. H: 3-wire interface.
RST_N	1	I (Pull-up)	Global reset pin. Low: active. When RST_N becomes low, driver will reset. All register will reset to default value. Driver all function will disable. Source/Gate/Border/VCOM will be released to floating. The minimal width of RST_N=low is 50us.
MS	1	I	Cascade setting pin. L: Slave chip. H: Master chip.
CL	1	I/O	Clock input/output pin. Master: Clock output. Slave: Clock input.
CDAIO	1	I/O	Cascade data pin. Leave it open if not used.
BUSY_N	1	O	Driver busy flag. L: Driver is Busy. H: Host side can send command/data to driver.
MCU INTERFACE (SPI) PINS			
CSB	1	I	Serial communication chip select.
SDA	1	I/O	Serial communication data input/output
SCL	1	I	Serial communication clock input.
DC	1	I	Command/Data input. L: command H: data Connect to GND if BS=High.

Pin (Pad) Name	Pin Count	Type	Description
I²C INTERFACE			
TSCL	2	O (open-drain)	I²C clock (External pull-up resistor is necessary.) Leave them open if not used.
TSDA	2	I/O (open-drain)	I²C data (External pull-up resistor is necessary.) Leave them open if not used.
OUTPUT PINS			
S0~S159 (S<0>~S<159>)	160	O	Source driver output signals.
G0~G295 (G<0>~G<295>)	296	O	Gate driver output signals.
VCOM	16	O	VCOM output.
VBD (VBD<1>, VBD<2>)	1, 1	O	Border output pins.
BOOSTER PINS			
GDR	8	O	N-MOS gate control
RESE	2	P	Current sense input for control loop.
FB	2	P	(Keep Open.)
VGH	12	I/O	Positive Gate voltage.
VGL	16	I/O	Negative Gate voltage.
CHECK PANEL PINS			
CHKGI	1	I (Pull-down)	Check panel break input. Leave open if it is not used.
CHKGO	1	O	Check panel break output. Leave open if it is not used.
RESERVED PINS			
VSYNC	1	O	Reserved pins. Leave it floating.
TEST1~TEST3	3	I	Reserved pins. Leave it floating or connected to VSS.
TEST6, TEST7	2	O	Reserved pins. Leave it floating.
DUMMY	15	-	Reserved pins. Leave it floating.
NC	32	-	Not Connected.

COMMAND TABLE

W/R: 0: Write Cycle 1: Read Cycle C/D: 0: Command / 1: Data D7~D0: –: Don't Care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00H
		0	1	#	#	#	#	#	#	#	#	RES[1:0],REG,KW/R,UD,SHL, SHD_N,RST_N	0FH
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01H
		0	1	--	--	--	--	--	--	#	#	VDS_EN, VDG_EN	03H
		0	1	--	--	--	--	--	#	#	#	VCOM_HV,VGHL_LV[1:0]	00H
		0	1	--	--	#	#	#	#	#	#	VDH[5:0]	26H
		0	1	--	--	#	#	#	#	#	#	VDL[5:0]	26H
		0	1	--	--	#	#	#	#	#	#	VDHR[5:0]	03H
3	Power OFF (POF)	0	0	0	0	0	0	0	0	1	0		02H
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1		03H
		0	1	--	--	#	#	--	--	--	--	T_VDS_OF[1:0]	00H
5	Power ON (PON)	0	0	0	0	0	0	0	1	0	0		04H
6	Power ON Measure (PMES)	0	0	0	0	0	0	0	1	0	1		05H
7	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06H
		0	1	#	#	#	#	#	#	#	#	BT_PHA[7:0]	17H
		0	1	#	#	#	#	#	#	#	#	BT_PHB[7:0]	17H
		0	1	--	--	#	#	#	#	#	#	BT_PHC[5:0]	17H
8	Deep sleep (DSLP)	0	0	0	0	0	0	0	1	1	1		07H
		0	1	1	0	1	0	0	1	0	1	Check code	A5H
9	Display Start Transmission 1 (DTM1, White/Black Data) (x-byte command)	0	0	0	0	0	1	0	0	0	0	B/W or OLD Pixel Data (160x296):	10H
		0	1	#	#	#	#	#	#	#	#	KPXL[1:8]	00H
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	KPXL[n-1:n]	00H
10	Data Stop (DSP)	0	0	0	0	0	1	0	0	0	1		11H
		1	1	#	--	--	--	--	--	--	--		00H
11	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12H
12	Display Start transmission 2 (DTM2, Red Data) (x-byte command)	0	0	0	0	0	1	0	0	1	1	Red or NEW Pixel Data (160X296):	13H
		0	1	#	#	#	#	#	#	#	#	RPXL[1:8]	00H
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	RPXL[n-1:n]	00H
13	Auto Sequence (AUTO)	0	0	0	0	0	1	0	1	1	1		17H
		1	1	1	0	1	0	0	1	0	1	Check code	A5H
14	LUT option (LUTOPT)	0	0	0	0	1	0	1	0	1	0		2AH
		0	1	--	--	#	#	#	#	#	#	STATE_XON[5:0]	00H
		0	1	--	--	#	#	--	#	#	#	EXS[1:0], DMS[2:0]	00H
15	PLL control (PLL)	0	0	0	0	1	1	0	0	0	0		30H
		0	1	--	--	#	#	#	#	#	#	M[2:0], N[2:0]	3CH
16	Temperature Sensor Calibration (TSC)	0	0	0	1	0	0	0	0	0	0		40H
		1	1	#	#	#	#	#	#	#	#	D[10:3] / TS[7:0]	00H
		1	1	#	#	#	--	--	--	--	--	D[2:0] / -	00H
17	Temperature Sensor Selection (TSE)	0	0	0	1	0	0	0	0	0	1		41H
		0	1	#	--	--	--	#	#	#	#	TSE,TO[3:0]	00H

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
18	Temperature Sensor Write (TSW)	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**		**42H**
		0	1	#	#	#	#	#	#	#	#	WATTR[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	WMSB[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	WLSB[7:0]	00H
19	Temperature Sensor Read (TSR)	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**		**43H**
		1	1	#	#	#	#	#	#	#	#	RMSB[7:0]	00H
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00H
20	Panel Break Check (PBC)	0	0	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**0**		**44H**
		1	1	--	--	--	--	--	--	--	#	PSTA	00H
21	VCOM and data interval setting (CDI)	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**		**50H**
		0	1	#	#	#	#	#	#	#	#	VBD[1:0], DDX[1:0], CDI[3:0]	D7H
22	Lower Power Detection (LPD)	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**		**51H**
		1	1	--	--	--	--	--	--	--	#	LPD	01H
23	TCON setting (TCON)	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**		**60H**
		0	1	#	#	#	#	#	#	#	#	S2G[3:0], G2S[3:0]	22H
24	Resolution setting (TRES)	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**1**		**61H**
		0	1	#	#	#	#	#	0	0	0	HRES[7:3]	00H
		0	1	--	--	--	--	--	--	--	#	VRES[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
25	Gate/Source Start setting (GSST)	0	0	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**1**		**65H**
		0	1	#	#	#	#	#	0	0	0	HST[7:3]	00H
		0	1	--	--	--	--	--	--	--	#	VST[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
26	Revision (REV)	0	0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**		**70H**
		1	1	#	#	#	#	#	#	#	#	LUT_REV[7:0]	FFH
		1	1	--	--	--	--	#	#	#	#	CHIP_REV[3:0]	0DH
27	Get Status (FLG)	0	0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**1**		**71H**
		1	1	--	#	#	#	#	#	#	#	PTL_FLAG ,I²C_ERR, I²C_BUSYN, DATA_FLAG, PON, POF, BUSY_N	13H
28	Auto Measurement VCOM (AMV)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**		**80H**
		0	1	--	--	#	#	#	#	#	#	AMVT[1:0], XON,AMVS, AMV, AMVE	10H
29	Read VCOM Value (VV)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**		**81H**
		1	1	--	--	#	#	#	#	#	#	VV[5:0]	00H
30	VCOM_DC Setting (VDCS)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**		**82H**
		0	1	--	--	#	#	#	#	#	#	VDCS[5:0]	00H
31	Partial Window (PTL)	0	0	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**		**90H**
		0	1	#	#	#	#	#	0	0	0	HRST[7:3]	00H
		0	1	#	#	#	#	#	1	1	1	HRED[7:3]	07H
		0	1	--	--	--	--	--	--	--	#	VRST[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
		0	1	--	--	--	--	--	--	--	#	VRED[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
		0	1	--	--	--	--	--	--	--	#	PT_SCAN	01H
32	Partial In (PTIN)	0	0	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**1**		**91H**
33	Partial Out (PTOUT)	0	0	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**0**		**92H**
34	Program Mode (PGM)	0	0	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**		**A0H**
35	Active Programming (APG)	0	0	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**1**		**A1H**

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
36	Read OTP (ROTP)	0	0	1	0	1	0	0	0	1	0		A2H
		1	1	--	--	--	--	--	--	--	--	Read Dummy	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = 000h	N/A
		1	1	:	:	:	:	:	:	:	:	:	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = n	N/A
37	Cascade Setting (CCSET)	0	0	1	1	1	0	0	0	0	0		E0H
		0	1	--	--	--	--	--	--	#	#	TSFIX, CCEN	00H
38	Power Saving (PWS)	0	0	1	1	1	0	0	0	1	1		E3H
		0	1	#	#	#	#	#	#	#	#	VCOM_W[3:0], SD_W[3:0]	00H
39	LVD Voltage Select (LVSEL)	0	0	1	1	1	0	0	1	0	0		E4H
		0	1	--	--	--	--	--	--	#	#	LVD_SEL[1:0]	03H
40	Force Temperature (TSSET)	0	0	1	1	1	0	0	1	0	1		E5H
		0	1	#	#	#	#	#	#	#	#	TS_SET[7:0]	00H

Note: (1) All other register addresses are invalid or reserved by UltraChip, and should NOT be used.

(2) Any bits shown here as 0 must be written with a 0. All unused bits should also be set to zero. Device malfunction may occur if this is not done.

(3) Commands are processed on the 'stop' condition of the interface.

(4) Registers marked 'W/R' can be read, but the contents are written when the SPI command completes – so the contents can be read and altered. The user can subsequently write the register to restore the contents following an SPI read.

COMMAND DESCRIPTION

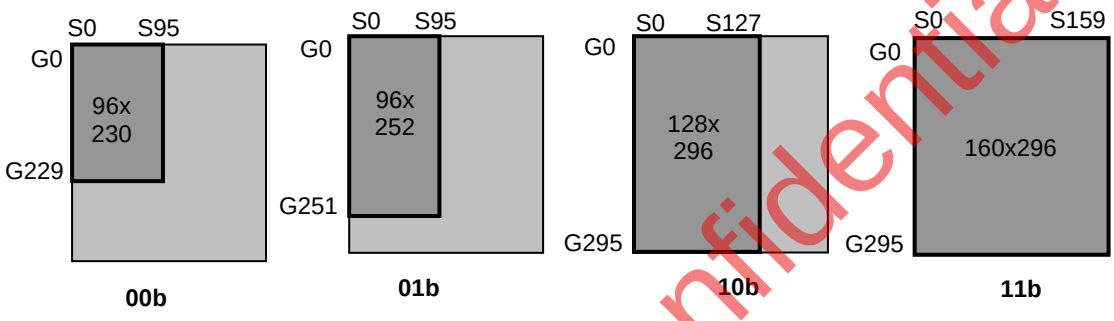
W/R: 0: Write Cycle / 1: Read Cycle C/D: 0: Command / 1: Data D7-D0: –: Don't Care

(1) PANEL SETTING (PSR) (REGISTER: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting the panel	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	00H
	0	1	RES1	RES0	REG	KW/R	UD	SHL	SHD_N	RST_N	0FH

RES[1:0]: Display Resolution setting (source x gate)

00b: 96x230 (Default) Active source channels: S0 ~ S95. Active gate channels: G0 ~ G229.
01b: 96x252 Active source channels: S0 ~ S95. Active gate channels: G0 ~ G251.
10b: 128x296 Active source channels: S0 ~ S127. Active gate channels: G0 ~ G295.
11b: 160x296 Active source channels: S0 ~ S159. Active gate channels: G0 ~ G295.



(1) Minimum active GD is always G0 regardless of <UD>(R00H).
(2) Minimum active SD is always S0 regardless of <SHL>(R00H).

maximum resolution
active resolution

REG: LUT selection

0: LUT from OTP. (Default)
1: LUT from register.

KW/R: Black / White / Red

0: Pixel with Black/White/Red, KWR mode. (Default)
1: Pixel with Black/White, KW mode.

UD: Gate Scan Direction

0: Scan down. First line to Last line: Gn-1 → Gn-2 → Gn-3 → … → G0
1: Scan up. (Default) First line to Last line: G0 → G1 → G2 → … … . → Gn-1

SHL: Source Shift Direction

0: Shift left. First data to Last data: Sn-1 → Sn-2 → Sn-3 → … → S0
1: Shift right. (Default) First data to Last data: S0 → S1 → S2 → … … . → Sn-1

SHD_N: Booster Switch

0: Booster OFF
1: Booster ON (Default)

When SHD_N becomes LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF. And Source/Gate/Border/VCOM will be released to floating.

RST_N: Soft Reset

0: Reset. Booster OFF, Register data are set to their default values, all drivers will be reset, and all functions will be disabled. Source/Gate/Border/VCOM will be released to floating.

1: No effect (Default).

(2) POWER SETTING (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Selecting Internal/External Power	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	01H
	0	1	-	-	-	-	-	-	VDS_EN	VDG_EN	03H
	0	1	-	-	-	-	-	VCOM_HV	VGHL_LV[1:0]		00H
	0	1	-	-	VDH[5:0]						26H
	0	1	-	-	VDL[5:0]						26H
	0	1	-	-	VDHR[5:0]						03H

VDS_EN: Source power selection
0 : External source power from VDH/VDL/VDHR pins
1 : Internal DC/DC function for generating VDH/VDL/VDHR. (Default)

VDG_EN: Gate power selection
0 : External gate power from VGH/VGL pins
1 : Internal DC/DC function for generating VGH/VGL. (Default)

VCOM_HV: VCOM Voltage Level
0 : VCOMH=VDH+VCOM_DC, VCOML=VDL+VCOM_DC. (Default)
1 : VCOMH=VGH, VCOML=VGL

VGHL_LV[1:0]: VGH / VGL Voltage Level selection.

VGHL_LV	VGHL Voltage Level
00 (Default)	VGH=20V, VGL= -20V
01	VGH=19V, VGL= -19V
10	VGH=18V, VGL= -18V
11	VGH=17V, VGL= -17V

VDH[5:0]: Internal VDH power selection for B/W pixel.(**Default value: 100110b**)

VDH	Voltage	VDH	Voltage	VDH	Voltage	VDH	Voltage
000000	6.4 V	001100	8.8 V	011000	11.2 V	100100	13.6 V
000001	6.6 V	001101	9.0 V	011001	11.4 V	100101	13.8 V
000010	6.8 V	001110	9.2 V	011010	11.6 V	**100110**	**14.0 V**
000011	7.0 V	001111	9.4 V	011011	11.8 V	100111	14.2 V
000100	7.2 V	010000	9.6 V	011100	12.0 V	101000	14.4 V
000101	7.4 V	010001	9.8 V	011101	12.2 V	101001	14.6 V
000110	7.6 V	010010	10.0 V	011110	12.4 V	101010	14.8 V
000111	7.8 V	010011	10.2 V	011111	12.6 V	101011	15.0 V
001000	8.0 V	010100	10.4 V	100000	12.8 V	(others)	15.0 V
001001	8.2 V	010101	10.6 V	100001	13.0 V		
001010	8.4 V	010110	10.8 V	100010	13.2 V		
001011	8.6 V	010111	11.0 V	100011	13.4 V		

VDL[5:0]: Internal VDL power selection for B/W pixel. (**Default value: 100110b**)

VDL	Voltage	VDL	Voltage	VDL	Voltage	VDL	Voltage
000000	-6.4 V	001100	-8.8 V	011000	-11.2 V	100100	-13.6 V
000001	-6.6 V	001101	-9.0 V	011001	-11.4 V	100101	-13.8 V
000010	-6.8 V	001110	-9.2 V	011010	-11.6 V	**100110**	**-14.0 V**
000011	-7.0 V	001111	-9.4 V	011011	-11.8 V	100111	-14.2 V
000100	-7.2 V	010000	-9.6 V	011100	-12.0 V	101000	-14.4 V
000101	-7.4 V	010001	-9.8 V	011101	-12.2 V	101001	-14.6 V
000110	-7.6 V	010010	-10.0 V	011110	-12.4 V	101010	-14.8 V
000111	-7.8 V	010011	-10.2 V	011111	-12.6 V	101011	-15.0 V
001000	-8.0 V	010100	-10.4 V	100000	-12.8 V	(others)	-15.0 V
001001	-8.2 V	010101	-10.6 V	100001	-13.0 V		
001010	-8.4 V	010110	-10.8 V	100010	-13.2 V		
001011	-8.6 V	010111	-11.0 V	100011	-13.4 V		

VDHR[5:0]: Internal VDHR power selection for Red pixel. (**Default value: 000011b**)

VDHR	Voltage	VDHR	Voltage	VDHR	Voltage	VDHR	Voltage
000000	2.4 V	001100	4.8 V	011000	7.2 V	100100	9.6 V
000001	2.6 V	001101	5.0 V	011001	7.4 V	100101	9.8 V
000010	2.8 V	001110	5.2 V	011010	7.6 V	100110	10.0V
000011	**3.0 V**	001111	5.4 V	011011	7.8 V	100111	10.2 V
000100	3.2 V	010000	5.6 V	011100	8.0 V	101000	10.4 V
000101	3.4 V	010001	5.8 V	011101	8.2V	101001	10.6 V
000110	3.6 V	010010	6.0 V	011110	8.4 V	101010	10.8 V
000111	3.8 V	010011	6.2 V	011111	8.6 V	101011	11.0 V
001000	4.0 V	010100	6.4 V	100000	8.8 V	(others)	11.0 V
001001	4.2 V	010101	6.6 V	100001	9.0 V		
001010	4.4 V	010110	6.8 V	100010	9.2 V		
001011	4.6 V	010111	7.0 V	100011	9.4 V		

(3) POWER OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning OFF the power	0	0	0	0	0	0	0	0	1	0	02H

After the Power OFF command, the driver will be powered OFF. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn off booster, controller, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD turned OFF or Deep Sleep Mode. Source/Gate/Border/VCOM will be released to floating.

(4) POWER OFF SEQUENCE SETTING (PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1	03H
	0	1	-	-	T_VDS_OFF[1:0]		-	-	-	-	00H

T_VDS_OFF[1:0]: Source to gate power off interval time.

00b: 1 frame (Default) 01b: 2 frames 10b: 3 frames 11b: 4 frame

(5) POWER ON (PON) (REGISTER: R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning ON the power	0	0	0	0	0	0	0	1	0	0	04H

After the Power ON command, the driver will be powered ON. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn on booster, controller, regulators, and temperature sensor will be activated for one-time sensing before enabling booster. When all voltages are ready, the BUSY_N signal will return to high.

(6) POWER ON MEASURE (PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
	0	0	0	0	0	0	0	1	0	1	05H

This command enables the internal bandgap, which will be cleared by the next POF.

(7) BOOSTER SOFT START (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	06H
	0	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0	17H
	0	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0	17H
	0	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0	17H

BTPHA[7:6]: Soft start period of phase A.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHA[5:3]: Driving strength of phase A

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHA[2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHB[7:6]: Soft start period of phase B.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHB[5:3]: Driving strength of phase B

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHB[2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHC[5:3]: Driving strength of phase C

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHC[2:0]: Minimum OFF time setting of GDR in phase C

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

(8) DEEP SLEEP (DSLP) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Deep Sleep	0	0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	07H
	0	1	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	A5H

After this command is transmitted, the chip will enter Deep Sleep Mode to save power. Deep Sleep Mode will return to Standby Mode by hardware reset. The only one parameter is a check code, the command will be executed if check code = 0xA5.

(9) DATA START TRANSMISSION 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	10H
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	00H
	0	1	:	:	:	:	:	:	:	:	00H
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	00H

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes “OLD” data to SRAM.

In KWR mode, this command writes “B/W” data to SRAM.

In Program mode, this command writes “OTP” data to SRAM for programming.

(10) DATA STOP (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Stopping data transmission	0	0	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**1**	11H
	1	1	data_flag	-	-	-	-	-	-	-	00H

Check the completeness of data. If data is complete, start to refresh display.

Data_flag: Data flag of receiving user data.

0: Driver didn’t receive all the data.
1: Driver has already received all the one-frame data (DTM1 and DTM2).

After “Data Start” (R10h) or “Data Stop” (R11h) commands and when data_flag=1, the refreshing of panel starts and BUSY_N signal will become “0”.

(11) DISPLAY REFRESH (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Refreshing the display	0	0	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	12H

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.

After Display Refresh command, BUSY_N signal will become “0” and the refreshing of panel starts.

The waiting interval form BUSY_N falling to the first FLG command must be larger than 200uS.

(12) DATA START TRANSMISSION 2 (DTM2) (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**1**	13H
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	00H
	0	1	:	:	:	:	:	:	:	:	00H
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	00H

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes “NEW” data to SRAM.

In KWR mode, this command writes “RED” data to SRAM.

(13) AUTO SEQUENCE (AUTO) (R17H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Auto Sequence	0	0	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**1**	17H
	0	1	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	A5H

The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP.

AUTO (0x17) + Code(0xA5) = (PON → DRF → POF)

AUTO (0x17) + Code(0xA7) = (PON → DRF → POF → DSLP)

(14) LUT OPTION (LUTOPT) (R2AH)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
LUT Option	0	0	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	2AH
	0	1	**-**	**-**	STATE_XON[5:0]						00H
	0	1	**-**	**-**	EXS[2:0]		**-**	DMS[2:0]			00H

This command sets XON and the 2 options of KWR mode's LUT.

STATE_XON[5:0]:

All Gate ON (Each bit controls one state, STATE_XON [0] for state-1, STATE_XON [1] for state-2 …..)

00 0000b: no All-Gate-ON

00 0001b: State-1 All-Gate-ON

00 0011b: State-1 and State2 All-Gate-ON

: :

DMS[2:0]: Dummy state position. The option is only available when KW/R=0.

EXS[1:0]: Extra state number. The option is only available when KW/R=0.

(15) PLL CONTROL (PLL) (R30H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Controlling PLL	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	30H
	0	1	-	-	M[2:0]			N[2:0]			3CH

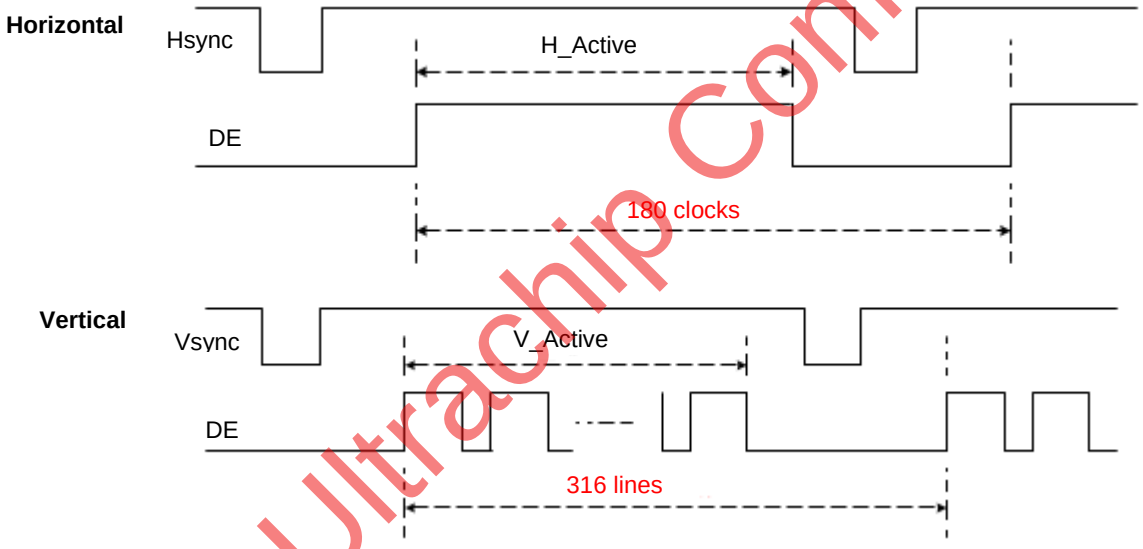
The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

M	N	Frame rate
1	1	29 Hz
	2	14 Hz
	3	10 Hz
	4	7 Hz
	5	6 Hz
	6	5 Hz
	7	4 Hz
2	1	57 Hz
	2	29 Hz
	3	19 Hz
	4	14 Hz
	5	11 Hz
	6	10 Hz
	7	8 Hz

M	N	Frame rate
3	1	86 Hz
	2	43 Hz
	3	29 Hz
	4	21 Hz
	5	17 Hz
	6	14 Hz
	7	12 Hz
4	1	114 Hz
	2	57 Hz
	3	38 Hz
	4	29 Hz
	5	23 Hz
	6	19 Hz
	7	16 Hz

M	N	Frame rate
5	1	150 Hz
	2	72 Hz
	3	48Hz
	4	36 Hz
	5	29 Hz
	6	24 Hz
	7	20 Hz
6	1	171 Hz
	2	86 Hz
	3	57 Hz
	4	43 Hz
	5	34 Hz
	6	29 Hz
	7	24 Hz

M	N	Frame rate
7	1	200 Hz
	2	100 Hz
	3	67 Hz
	4	**50 Hz (default)**
	5	40 Hz
	6	33 Hz
	7	29 Hz



(16) TEMPERATURE SENSOR CALIBRATION (TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Sensing Temperature	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	40H
	1	1	D10/TS7	D9/TS6	D8/TS5	D7/TS4	D6 / TS3	D5 / TS2	D4 / TS1	D3 / TS0	00H
	1	1	D2	D1	D0	-	-	-	-	-	00H

This command enables internal or external temperature sensor, and reads the result.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

TS[7:0]/D[10:3]	Temperature (°C)
1110_0111	-25
1110_1000	-24
1110_1001	-23
1110_1010	-22
1110_1011	-21
1110_1100	-20
1110_1101	-19
1110_1110	-18
1110_1111	-17
1111_0000	-16
1111_0001	-15
1111_0010	-14
1111_0011	-13
1111_0100	-12
1111_0101	-11
1111_0110	-10
1111_0111	-9
1111_1000	-8
1111_1001	-7
1111_1010	-6
1111_1011	-5
1111_1100	-4
1111_1101	-3
1111_1110	-2
1111_1111	-1

TS[7:0]/D[10:3]	Temperature(°C)
0000_0000	**0**
0000_0001	1
0000_0010	2
0000_0011	3
0000_0100	4
0000_0101	5
0000_0110	6
0000_0111	7
0000_1000	8
0000_1001	9
0000_1010	10
0000_1011	11
0000_1100	12
0000_1101	13
0000_1110	14
0000_1111	15
0001_0000	16
0001_0001	17
0001_0010	18
0001_0011	19
0001_0100	20
0001_0101	21
0001_0110	22
0001_0111	23
0001_1000	24

TS[7:0]/D[10:3]	Temperature(°C)
0001_1001	25
0001_1010	26
0001_1011	27
0001_1100	28
0001_1101	29
0001_1110	30
0001_1111	31
0010_0000	32
0010_0001	33
0010_0010	34
0010_0011	35
0010_0100	36
0010_0101	37
0010_0110	38
0010_0111	39
0010_1000	40
0010_1001	41
0010_1010	42
0010_1011	43
0010_1100	44
0010_1101	45
0010_1110	46
0010_1111	47
0011_0000	48
0011_0001	49

(17) TEMPERATURE SENSOR ENABLE (TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enable Temperature Sensor /Offset	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	41H
	0	1	TSE	-	-	-	TO[3:0]				00H

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable (default) 1: Disable; using external sensor.

TO[3:0]: Temperature offset.

TO[3:0]	Calculation
0000 b	**+0 (Default)**
0001	+1
0010	+2
0011	+3
0100	+4
0101	+5
0110	+6
0111	+7

TO[3:0]	Calculation
1000	-8
1001	-7
1010	-6
1011	-5
1100	-4
1101	-3
1110	-2
1111	-1

(18) TEMPERATURE SENSOR WRITE (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Write External Temperature Sensor	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	42H
	0	1	WATTR[7:0]								00H
	0	1	WMSB[7:0]								00H
	0	1	WLSB[7:0]								00H

This command writes the temperature sensed by the temperature sensor.

WATTR[7:6]: I^2C Write Byte Number

00b : 1 byte (head byte only)
01b : 2 bytes (head byte + pointer)
10b : 3 bytes (head byte + pointer + 1st parameter)
11b : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

WATTR[5:3]: User-defined address bits (A2, A1, A0)

WATTR[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor

WLSB[7:0]: LSByte of write-data to external temperature sensor

(19) TEMPERATURE SENSOR READ (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read External Temperature Sensor	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	43H
	1	1	RMSB[7:0]								00H
	1	1	RLSB[7:0]								00H

This command reads the temperature sensed by the temperature sensor.

RMSB[7:0]: MSByte read data from external temperature sensor

RLSB[7:0]: LSByte read data from external temperature sensor

(20) PANEL GLASS CHECK (PBC)

Action	R/W	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Check Panel Glass	W	0	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**0**	44H
	R	1	-	-	-	-	-	-	-	PSTA	00H

This command is used to enable panel check, and to disable after reading result.

PSTA: 0: Panel check fail (panel broken) 1: Panel check pass

(21) VCOM AND DATA INTERVAL SETTING (CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Interval between VCOM and Data	0	0	0	1	0	1	0	0	0	0	50h
	0	1	VBD[1:0]		DDX[1:0]		CDI[3:0]				D7h

This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

VBD[1:0]: Border data selection

KWR mode (KW/R=0)

DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTR
	10	LUTW
	11	LUTB
1 (Default)	00	LUTB
	01	LUTW
	10	LUTR
	11	Floating

KW mode (KW/R=1)

DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTBW (1 → 0)
	10	LUTWB (0 → 1)
	11	Floating
1 (Default)	00	Floating
	01	LUTWB (1 → 0)
	10	LUTBW (0 → 1)
	11	Floating

DDX[1:0]: Data polality.

Under KWR mode (KW/R=0):

DDX[1] is for RED data.
DDX[0] is for B/W data,

DDX[1:0]	Data {Red, B/W}	LUT
00	00	LUTW
	01	LUTB
	10	LUTR
	11	LUTR
01 (Default)	00	LUTB
	01	LUTW
	10	LUTR
	11	LUTR

DDX[1:0]	Data {Red, B/W}	LUT
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTB
11	00	LUTR
	01	LUTR
	10	LUTB
	11	LUTW

Under KW mode (KW/R=1):

DDX[1]=0 is for KW mode with NEW/OLD,
DDX[1]=1 is for KW mode without NEW/OLD.

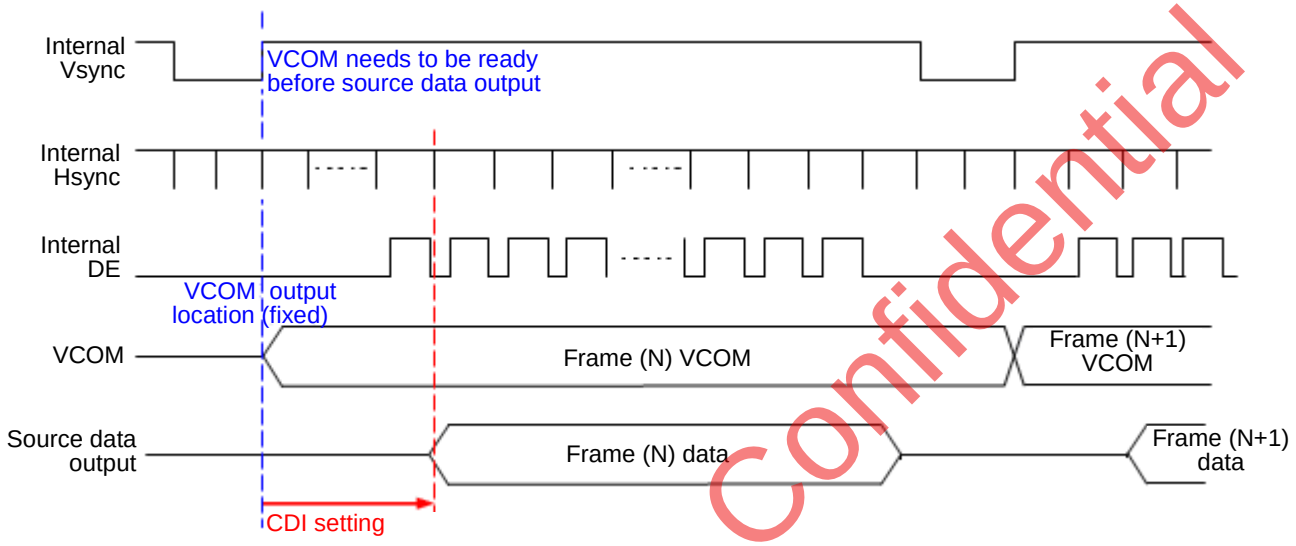
DDX[1:0]	Data {NEW, OLD}	LUT
00	00	LUTWW (0 → 0)
	01	LUTBW (1 → 0)
	10	LUTWB (0 → 1)
	11	LUTBB (1 → 1)
01 (Default)	00	LUTBB (0 → 0)
	01	LUTWB (1 → 0)
	10	LUTBW (0 → 1)
	11	LUTWW (1 → 1)

DDX[1:0]	Data {NEW}	LUT
10	0	LUTBW (1 → 0)
	1	LUTWB (0 → 1)
11	0	LUTWB (1 → 0)
	1	LUTBW (0 → 1)

CDI[3:0]: VCOM and data interval

CDI[3:0]	VCOM and Data Interval
0000 b	17 hsync
0001	16
0010	15
0011	14
0100	13
0101	12
0110	11
0111	**10 (Default)**

CDI[3:0]	VCOM and Data Interval
1000	9
1001	8
1010	7
1011	6
1100	5
1101	4
1110	3
1111	2



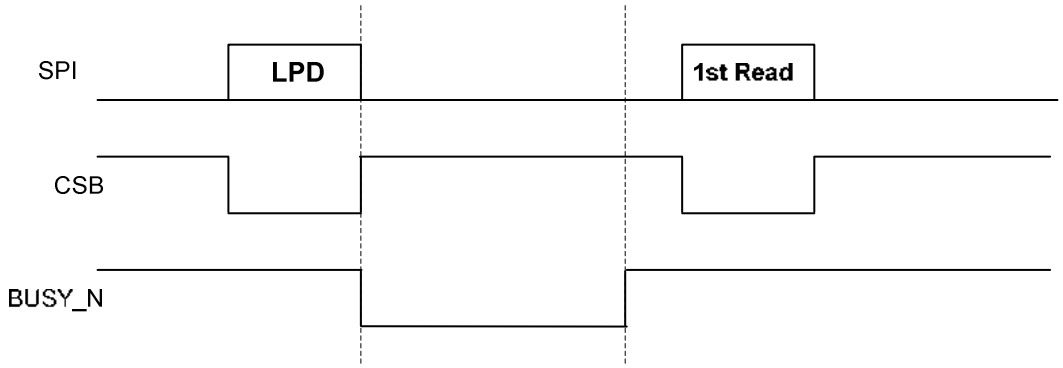
(22) LOW POWER DETECTION (LPD) (R51H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Detect Low Power	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**	51h
	1	1	-	-	-	-	-	-	-	LPD	01h

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal Low Power Detection Flag

0: Low power input (V_{DD}<2.5V, selected by LVD_SEL[1:0] in command LVSEL)
1: Normal status (default)



(23) TCON SETTING (TCON) (R60H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Non-overlap Period	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	60h
	0	1	S2G[3:0]				G2S[3:0]				22h

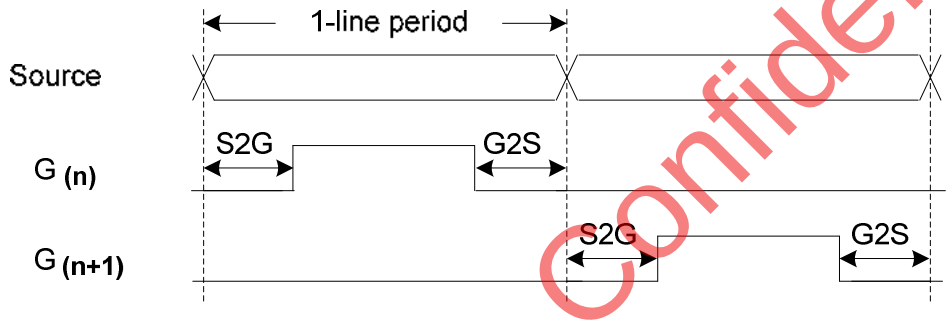
This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period
0000 b	4
0001	8
0010	**12 (Default)**
0011	16
0100	20
0101	24
0110	28
0111	32

S2G[3:0] or G2S[3:0]	Period
1000 b	36
1001	40
1010	44
1011	48
1100	52
1101	56
1110	60
1111	64

Period Unit = 660 nS.



(24) RESOLUTION SETTING (TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display Resolution	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**1**	61h
	0	1	HRES[7:3]					**0**	**0**	**0**	00h
	0	1	-	-	-	-	-	-	-	VRES[8]	00h
	0	1	VRES[7:0]								00h

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

HRES[7:3]: Horizontal Display Resolution

VRES[8:0]: Vertical Display Resolution

Active channel calculation:

Gate: First active gate = G0 (defined by GSST setting, default start gate is G0);
Last active gate = VRES[8:0] – 1

Source: First active source = S0 (defined by GSST setting, default start source is S0);
Last active source = HRES[7:3]*8 - 1

Example: 128 (source) x 272 (gate)

Gate: First active gate = G0 (default start gate),
Last active gate = 272 - 1= 271; (VRES[8:0] = 272, G271)

Source: First active source = S0 (default start source),
Last active source = 16*8 – 1 = 127; (HRES[7:3]=16, S127)

(25) GATE/SOURCE START SETTING (GSST) (R65H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Start	0	0	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**1**	65h
	0	1	HST[7:3]					**0**	**0**	**0**	00h
	0	1	-	-	-	-	-	-	-	VST[8]	00h
	0	1	VST[7:0]								00h

This command defines resolution start gate/source position.

HST[7:3]: Horizontal Display Start Position (Source)

VST[8:0]: Vertical Display Start Position (Gate)

Example : 128(Source) x 240(Gate)

HST[7:3] = 4 (HST = 4*8 = 32),

VST[8:0] = 32

Gate: First active gate = G32 (Because HST[7:3] = 4),
Last active gate = G271

Source: First active source = S32 (Because VST[8:0] = 32),
Last active source = S159

(26) REVISION (REV) (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Chip Revision	0	0	0	1	1	1	0	0	0	0	70h
	1	1	LUT_REV								FFh
	1	1	-	-	-	-	LUT_REV[3:0]				0Dh

The LUT_REV is read from OTP address = 0x001 / 0x801.

CHIP_REV[3:0]: Chip Revision, fixed at 1101b.

(27) GET STATUS (FLG) (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read Flags	0	0	0	1	1	1	0	0	0	1	71h
	1	1	-	PTL_ flag	I^2C_ERR	I^2C_ BUSYN	data_ flag	PON	POF	BUSY_N	13h

This command reads the IC status.

PTL_FLAG Partial display status (high: partial mode)

I^2C_ERR: I^2C master error status

I^2C_BUSYN: I^2C master busy status (low active)

data_flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY_N: Driver busy status (low active)

(28) AUTO MEASURE VCOM (AMV) (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure VCOM	0	0	1	0	0	0	0	0	0	0	80h
	0	1	-	-	AMVT[1:0]		XON	AMVS	AMV	AMVE	10h

This command reads the IC status.

AMVT[1:0]: Auto Measure VCOM Time

00b: 3s **01b: 5s (default)**
10b: 8s 11b: 10s

XON: All Gate ON of AMV

0: Gate normally scan during Auto Measure VCOM period. (default)
1: All Gate ON during Auto Measure VCOM period.

AMVS: Source output of AMV

0: Source output 0V during Auto Measure VCOM period. (default)
1: Source output VDHR during Auto Measure VCOM period.

AMV: Analog signal

0: Get VCOM value with the VV command (R81h) (default)
1: Get VCOM value in analog signal. (External analog to digital converter)

AMVE: Auto Measure VCOM Enable (/Disable)

0: No effect (default)
1: Trigger auto VCOM sensing.

(29) VCOM VALUE (VV) (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure VCOM	0	0	1	0	0	0	0	0	0	1	81h
	1	1	-	-	VV[5:0]						00h

This command gets the VCOM value.

VV[5:0]: VCOM Value Output

VV [5:0]	VCOM Voltage (V)	VV [5:0]	VCOM Voltage (V)	VV [5:0]	VCOM Voltage (V)
00 0000b	-0.10	01 0100b	-1.10	10 1000b	-2.10
00 0001b	-0.15	01 0101b	-1.15	10 1001b	-2.15
00 0010b	-0.20	01 0110b	-1.20	10 1010b	-2.20
00 0011b	-0.25	01 0111b	-1.25	10 1011b	-2.25
00 0100b	-0.30	01 1000b	-1.30	10 1100b	-2.30
00 0101b	-0.35	01 1001b	-1.35	10 1101b	-2.35
00 0110b	-0.40	01 1010b	-1.40	10 1110b	-2.40
00 0111b	-0.45	01 1011b	-1.45	10 1111b	-2.45
00 1000b	-0.50	01 1100b	-1.50	11 0000b	-2.50
00 1001b	-0.55	01 1101b	-1.55	11 0001b	-2.55
00 1010b	-0.60	01 1110b	-1.60	11 0010b	-2.60
00 1011b	-0.65	01 1111b	-1.65	11 0011b	-2.65
00 1100b	-0.70	10 0000b	-1.70	11 0100b	-2.70
00 1101b	-0.75	10 0001b	-1.75	11 0101b	-2.75
00 1110b	-0.80	10 0010b	-1.80	11 0110b	-2.80
00 1111b	-0.85	10 0011b	-1.85	11 0111b	-2.85
01 0000b	-0.90	10 0100b	-1.90	11 1000b	-2.90
01 0001b	-0.95	10 0101b	-1.95	11 1001b	-2.95
01 0010b	-1.00	10 0110b	-2.00	11 1010b	-3.00
01 0011b	-1.05	10 0111b	-2.05	11 1011b	-3.05

(30) VCOM_DC SETTING (VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set VCOM_DC	0	0	1	0	0	0	0	0	1	0	82h
	0	1	-	-	VDCS[5:0]						00h

This command sets VCOM_DC value

VDCS[5:0]: VCOM_DC Setting

VDCS [5:0]	VCOM Voltage (V)	VDCS [5:0]	VCOM Voltage (V)	VDCS [5:0]	VCOM Voltage (V)
00 0000b	-0.10	01 0100b	-1.10	10 1000b	-2.10
00 0001b	-0.15	01 0101b	-1.15	10 1001b	-2.15
00 0010b	-0.20	01 0110b	-1.20	10 1010b	-2.20
00 0011b	-0.25	01 0111b	-1.25	10 1011b	-2.25
00 0100b	-0.30	01 1000b	-1.30	10 1100b	-2.30
00 0101b	-0.35	01 1001b	-1.35	10 1101b	-2.35
00 0110b	-0.40	01 1010b	-1.40	10 1110b	-2.40
00 0111b	-0.45	01 1011b	-1.45	10 1111b	-2.45
00 1000b	-0.50	01 1100b	-1.50	11 0000b	-2.50
00 1001b	-0.55	01 1101b	-1.55	11 0001b	-2.55
00 1010b	-0.60	01 1110b	-1.60	11 0010b	-2.60
00 1011b	-0.65	01 1111b	-1.65	11 0011b	-2.65
00 1100b	-0.70	10 0000b	-1.70	11 0100b	-2.70
00 1101b	-0.75	10 0001b	-1.75	11 0101b	-2.75
00 1110b	-0.80	10 0010b	-1.80	11 0110b	-2.80
00 1111b	-0.85	10 0011b	-1.85	11 0111b	-2.85
01 0000b	-0.90	10 0100b	-1.90	11 1000b	-2.90
01 0001b	-0.95	10 0101b	-1.95	11 1001b	-2.95
01 0010b	-1.00	10 0110b	-2.00	11 1010b	-3.00
01 0011b	-1.05	10 0111b	-2.05	others	-3.00

(31) PARTIAL WINDOW (PTL) (R90H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Partial Window	0	0	1	0	0	0	0	0	1	0	90h
	0	1	HRST[7:3]					0	0	0	00h
	0	1	HRED[7:3]					1	1	1	07h
	0	1	-	-	-	-	-	-	-	VRST[8]	00h
	0	1	VRST[7:0]								00h
	0	1	-	-	-	-	-	-	-	VRED[8]	00h
	0	1	VRED[7:0]								00h
	0	1	-	-	-	-	-	-	-	PT_SCAN	01h

This command sets partial window.

HRST[7:3]: Horizontal start channel bank. (value 00h~13h)

HRED[7:3]: Horizontal end channel bank. (value 00h~13h). HRED must be greater than HRST.

VRST[8:0]: Vertical start line. (value 000h~127h)

VRED[8:0]: Vertical end line. (value 000h~127h). VRED must be greater than VRST.

PT_SCAN: 0: Gates scan only inside of the partial window.
1: Gates scan both inside and outside of the partial window. (default)

(32) PARTIAL IN (PTIN) (R91H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial In	0	0	1	0	0	1	0	0	0	1	91h

This command makes the display enter partial mode.

(33) PARTIAL OUT (PTOUT) (R92H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial Out	0	0	1	0	0	1	0	0	1	0	92h

This command makes the display exit partial mode and enter normal mode.

(34) PROGRAM MODE (PGM) (RA0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enter Program Mode	0	0	1	0	1	0	0	0	0	0	A0h

After this command is issued, the chip would enter the program mode.

After the programming procedure completed, a hardware reset is necessary for leaving program mode.

(35) ACTIVE PROGRAM (APG) (RA1H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Active Program OTP	0	0	1	0	1	0	0	0	0	1	A1h

After this command is transmitted, the programming state machine would be activated.

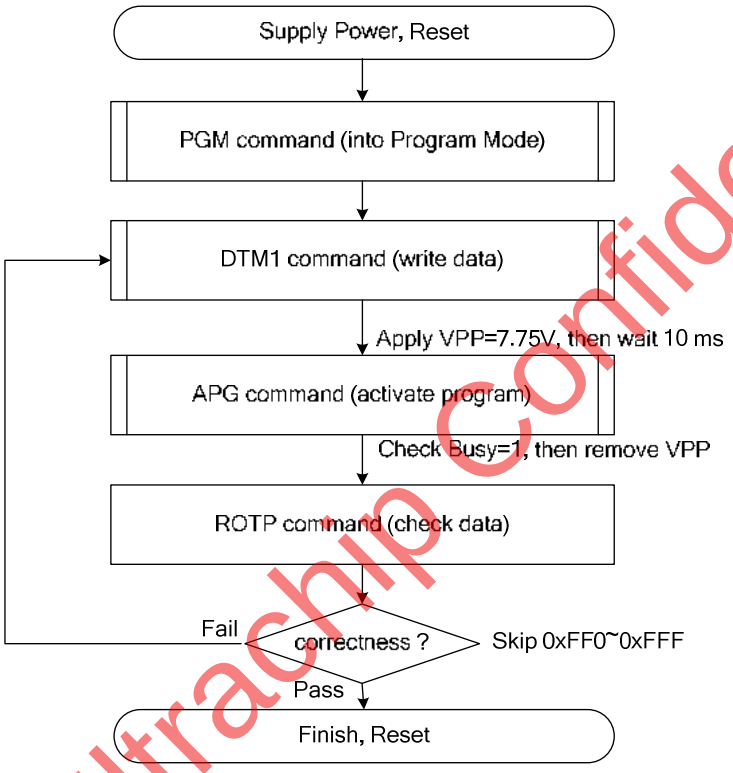
The BUSY_N flag would fall to 0 until the programming is completed.

(36) READ OTP DATA (ROTP) (RA2H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read OTP data for check	0	0	1	0	1	0	0	0	1	0	A2h
	1	1	Dummy								--
	1	1	The data of address 0x000 in the OTP								--
	1	1	The data of address 0x001 in the OTP								--
	1	1	:								--
	1	1	The data of address (n-1) in the OTP								--
	1	1	The data of address (n) in the OTP								--

The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, the max address = 0xFFF.



The sequence of programming OTP.

(37) CASCADE SETTING (CCSET) (RE0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Cascade Option	0	0	1	1	1	0	0	0	0	0	E0h
	0	1	-	-	-	-	-	-	TSFIX	CCEN	00h

This command is used for cascade.

CCEN: Output clock enable/disable.

0: Output 0V at CL pin. (default)

1: Output clock at CL pin for slave chip.

TSFIX: Let the value of slave's temperature is same as the master's.

0: Temperature value is defined by internal temperature sensor / external LM75. (default)

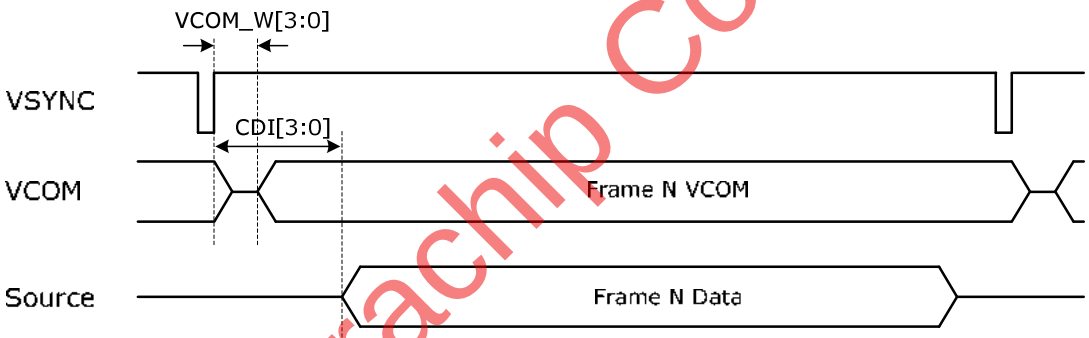
1: Temperature value is defined by TS_SET[7:0] registers.

(38) POWER SAVING (PWS) (RE3H)

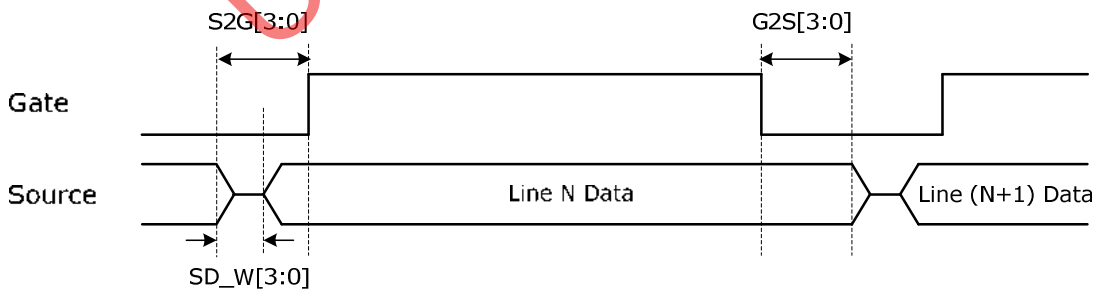
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Power Saving for VCOM & Source	0	0	1	1	1	0	0	0	1	1	E3h
	0	1	VCOM_W[3:0]				SD_W[3:0]				00h

This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W[3:0]: VCOM power saving width (unit = line period)



SD_W[3:0]: Source power saving width (unit = 660nS)



(39) LVD VOLTAGE SELECT (LVSEL) (RE4H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Select LVD Voltage	0	0	1	1	1	0	0	1	0	0	E4h
	0	1	-	-	-	-	-	-	LVD_SEL[1:0]		03h

LVD_SEL[1:0]: Low Power Voltage selection

LVD_SEL[1:0]	LVD value
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5 V (default)

(40) FORCE TEMPERATURE (TSSET) (RE5H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Force Temperature Value for Cascade	0	0	1	1	1	0	0	1	0	1	E5h
	0	1	TS_SET[7:0]								00h

This command is used for cascade to fix the temperature value of master and slave chip.

HOST INTERFACES

UC8151 provides 3-wire/4-wire serial interface for command and display data transferred from the MCU. The serial interface supports 8-bit mode. Data can be input/output by clocks while the chip is active (CSB =LOW). While input, data are written in order from MSB at the clock rising edge. When too many parameters are input, the chip accepts only defined parameters, and ignores undefined ones.

BS	Interface	CSB	DC	SCL	SDA
High	3-wire SPI	Available	Fix to GND	Available	Available
Low	4-wire SPI	Available	Available	Available	Available

3 wire SPI format

Data / Command is recognized with the first bit transferred. Data are transferred in the unit of 9 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 9 bits. (The serial counter is reset at the rising edge of the CSB signal.)

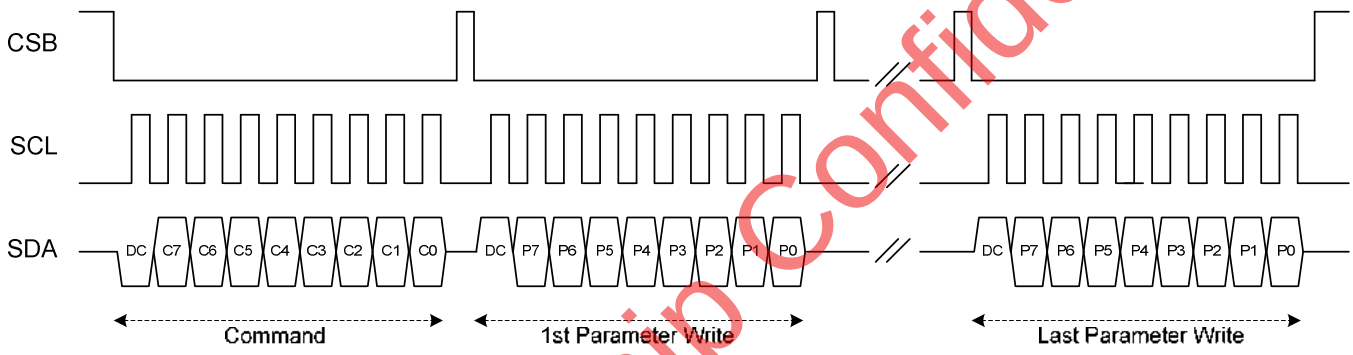


Figure: 3-wire SPI write operation

The MSB bit of data will be output at SDA pin after the 1st SCL falling edge, if the 1st input data at SDA is high. Only in the case of OTP data read, the 1st packet of output data are dummy data.

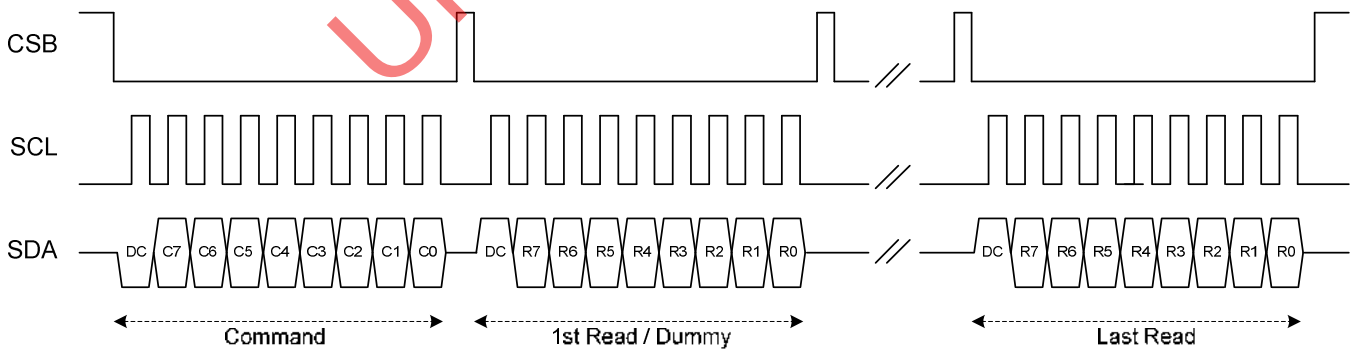


Figure: 3-wire SPI read operation

4 wire SPI format

Data / Command is recognized with DC pin. Data are transferred in the unit of 8 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 8 bits. (The serial counter is reset at the rising edge of the CSB signal.)

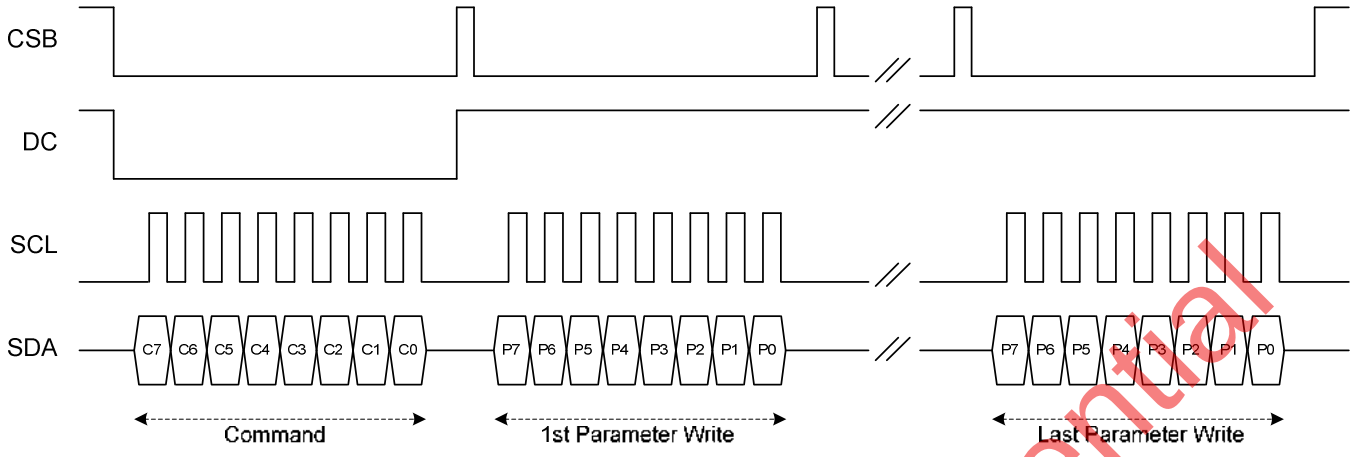


Figure: 4-wire SPI write operation

The MSB bit of data will be output at SDA pin after the CSB falling edge, if DC pin is High. Only in the case of OTP data read, the 1st packet of output data are dummy data.

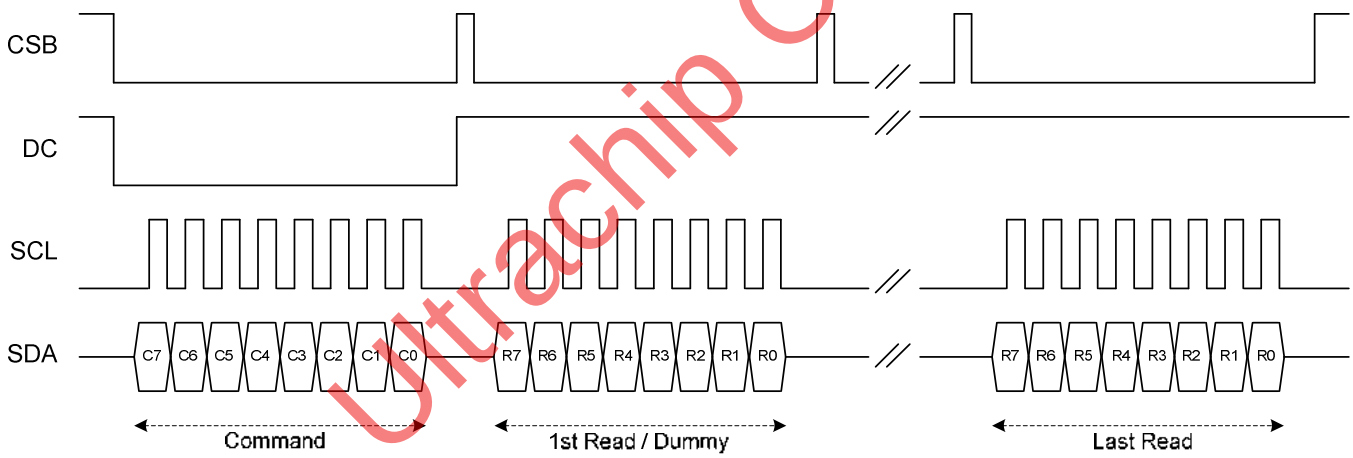
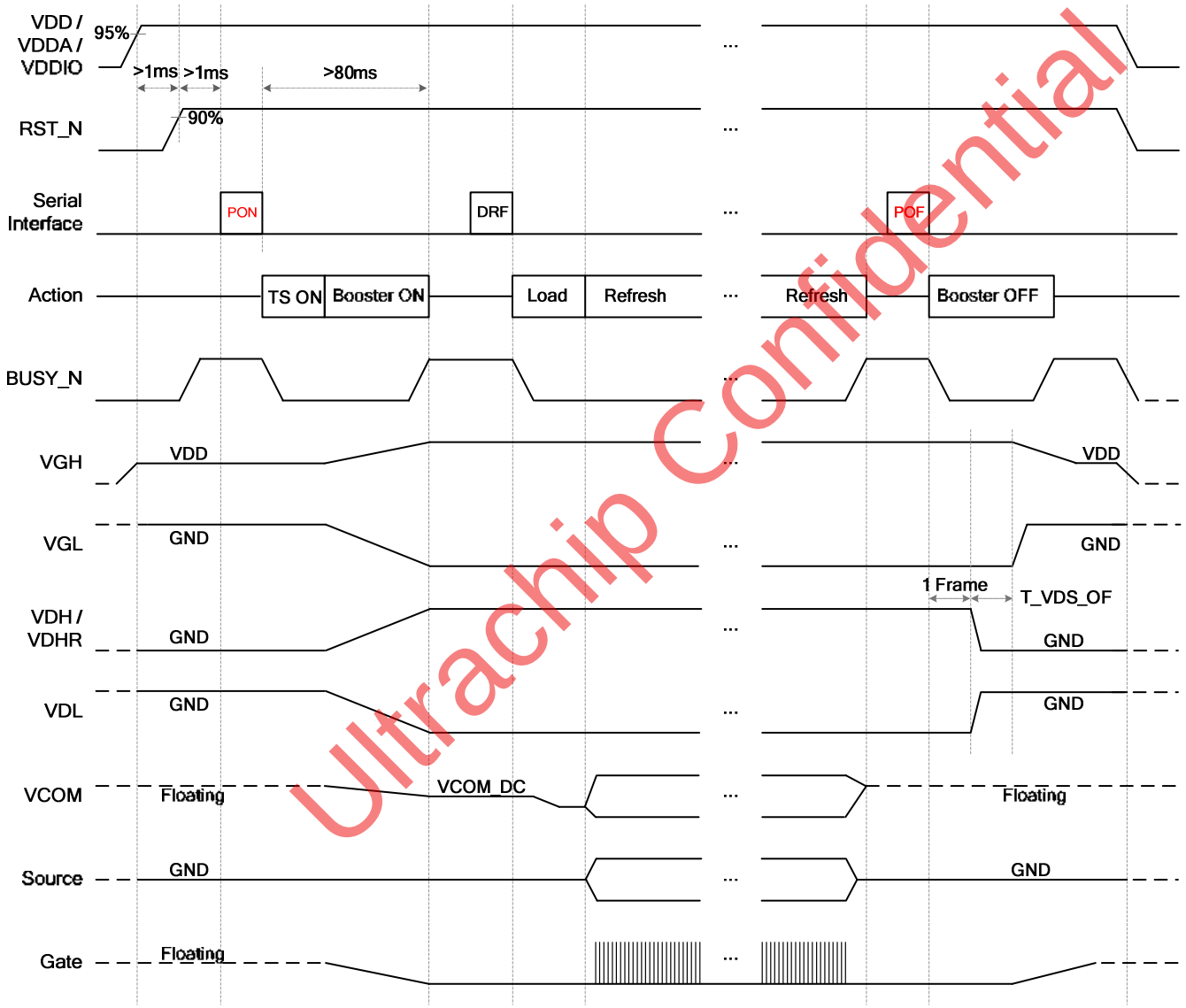


Figure: 4-wire SPI read operation

POWER MANAGEMENT

Power ON/OFF Sequence

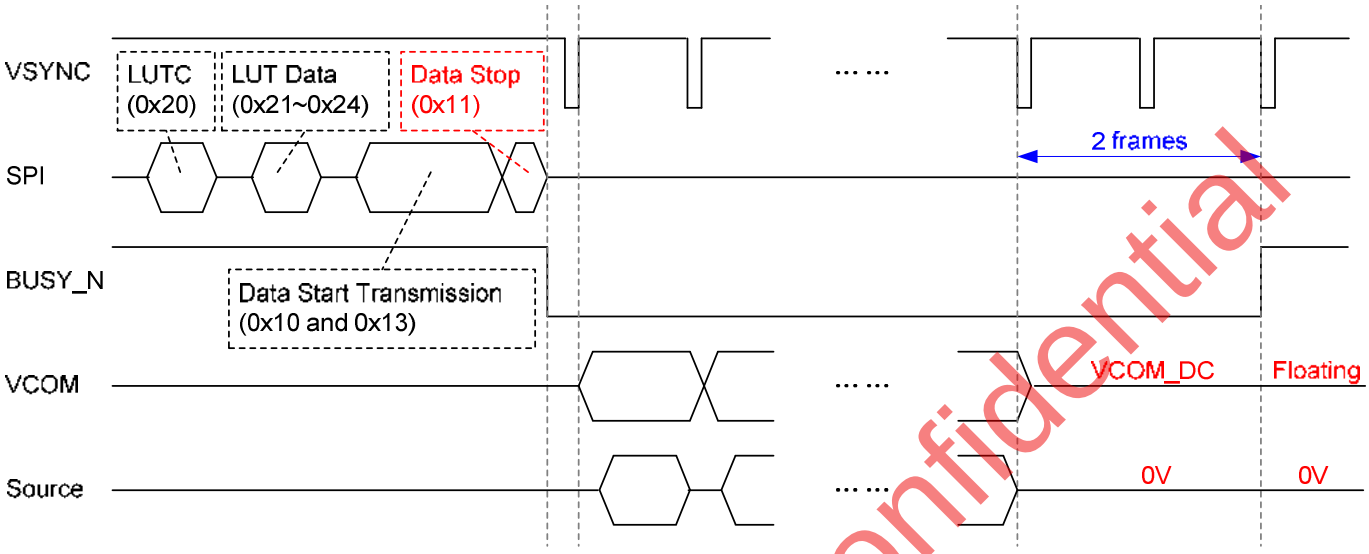
1. Temperature sensor will be activated automatically for one-time sensing before enabling booster.
2. After refreshing display, VCOM will be set to floating automatically.
3. In OTP mode (REG=0), the LUT in OTP will be copied to register automatically after the DSP/DRF command.
4. After RST_N rising, the waiting time for internal initial processing, greater than 1mS, is necessary. Any commands transmitted to chip during this time will be ignored.



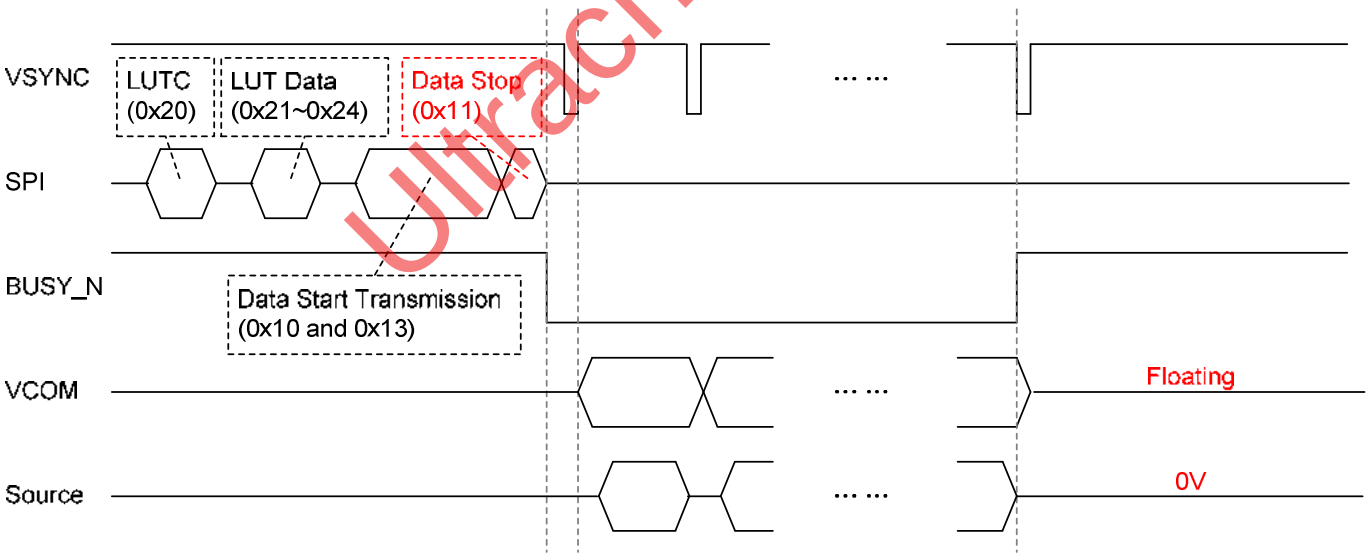
Data Transmission Waveform

Example 1: After 3 cases, the driver will send 2 frame VCOM and data to 0 V.

1. All 7 LUT states complete.
2. meet the state whose Times to Repeat =0
3. meet the state whose all Number of Frames =0



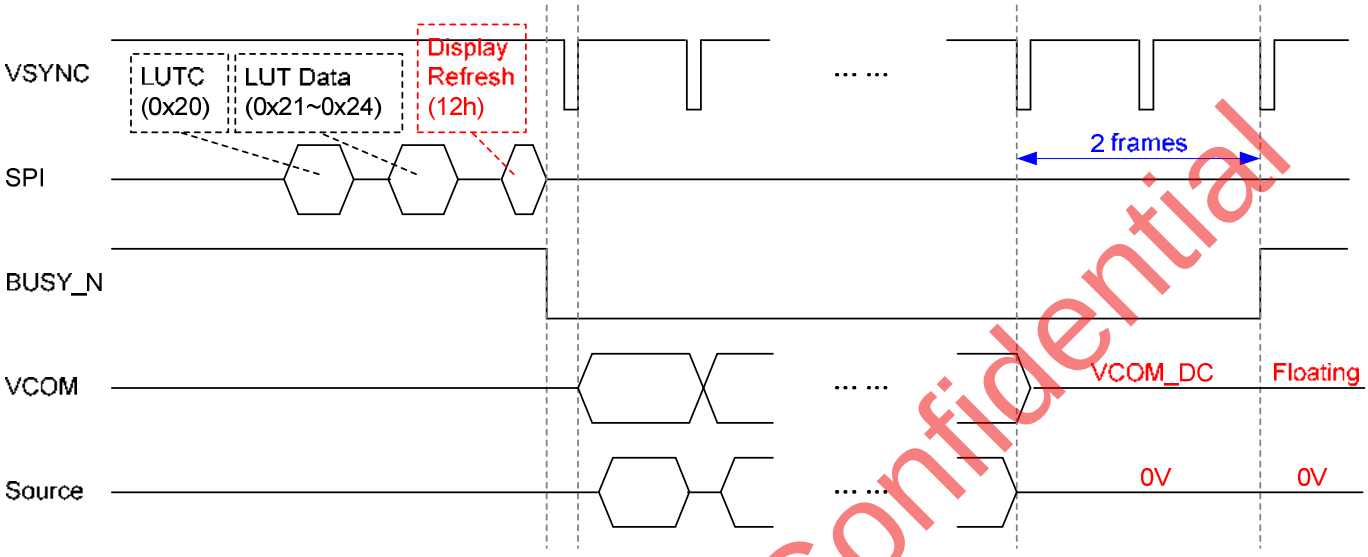
Example2: While level selection in LUT (LUTC only) is “1111_1111b”, the driver will float VCOM.



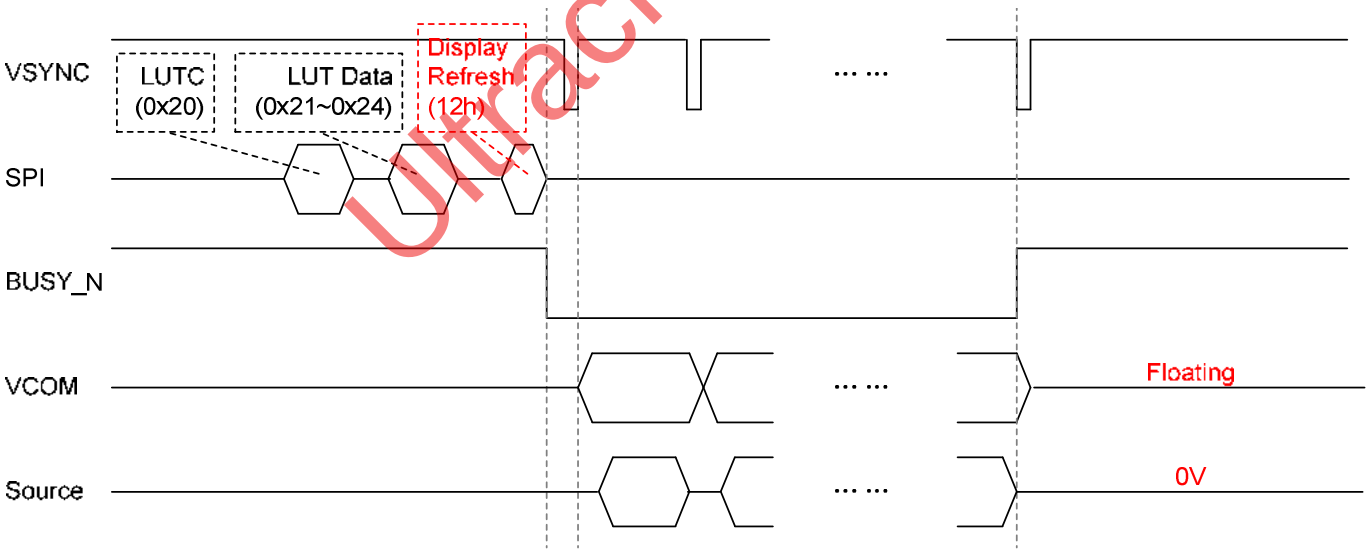
Display Refresh Waveform

Example 1: After three cases, the driver will send 2 frames VCOM and data to 0 V.

1. All 7 LUT states complete.
2. meet the state whose Times to Repeat = 0
3. meet the state whose all Number of Frames = 0



Example2: While level selection in LUT (LUTC only) is “1111_1111b”, the driver will float VCOM.



BUSY_N Signal

Commands, except reading command, are restricted by refreshing display (DRF / DSP) as listed in the following table.

BUSY_N is used to represent the status of internal action. Commands activating internal operation or calculation will cause BUSY_N falling to LOW. After actions completed, BUSY_N will return to HIGH.

Command	Refresh Restriction	BUSY_N flag
PSR	X	No action
PWR	X	No action
POF	X	Flag
PFS	X	No action
PON	X	Flag
PMES	X	Flag
BTST	X	No action
DSLP	X	Flag
AUTO	X	Flag
DTM1	X	No action
DSP	X	Flag
DRF	X	Flag
DTM2	X	No action
LUTC	X	No action
LUTWW	X	No action
LUTWB/LUTW	X	No action
LUTBW/LUTR	X	No action
LUTBB/LUTB	X	No action
LUTOPT	X	No action
PLL	X	No action
TSC	X	Flag
TSE	X	No action
TSW	X	No action
TSR	X	No action
PBC	X	No action
CDI	X	No action
LPD	X	Flag
TCON	X	No action
TRES	X	No action
GSST	X	No action
REV	V	No action
FLG	V	No action
AMV	X	Flag
VV	V	No action
VDCS	X	No action
PTL	X	No action
PTIN	X	No action
PTOUT	X	No action
PGM	X	No action
APG	X	Flag
ROTP	X	No action
CCSET	X	No action
PWS	X	No action
LVSEL	X	No action
TSSET	X	No action

V: Accepted, X: Ignored

TEMPERATURE RANGE

The temperature selection mechanism consists of a less-than-or-equal-to operator and 9 temperature boundary settings (TBx) to determine 10 temperature ranges. The sequence of mechanism is from TB0 to TB8, as shown below. If less than 10 tempeature ranges are used, the last TBx must be set to 0x7F to end the mechanism.

Procedure Order	Comparison Condition	Action & Segment Selection
1-0. Read 0x000	Content = 0xA5 ?	Yes: Jump to Procedure 2 (Bank0), No: Jump to Procedure 1-1
1-1, Read 0x800	Content = 0xA5 ?	Yes: Jump to Procedure 2 (Bank1), No: Stop Refresh
2. Read 0x002 / 0x802	Real Temperature ≦ TB0	Use TR0's table & setting, exit
3. Read 0x003 / 0x803	Real Temperature ≦ TB1	Use TR1's table & setting, exit
4. Read 0x004 / 0x804	Real Temperature ≦ TB2	Use TR2's table & setting, exit
5. Read 0x005 / 0x805	Real Temperature ≦ TB3	Use TR3's table & setting, exit
6. Read 0x006 / 0x806	Real Temperature ≦ TB4	Use TR4's table & setting, exit
7. Read 0x007 / 0x807	Real Temperature ≦ TB5	Use TR5's table & setting, exit
8. Read 0x008 / 0x808	Real Temperature ≦ TB6	Use TR6's table & setting, exit
9. Read 0x009 / 0x809	Real Temperature ≦ TB7	Use TR7's table & setting, exit
10. Read 0x00A / 0x80A	Real Temperature ≦ TB8	Use TR8's table & setting, exit
11. Other	Real Temperature > TB8	Use TR9's table & setting, finish

***Note:**

(1) TRx's content is defined in "LUT FORMAT IN OTP" section.

Example:

If temperature = -20 °C, TR0 is selected.

If temperature = -10 °C, TR1 is selected.

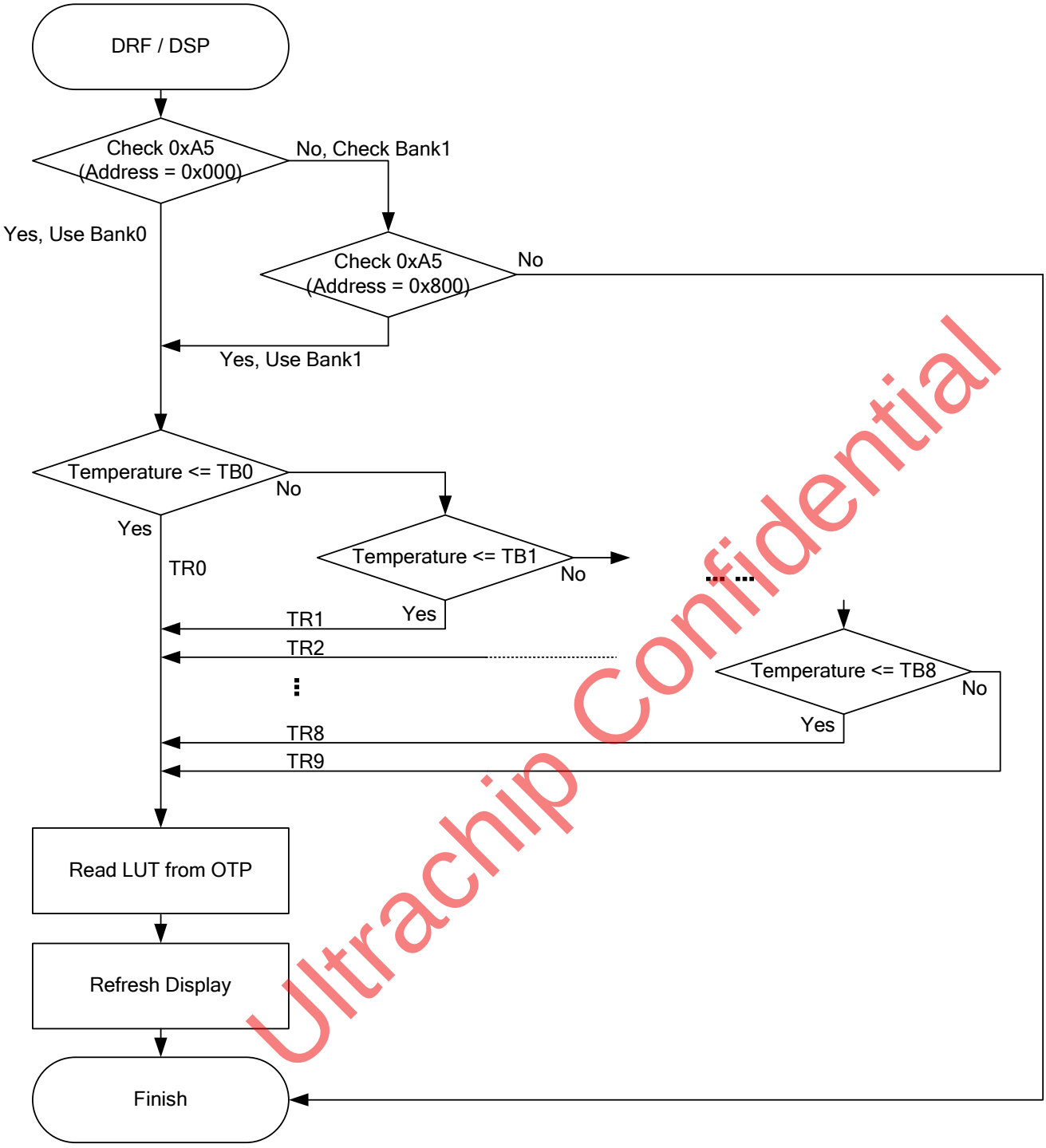
If temperature = 0 °C, TR2 is selected.

If temperature = 20 °C, TR4 is selected.

If temperature = 40 °C, TR5 is selected.

If temperature > 40 °C, TR5 is selected.

OTP Address	Content	
002h	0xF1	(-15 °C)
003h	0xFB	(-5 °C)
004h	0x00	(0 °C)
005h	0x0A	(10 °C)
006h	0x1E	(30 °C)
007h	0x7F	-



Temperature Selection Mechanism

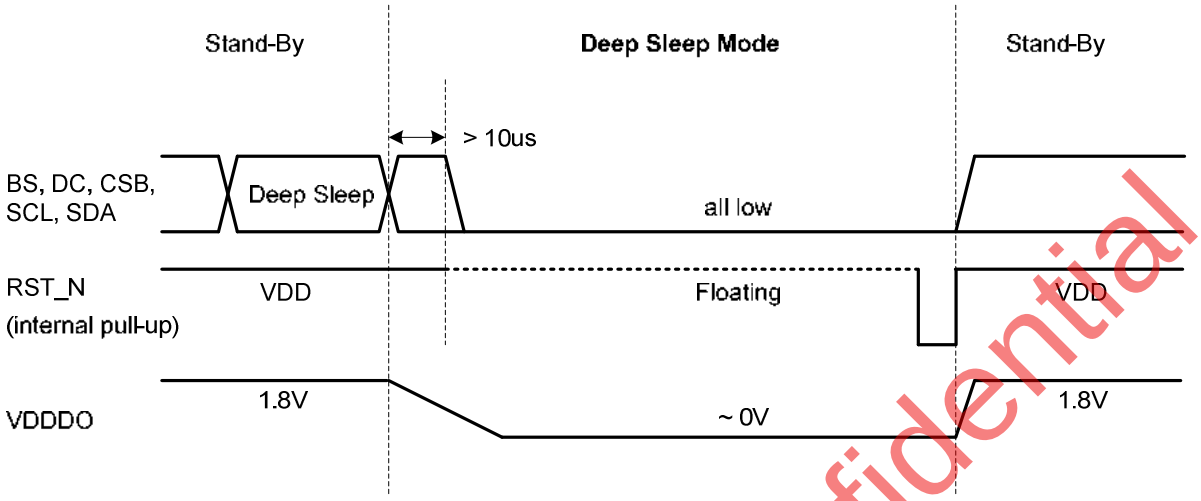
COMMAND DEFAULT SETTING

This function can modify the default value of command registers by the OTP content between address 0x00B~0x01D (or 0x80B~0x81D). The data of address 0x00B (or 0x80B) is the enable key of the function. Changing default value function is used to reduce the initial code length executed by the microcontroller.

Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0	Command	Registers	Original
0x00B	#	#	#	#	#	#	#	#	Check Code	0xA5 (Enable Key)	--
0x00C	#	#	#	#	#	#	--	--	PSR	RES[1:0], REG, KW/R, UD, SHL	0x0F
0x00D	--	--	#	#	--	--	--	--	PFS	T_VDS_OF[1:0]	0x00
0x00E	#	#	#	#	#	#	#	#	BTST	BT_PHA[7:0]	0x17
0x00F	#	#	#	#	#	#	#	#		BT_PHB[7:0]	0x17
0x010	--	--	#	#	#	#	#	#		BT_PHC[5:0]	0x17
0x011	#	--	--	--	#	#	#	#	TSE	TSE, TO[3:0]	0x00
0x012	#	#	#	#	#	#	#	#	CDI	VBD[1:0], DDX[1:0], CDI[3:0]	0xD7
0x013	#	#	#	#	#	#	#	#	TCON	S2G[3:0], G2S[3:0]	0x22
0x014	#	#	#	#	#	#	#	#	TRES	HRES[7:3]	0x00
0x015	--	--	--	--	--	--	--	#		VRES[8:0]	0x00
0x016	#	#	#	#	#	#	#	#			0x00
0x017	#	#	#	#	#	#	#	#	GSST	HST[7:3]	0x00
0x018	--	--	--	--	--	--	--	#		VST[8:0]	0x00
0x019	#	#	#	#	#	#	#	#			0x00
0x01A	--	--	--	--	--	--	#	--	CCSET	TSFIX	0x00
0x01B	#	#	#	#	#	#	#	#	PWS	VCOM_W[3:0], SD_W[3:0]	0x00
0x01C	--	--	--	--	--	--	#	#	LVSEL	LVD_SEL[1:0]	0x03
0x01D	#	#	#	#	#	#	#	#	TSSET	TS_SET[7:0]	0x00

DEEP SLEEP MODE

After deep sleep command (R07H) is transmitted, UC8151 enter “Deep Sleep Mode”, and leaves by RST_N falling. In “Deep Sleep Mode”, the control signals are recommended tied to 0v to avoid IO leakage current. And the die must be keep away from light which causes photoelectric effect to make internal nodes unstable.



PANEL BREAK CHECK

The panel break check (PBC) function is accomplished by testing the connection of the ITO along panel edge. If the panel is broken, the loop ITO may be cut off. The connection check is judged by signal transmission from CHKGO to CHKGI.

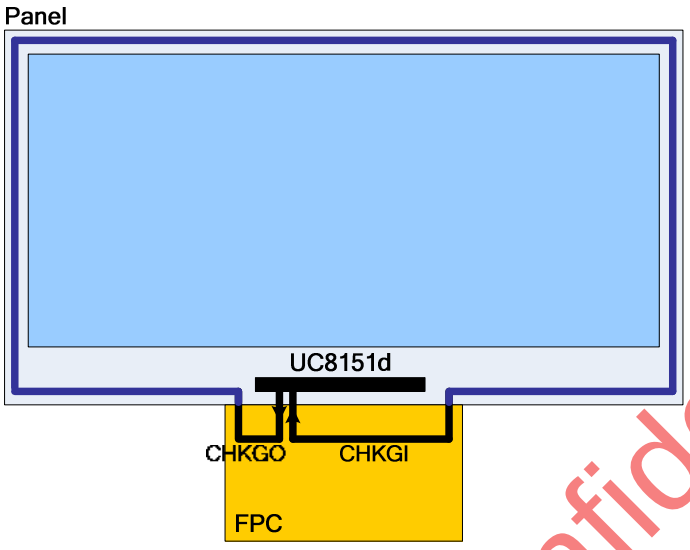


Figure: Panel break check layout example

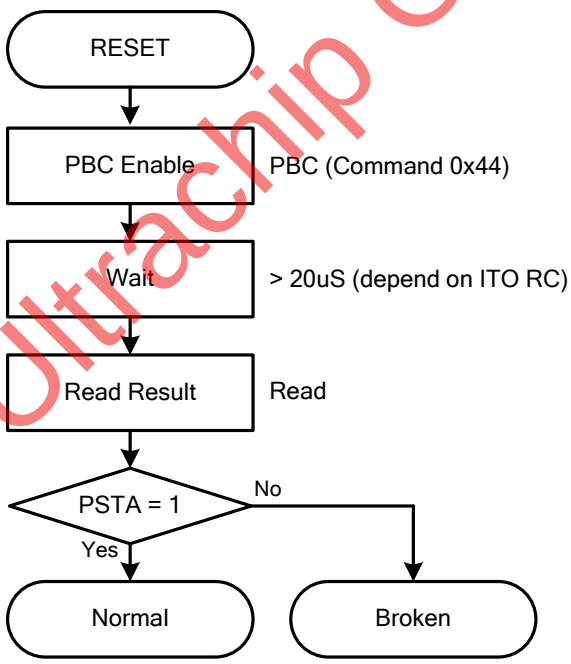
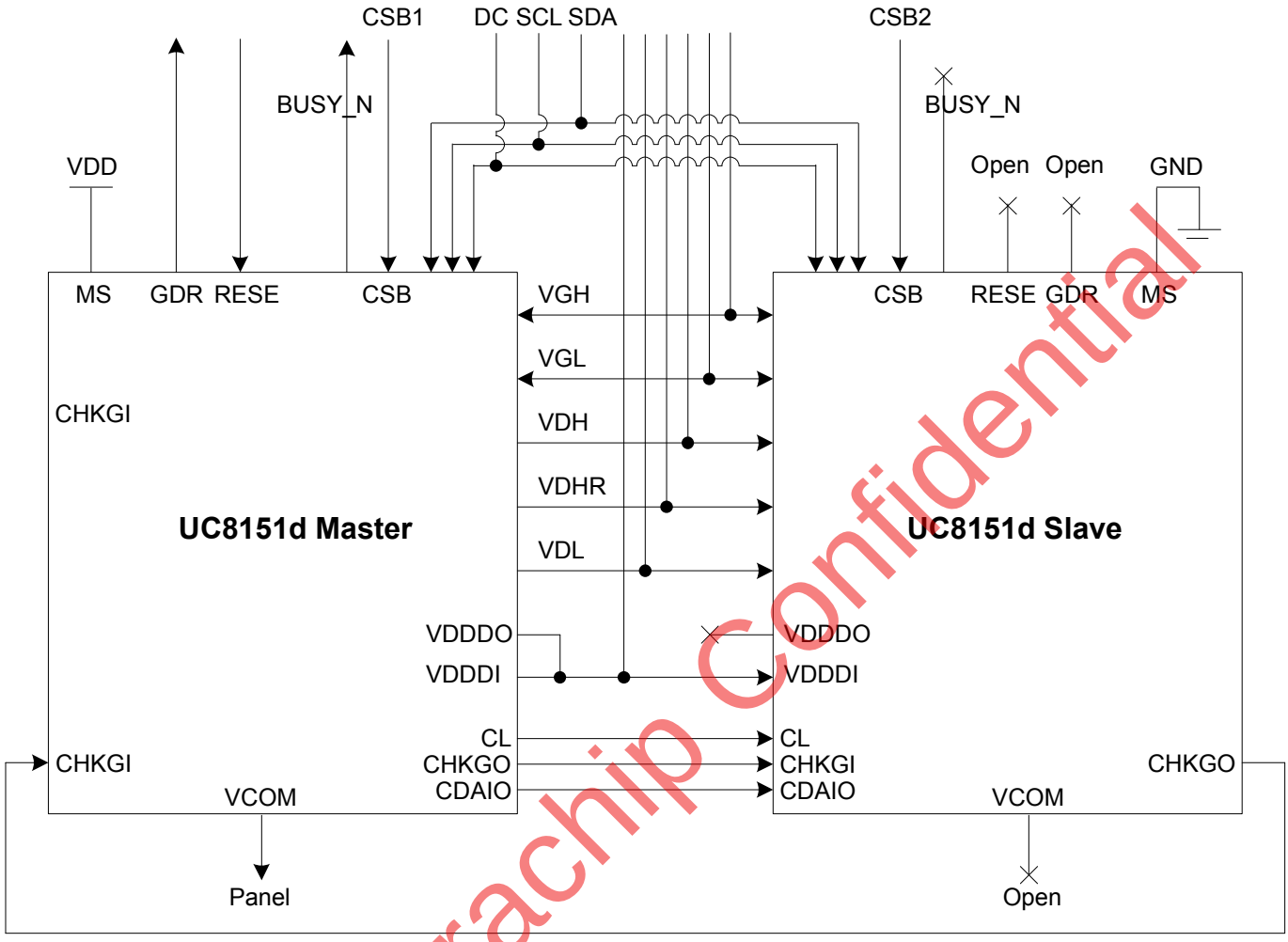


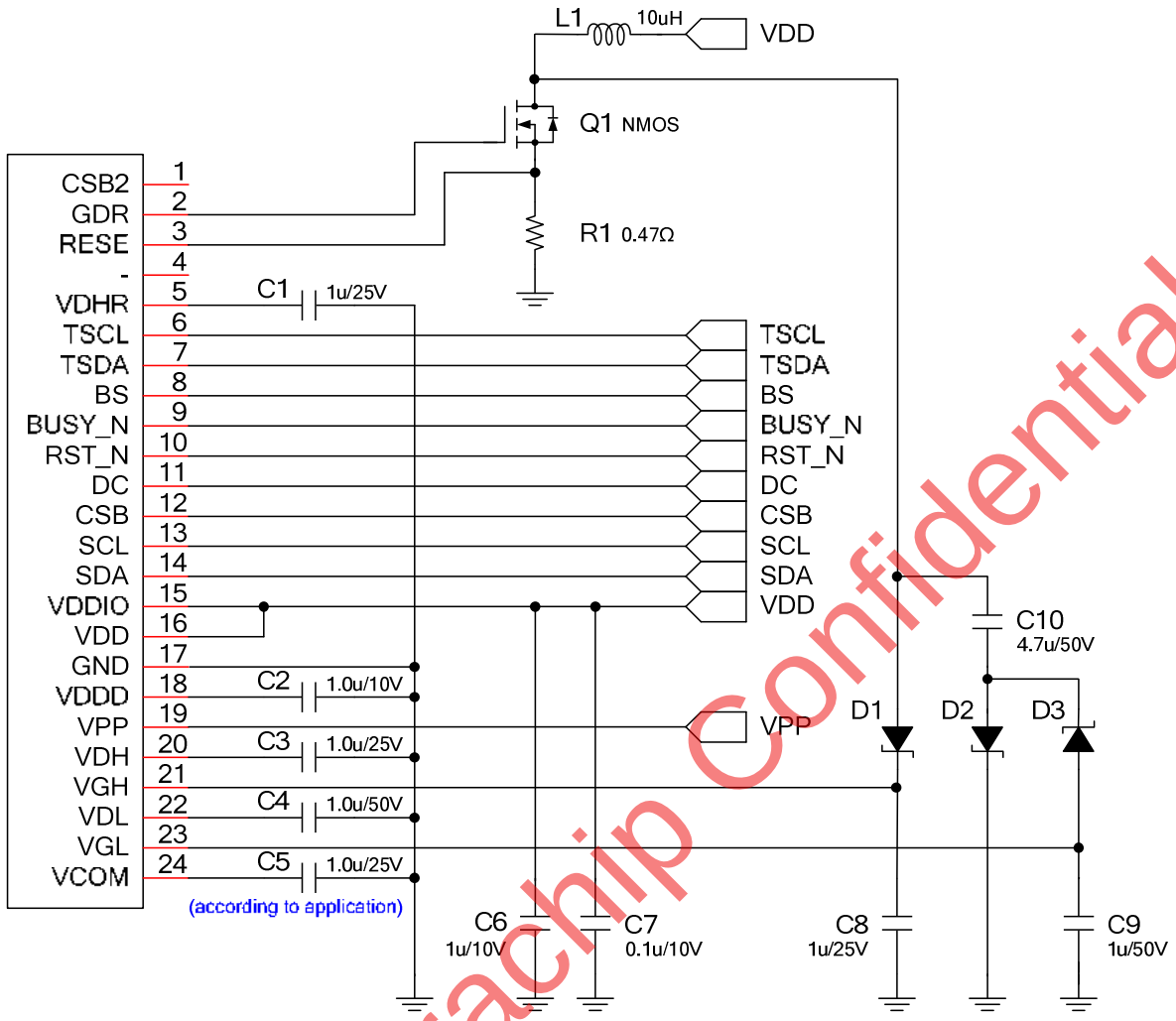
Figure: Panel Break Check (PBC) Sequence

CASCADE APPLICATION CIRCUIT



All commands sent to **Master** must be also sent to **Slave** except for data writing (DTM1 and DTM2). The display data must be separated to two parts, one is for **Master** and another is for **Slave**. They are transmitted to **Master** and **Slave** individually by using CSB1 and CSB2.

BOOSTER APPLICATION CIRCUIT



Recommended Device

1. Switch MOS NMOS: Vishay Si1308EDL (V_{DS} > 20V, I_D > 500mA, V_{GS}(th) < 1.5V, C_{iss} < 200pF, R_{DS}(on) < 400mΩ)
2. Schottky Diode: OnSemi MBR0530 (V_R > 20V, I_F > 500mA, I_R < 1mA @ V_R=15V, T_a=100°C)

Recommended Resister

Item	Pins	Resistance
Powers	VDD, VDDA, VDDIO, GND, GNDA, VDM	< 10 Ω
Boosters	VGL, VGH, GDR, RESE	< 10 Ω
Regulators	VDH, VDL, VDHR, VCOM, VDDD, VDDDO	< 10 Ω
Logics	MS, BS, CSB, SCL, SDA, GDR, etc.	< 50 Ω
OTP	VPP	< 20 Ω

ABSOLUTE MAXIMUM RATINGS

Signal	Item	Min	Max.	Unit
V_{DD}, V_{DDIO}, V_{DDA}	Logic Supply voltage	-0.3	+6.0	V
V_{PP}	OTP programming voltage	-0.3	+8.0	V
V_I	Digital input range	-0.3	V_{DDIO}+0.3	V
VGH-VGL	Supply range	-	+44.0	V
Source				
VDH	Analog supply voltage – positive	+16		V
VDL	Analog supply voltage -- negative	-16		V
VDHR	Analog supply voltage – positive	+16		V
Gate				
VGH	Analog supply voltage – positive	-0.3	+22	V
VGL	Analog supply voltage -- negative	-22	0.3	V
IVGH	Input rush current for VGH	(TBD)	(TBD)	mA
IVGL	Input rush current for VGL	(TBD)	(TBD)	mA
T_{STG}	Storage temperature range	-55	+125	^{o}C

Warning:

If ICs are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
VDDIO	IO supply voltage		2.3	3.3	3.6	V
VDD	Supply voltage		2.3	3.3	3.6	V
VDDA	DCDC driver supply voltage		2.3	3.3	3.6	V
VIL	LOW Level input voltage	Digital input pins	0	--	0.3xVDD	V
VIH	HIGH Level input voltage	Digital input pins	0.7xVDDIO	--	VDDIO	V
VOH	HIGH Level output voltage	Digital input pins, IOH=400uA	VDDIO-0.4	--	--	V
VOL	LOW Level Output voltage	Digital input pins, IOL=-400uA	0	--	0.4	V
IIN	Input leakage current	Digital input pins except pull-up, pull-down pin	-1	--	1	uA
RIN	Pull-up/down impedance			200		KΩ
Top	Operating temperature		-30		85	^{o}C
dVGH	VGH Supply voltage dev		-400	0	+400	mV
VGH-VGL	Voltage Range of VGH - VGL		--		40	V
dVDH	Supply voltage dev		-200	0	+200	mV
dVDL	Supply voltage dev		-200	0	+200	mV
dVDHR	Supply voltage dev		-200	0	+200	mV
dVCOM	Supply voltage dev		-200	0	+200	mV
RON	Driver Output Resistance	For source driver, TOP=25^{o}C, VOUT = ±15V		16.0	38.4	KΩ
		For gate driver, TOP=25^{o}C, VOUT = ±20V		4.0	8	

VDD=VDDA=VDDIO=3.0V, TOP=25.0 ^{o}C

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
IVDD	Digital deep sleep current	VDDD OFF	--	0.3	0.5	uA
	Digital stand-by current	All stopped	--	8.2	10.0	uA
	Digital operating current		--	--	0.1	mA
IVDDIO	IO deep sleep current	VDDD OFF	--	0.1	0.3	uA
	IO stand-by current	Booster OFF	--	2.5	4.0	uA
	IO operating current	No load	--	--	0.1	mA
IVDDA	DCDC deep sleep current	VDDD OFF	--	0.1	0.3	uA
	DCDC stand-by current	Booster OFF	--	15.5	20.0	uA
	DCDC operating current	Source output VDH/VDL, Duty=0.5, Period =126us VCOM DC No load	--	--	4.0	mA
		Source output VDH/VDL, Duty=0.5, Period =126us, VCOM DC External cap: 415pF, NMOS=340pF	--	--	20.0	

AC CHARACTERISTICS

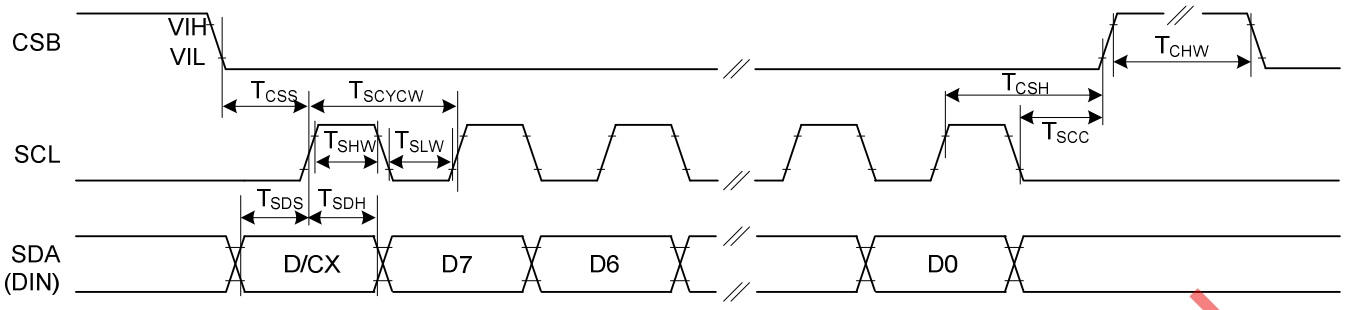


Figure: 3-wire Serial Interface Characteristics (Write mode)

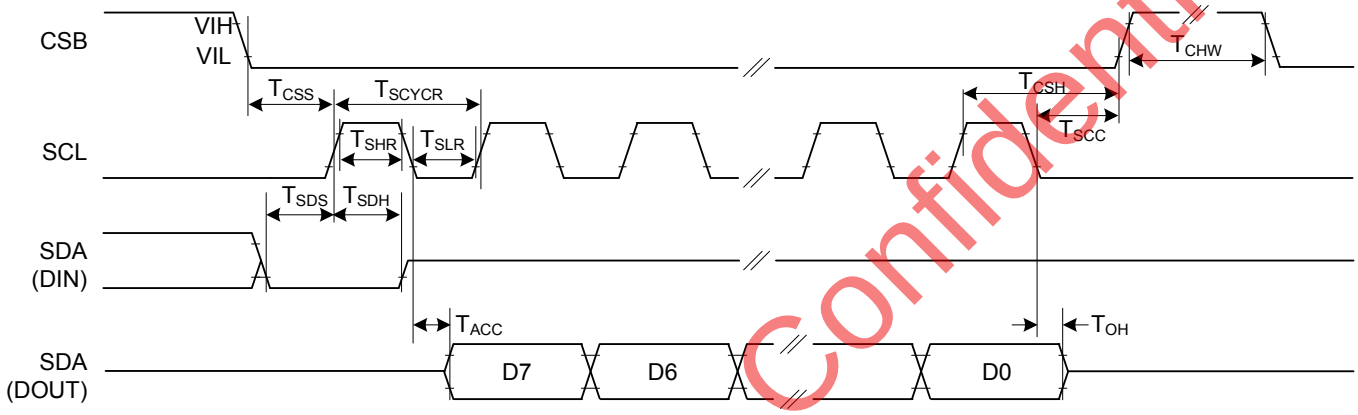


Figure: 3-wire Serial Interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL “H” pulse width (Write)	35			ns
T_{SLW}		SCL “L” pulse width (Write)	35			ns
T_{SCYCR}		Serial clock cycle (Read)	150			ns
T_{SHR}		SCL “H” pulse width (Read)	60			ns
T_{SLR}		SCL “L” pulse width (Read)	60			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			50	ns
T_{OH}		Output disable time	15			ns

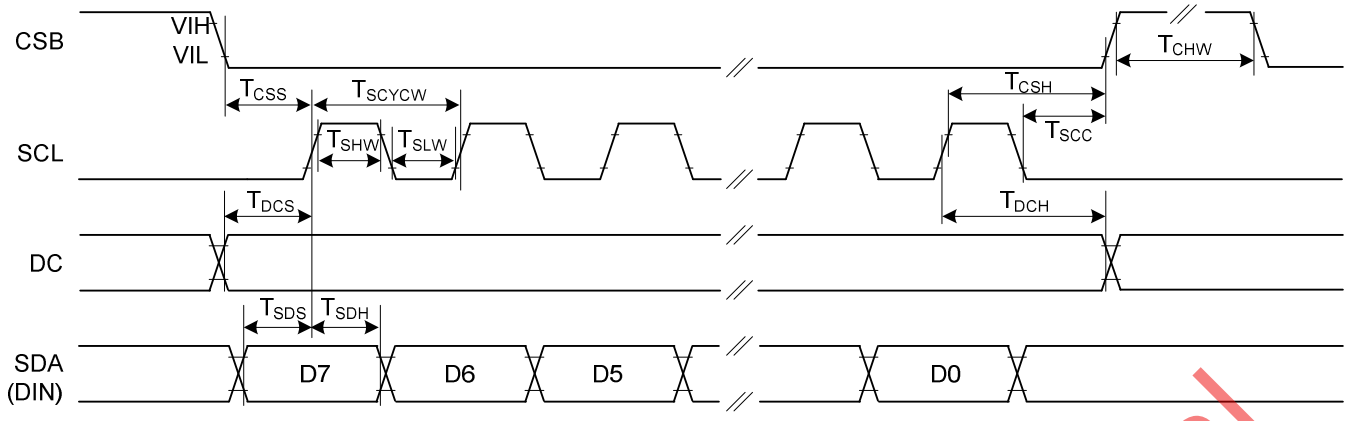


Figure: 4-wire Serial Interface Characteristics (Write mode)

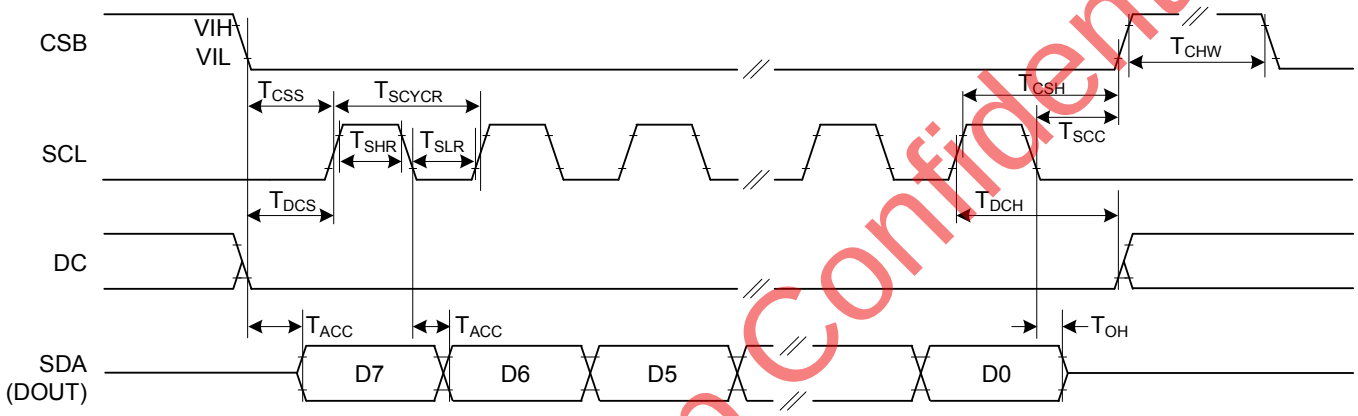
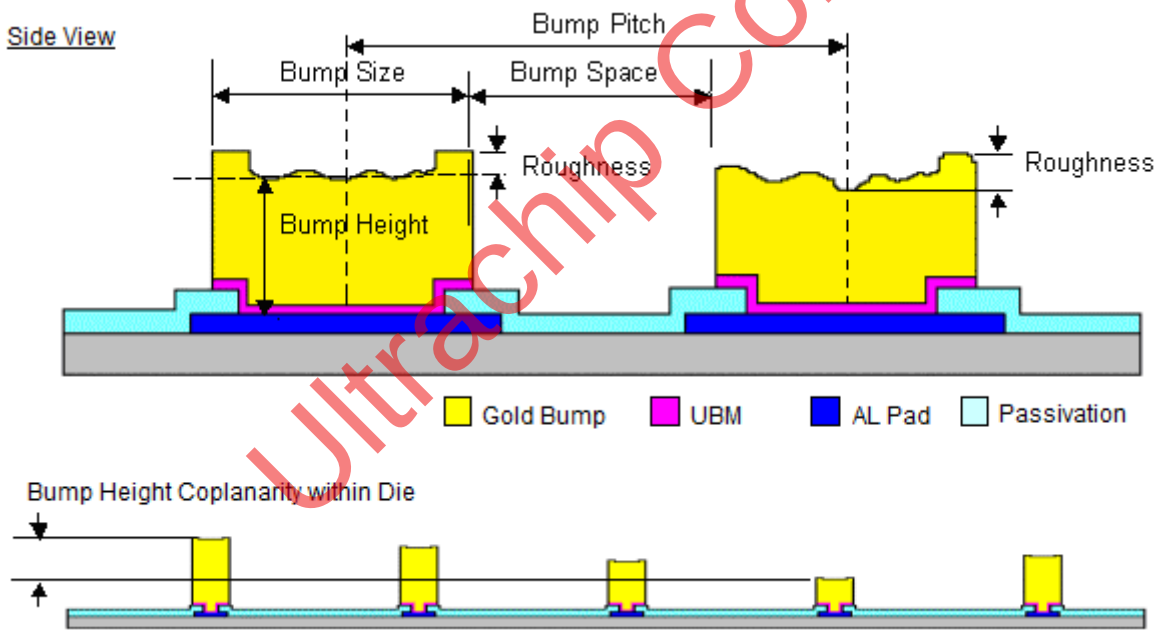


Figure: 4-wire Serial Interface Characteristics (Read mode)

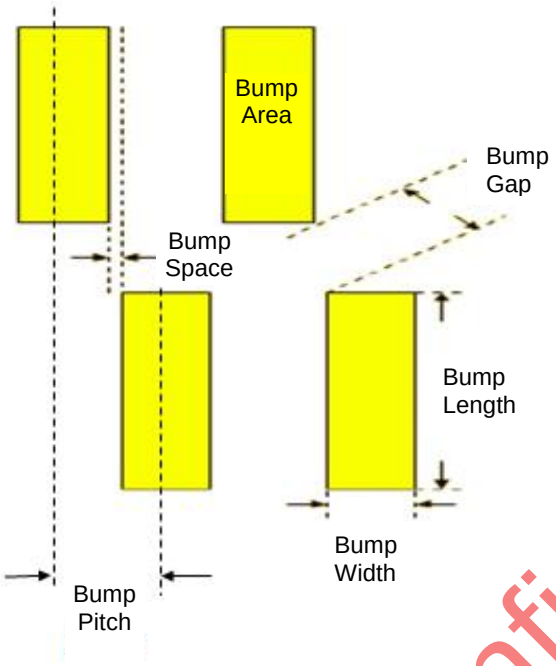
Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL “H” pulse width (Write)	35			ns
T_{SLW}		SCL “L” pulse width (Write)	35			ns
T_{SCYCR}		Serial clock cycle (Read)	150			ns
T_{SHR}		SCL “H” pulse width (Read)	60			ns
T_{SLR}		SCL “L” pulse width (Read)	60			ns
T_{DCS}	DC	DC setup time	30			ns
T_{DCH}		DC hold time	30			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			50	ns
T_{OH}		Output disable time	15			ns

PHYSICAL DIMENSIONS

Die Size:	(9530 μM ± 40μM) x (980 μM ± 40μM)
Die Thickness:	300 μM ± 20μM
	180 μM ± 15μM
Die TTV:	(D_{MAX} – D_{MIN}) within die ⩽ 2μM
Bump Height:	15 μM ± 3μM
	(H_{MAX} – H_{MIN}) within die ⩽ 2μM
Bump Size:	12 μM x 100 μM ± 2μM
Bump Area:	1200 μM^2
Bump Pitch:	13 μM ± 2μM
Bump Space:	1 μM ± 3μM
Hardness:	65 Hv ± 15Hv
Shear:	⩾ 5g/Mil^2
Coordinate origin:	Chip center
Pad reference:	Pad center

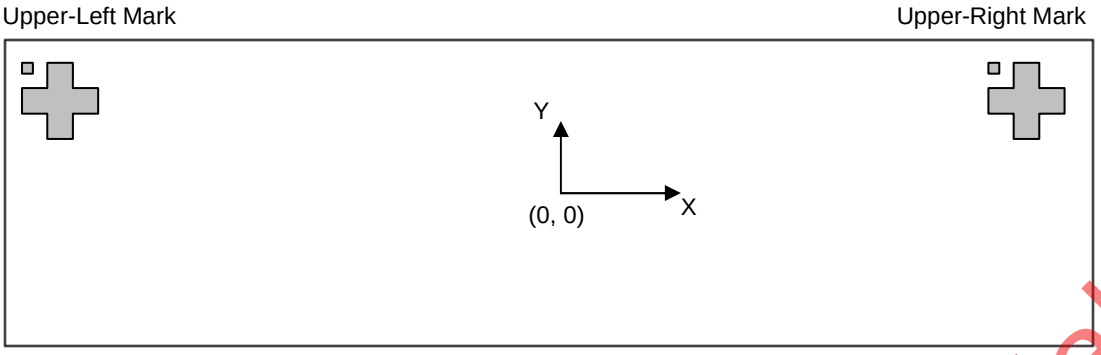


For Stagger Layout

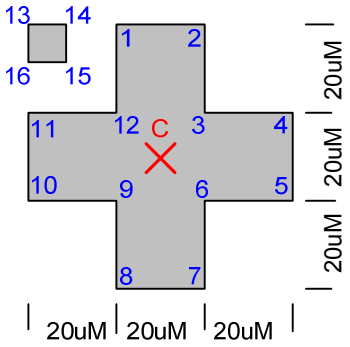


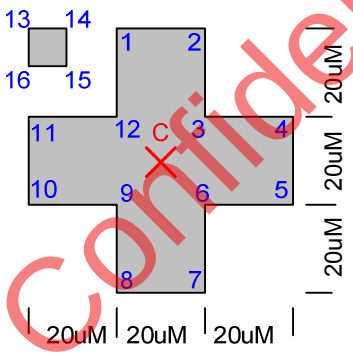
ALIGNMENT MARK INFORMATION

Location:



Shapes and Points:





Point Coordinates:

Point	Upper-Left Mark		Upper-Right Mark	
	X	Y	X	Y
Center	-4665	390	4665	390
1	-4675	420	4655	420
2	-4655	420	4675	420
3	-4655	400	4675	400
4	-4635	400	4695	400
5	-4635	380	4695	380
6	-4655	380	4675	380
7	-4655	360	4675	360
8	-4675	360	4655	360
9	-4675	380	4655	380
10	-4695	380	4635	380
11	-4695	400	4635	400
12	-4675	400	4655	400
13	-4695	420	4635	420
14	-4685	420	4645	420
15	-4685	410	4645	410
16	-4695	410	4635	410

PAD COORDINATES

No.	Pad	X	Y	W	H
1	NC	-4646	-398	28	70
2	VCOM	-4600	-398	28	70
3	VCOM	-4554	-398	28	70
4	VCOM	-4508	-398	28	70
5	VCOM	-4462	-398	28	70
6	VCOM	-4416	-398	28	70
7	VCOM	-4370	-398	28	70
8	VCOM	-4324	-398	28	70
9	VCOM	-4278	-398	28	70
10	VDM	-4232	-398	28	70
11	VGL	-4186	-398	28	70
12	VGL	-4140	-398	28	70
13	VGL	-4094	-398	28	70
14	VGL	-4048	-398	28	70
15	VGL	-4002	-398	28	70
16	VGL	-3956	-398	28	70
17	VGL	-3910	-398	28	70
18	VGL	-3864	-398	28	70
19	VGL	-3818	-398	28	70
20	VGL	-3772	-398	28	70
21	VGL	-3726	-398	28	70
22	VGL	-3680	-398	28	70
23	VGL	-3634	-398	28	70
24	VGL	-3588	-398	28	70
25	VGL	-3542	-398	28	70
26	VGL	-3496	-398	28	70
27	GNDA	-3450	-398	28	70
28	VSL	-3404	-398	28	70
29	VSL	-3358	-398	28	70
30	VSL	-3312	-398	28	70
31	VSL	-3266	-398	28	70
32	VSL	-3220	-398	28	70
33	VSL	-3174	-398	28	70
34	VSL	-3128	-398	28	70
35	VSL	-3082	-398	28	70
36	VSL	-3036	-398	28	70
37	VSL	-2990	-398	28	70
38	GNDA	-2944	-398	28	70
39	VGH	-2898	-398	28	70
40	VGH	-2852	-398	28	70
41	VGH	-2806	-398	28	70
42	VGH	-2760	-398	28	70
43	VGH	-2714	-398	28	70
44	VGH	-2668	-398	28	70
45	VGH	-2622	-398	28	70
46	VGH	-2576	-398	28	70
47	VGH	-2530	-398	28	70
48	VGH	-2484	-398	28	70
49	VGH	-2438	-398	28	70
50	VGH	-2392	-398	28	70
51	GNDA	-2346	-398	28	70
52	VSH	-2300	-398	28	70
53	VSH	-2254	-398	28	70
54	VSH	-2208	-398	28	70
55	VSH	-2162	-398	28	70
56	VSH	-2116	-398	28	70
57	VSH	-2070	-398	28	70
58	VSH	-2024	-398	28	70
59	VSH	-1978	-398	28	70
60	VSH	-1932	-398	28	70
61	VSH	-1886	-398	28	70
62	GNDA	-1840	-398	28	70
63	VPP	-1794	-398	28	70
64	VPP	-1748	-398	28	70
65	VPP	-1702	-398	28	70
66	VPP	-1656	-398	28	70
67	VPP	-1610	-398	28	70
68	VPP	-1564	-398	28	70
69	VDDDI	-1518	-398	28	70
70	VDDDI	-1472	-398	28	70
71	VDDDI	-1426	-398	28	70
72	VDDDI	-1380	-398	28	70
73	VDDDO	-1334	-398	28	70
74	VDDDO	-1288	-398	28	70
75	VDDDO	-1242	-398	28	70
76	VDDDO	-1196	-398	28	70
77	VDM	-1150	-398	28	70
78	VDM	-1104	-398	28	70
79	GNDA	-1058	-398	28	70
80	GNDA	-1012	-398	28	70
81	GNDA	-966	-398	28	70
82	GNDA	-920	-398	28	70
83	GNDA	-874	-398	28	70
84	GNDA	-828	-398	28	70
85	GNDA	-782	-398	28	70
86	GNDA	-736	-398	28	70
87	GNDA	-690	-398	28	70
88	GNDA	-644	-398	28	70
89	GND	-598	-398	28	70
90	GND	-552	-398	28	70
91	GND	-506	-398	28	70
92	GND	-460	-398	28	70
93	GND	-414	-398	28	70
94	GND	-368	-398	28	70
95	GND	-322	-398	28	70
96	GND	-276	-398	28	70
97	GND	-230	-398	28	70
98	GND	-184	-398	28	70
99	GND	-138	-398	28	70
100	GND	-92	-398	28	70
101	VDDA	-46	-398	28	70
102	VDDA	0	-398	28	70
103	VDDA	46	-398	28	70
104	VDDA	92	-398	28	70
105	VDDA	138	-398	28	70
106	VDDA	184	-398	28	70
107	VDDA	230	-398	28	70
108	VDDA	276	-398	28	70
109	VDDA	322	-398	28	70
110	VDDA	368	-398	28	70
111	VDD	414	-398	28	70
112	VDD	460	-398	28	70
113	VDD	506	-398	28	70
114	VDD	552	-398	28	70

No.	Pad	X	Y	W	H
115	VDD	598	-398	28	70
116	VDD	644	-398	28	70
117	VDD	690	-398	28	70
118	TEST1	736	-398	28	70
119	TEST2	782	-398	28	70
120	VDDIO	828	-398	28	70
121	VDDIO	874	-398	28	70
122	VDDIO	920	-398	28	70
123	VDDIO	966	-398	28	70
124	TEST3	1012	-398	28	70
125	DUMMY	1058	-398	28	70
126	DUMMY	1104	-398	28	70
127	DUMMY	1150	-398	28	70
128	DUMMY	1196	-398	28	70
129	DUMMY	1242	-398	28	70
130	SDA	1288	-398	28	70
131	SCL	1334	-398	28	70
132	GND	1380	-398	28	70
133	CSB	1426	-398	28	70
134	VDDIO	1472	-398	28	70
135	DUMMY	1518	-398	28	70
136	GND	1564	-398	28	70
137	DC	1610	-398	28	70
138	VDDIO	1656	-398	28	70
139	DUMMY	1702	-398	28	70
140	GND	1748	-398	28	70
141	RST_N	1794	-398	28	70
142	BUSY_N	1840	-398	28	70
143	CL	1886	-398	28	70
144	VDDIO	1932	-398	28	70
145	VSYNC	1978	-398	28	70
146	GND	2024	-398	28	70
147	DUMMY	2070	-398	28	70
148	VDDIO	2116	-398	28	70
149	BS	2162	-398	28	70
150	GND	2208	-398	28	70
151	DUMMY	2254	-398	28	70
152	VDDIO	2300	-398	28	70
153	CHKGI	2346	-398	28	70
154	GND	2392	-398	28	70
155	MS	2438	-398	28	70
156	VDDIO	2484	-398	28	70
157	TSDA	2530	-398	28	70
158	TSDA	2576	-398	28	70
159	TSCL	2622	-398	28	70
160	TSCL	2668	-398	28	70
161	CHKGO	2714	-398	28	70
162	CDAIO	2760	-398	28	70
163	TEST6	2806	-398	28	70
164	TEST7	2852	-398	28	70
165	VDHR	2898	-398	28	70
166	VDHR	2944	-398	28	70
167	VDHR	2990	-398	28	70
168	VDHR	3036	-398	28	70
169	VDHR	3082	-398	28	70
170	VDHR	3128	-398	28	70
171	VDHR	3174	-398	28	70
172	VDHR	3220	-398	28	70
173	DUMMY	3266	-398	28	70

No.	Pad	X	Y	W	H
174	DUMMY	3312	-398	28	70
175	DUMMY	3358	-398	28	70
176	DUMMY	3404	-398	28	70
177	DUMMY	3450	-398	28	70
178	DUMMY	3496	-398	28	70
179	GNDA	3542	-398	28	70
180	FB	3588	-398	28	70
181	FB	3634	-398	28	70
182	GNDA	3680	-398	28	70
183	RESE	3726	-398	28	70
184	RESE	3772	-398	28	70
185	GNDA	3818	-398	28	70
186	GDR	3864	-398	28	70
187	GDR	3910	-398	28	70
188	GDR	3956	-398	28	70
189	GDR	4002	-398	28	70
190	GDR	4048	-398	28	70
191	GDR	4094	-398	28	70
192	GDR	4140	-398	28	70
193	GDR	4186	-398	28	70
194	VDM	4232	-398	28	70
195	VCOM	4278	-398	28	70
196	VCOM	4324	-398	28	70
197	VCOM	4370	-398	28	70
198	VCOM	4416	-398	28	70
199	VCOM	4462	-398	28	70
200	VCOM	4508	-398	28	70
201	VCOM	4554	-398	28	70
202	VCOM	4600	-398	28	70
203	NC	4646	-398	28	70
204	NC	4540	313.5	18	75
205	NC	4519	413.5	18	75
206	NC	4498	313.5	18	75
207	NC	4477	413.5	18	75
208	NC	4456	313.5	18	75
209	NC	4435	413.5	18	75
210	G<0>	4414	313.5	18	75
211	G<2>	4393	413.5	18	75
212	G<4>	4372	313.5	18	75
213	G<6>	4351	413.5	18	75
214	G<8>	4330	313.5	18	75
215	G<10>	4309	413.5	18	75
216	G<12>	4288	313.5	18	75
217	G<14>	4267	413.5	18	75
218	G<16>	4246	313.5	18	75
219	G<18>	4225	413.5	18	75
220	G<20>	4204	313.5	18	75
221	G<22>	4183	413.5	18	75
222	G<24>	4162	313.5	18	75
223	G<26>	4141	413.5	18	75
224	G<28>	4120	313.5	18	75
225	G<30>	4099	413.5	18	75
226	G<32>	4078	313.5	18	75
227	G<34>	4057	413.5	18	75
228	G<36>	4036	313.5	18	75
229	G<38>	4015	413.5	18	75
230	G<40>	3994	313.5	18	75
231	G<42>	3973	413.5	18	75
232	G<44>	3952	313.5	18	75

No.	Pad	X	Y	W	H
233	G<46>	3931	413.5	18	75
234	G<48>	3910	313.5	18	75
235	G<50>	3889	413.5	18	75
236	G<52>	3868	313.5	18	75
237	G<54>	3847	413.5	18	75
238	G<56>	3826	313.5	18	75
239	G<58>	3805	413.5	18	75
240	G<60>	3784	313.5	18	75
241	G<62>	3763	413.5	18	75
242	G<64>	3742	313.5	18	75
243	G<66>	3721	413.5	18	75
244	G<68>	3700	313.5	18	75
245	G<70>	3679	413.5	18	75
246	G<72>	3658	313.5	18	75
247	G<74>	3637	413.5	18	75
248	G<76>	3616	313.5	18	75
249	G<78>	3595	413.5	18	75
250	G<80>	3574	313.5	18	75
251	G<82>	3553	413.5	18	75
252	G<84>	3532	313.5	18	75
253	G<86>	3511	413.5	18	75
254	G<88>	3490	313.5	18	75
255	G<90>	3469	413.5	18	75
256	G<92>	3448	313.5	18	75
257	G<94>	3427	413.5	18	75
258	G<96>	3406	313.5	18	75
259	G<98>	3385	413.5	18	75
260	G<100>	3364	313.5	18	75
261	G<102>	3343	413.5	18	75
262	G<104>	3322	313.5	18	75
263	G<106>	3301	413.5	18	75
264	G<108>	3280	313.5	18	75
265	G<110>	3259	413.5	18	75
266	G<112>	3238	313.5	18	75
267	G<114>	3217	413.5	18	75
268	G<116>	3196	313.5	18	75
269	G<118>	3175	413.5	18	75
270	G<120>	3154	313.5	18	75
271	G<122>	3133	413.5	18	75
272	G<124>	3112	313.5	18	75
273	G<126>	3091	413.5	18	75
274	G<128>	3070	313.5	18	75
275	G<130>	3049	413.5	18	75
276	G<132>	3028	313.5	18	75
277	G<134>	3007	413.5	18	75
278	G<136>	2986	313.5	18	75
279	G<138>	2965	413.5	18	75
280	G<140>	2944	313.5	18	75
281	G<142>	2923	413.5	18	75
282	G<144>	2902	313.5	18	75
283	G<146>	2881	413.5	18	75
284	G<148>	2860	313.5	18	75
285	G<150>	2839	413.5	18	75
286	G<152>	2818	313.5	18	75
287	G<154>	2797	413.5	18	75
288	G<156>	2776	313.5	18	75
289	G<158>	2755	413.5	18	75
290	G<160>	2734	313.5	18	75
291	G<162>	2713	413.5	18	75

No.	Pad	X	Y	W	H
292	G<164>	2692	313.5	18	75
293	G<166>	2671	413.5	18	75
294	G<168>	2650	313.5	18	75
295	G<170>	2629	413.5	18	75
296	G<172>	2608	313.5	18	75
297	G<174>	2587	413.5	18	75
298	G<176>	2566	313.5	18	75
299	G<178>	2545	413.5	18	75
300	G<180>	2524	313.5	18	75
301	G<182>	2503	413.5	18	75
302	G<184>	2482	313.5	18	75
303	G<186>	2461	413.5	18	75
304	G<188>	2440	313.5	18	75
305	G<190>	2419	413.5	18	75
306	G<192>	2398	313.5	18	75
307	G<194>	2377	413.5	18	75
308	G<196>	2356	313.5	18	75
309	G<198>	2335	413.5	18	75
310	G<200>	2314	313.5	18	75
311	G<202>	2293	413.5	18	75
312	G<204>	2272	313.5	18	75
313	G<206>	2251	413.5	18	75
314	G<208>	2230	313.5	18	75
315	G<210>	2209	413.5	18	75
316	G<212>	2188	313.5	18	75
317	G<214>	2167	413.5	18	75
318	G<216>	2146	313.5	18	75
319	G<218>	2125	413.5	18	75
320	G<220>	2104	313.5	18	75
321	G<222>	2083	413.5	18	75
322	G<224>	2062	313.5	18	75
323	G<226>	2041	413.5	18	75
324	G<228>	2020	313.5	18	75
325	G<230>	1999	413.5	18	75
326	G<232>	1978	313.5	18	75
327	G<234>	1957	413.5	18	75
328	G<236>	1936	313.5	18	75
329	G<238>	1915	413.5	18	75
330	G<240>	1894	313.5	18	75
331	G<242>	1873	413.5	18	75
332	G<244>	1852	313.5	18	75
333	G<246>	1831	413.5	18	75
334	G<248>	1810	313.5	18	75
335	G<250>	1789	413.5	18	75
336	G<252>	1768	313.5	18	75
337	G<254>	1747	413.5	18	75
338	G<256>	1726	313.5	18	75
339	G<258>	1705	413.5	18	75
340	G<260>	1684	313.5	18	75
341	G<262>	1663	413.5	18	75
342	G<264>	1642	313.5	18	75
343	G<266>	1621	413.5	18	75
344	G<268>	1600	313.5	18	75
345	G<270>	1579	413.5	18	75
346	G<272>	1558	313.5	18	75
347	G<274>	1537	413.5	18	75
348	G<276>	1516	313.5	18	75
349	G<278>	1495	413.5	18	75
350	G<280>	1474	313.5	18	75

No.	Pad	X	Y	W	H
351	G<282>	1453	413.5	18	75
352	G<284>	1432	313.5	18	75
353	G<286>	1411	413.5	18	75
354	G<288>	1390	313.5	18	75
355	G<290>	1369	413.5	18	75
356	G<292>	1348	313.5	18	75
357	G<294>	1327	413.5	18	75
358	NC	1306	313.5	18	75
359	NC	1285	413.5	18	75
360	NC	1264	313.5	18	75
361	NC	1243	413.5	18	75
362	NC	1222	313.5	18	75
363	NC	1201	413.5	18	75
364	NC	1180	313.5	18	75
365	NC	1072.5	420	12	100
366	NC	1059.5	301	12	100
367	VBD<1>	1046.5	420	12	100
368	S<0>	1033.5	301	12	100
369	S<1>	1020.5	420	12	100
370	S<2>	1007.5	301	12	100
371	S<3>	994.5	420	12	100
372	S<4>	981.5	301	12	100
373	S<5>	968.5	420	12	100
374	S<6>	955.5	301	12	100
375	S<7>	942.5	420	12	100
376	S<8>	929.5	301	12	100
377	S<9>	916.5	420	12	100
378	S<10>	903.5	301	12	100
379	S<11>	890.5	420	12	100
380	S<12>	877.5	301	12	100
381	S<13>	864.5	420	12	100
382	S<14>	851.5	301	12	100
383	S<15>	838.5	420	12	100
384	S<16>	825.5	301	12	100
385	S<17>	812.5	420	12	100
386	S<18>	799.5	301	12	100
387	S<19>	786.5	420	12	100
388	S<20>	773.5	301	12	100
389	S<21>	760.5	420	12	100
390	S<22>	747.5	301	12	100
391	S<23>	734.5	420	12	100
392	S<24>	721.5	301	12	100
393	S<25>	708.5	420	12	100
394	S<26>	695.5	301	12	100
395	S<27>	682.5	420	12	100
396	S<28>	669.5	301	12	100
397	S<29>	656.5	420	12	100
398	S<30>	643.5	301	12	100
399	S<31>	630.5	420	12	100
400	S<32>	617.5	301	12	100
401	S<33>	604.5	420	12	100
402	S<34>	591.5	301	12	100
403	S<35>	578.5	420	12	100
404	S<36>	565.5	301	12	100
405	S<37>	552.5	420	12	100
406	S<38>	539.5	301	12	100
407	S<39>	526.5	420	12	100
408	S<40>	513.5	301	12	100
409	S<41>	500.5	420	12	100

No.	Pad	X	Y	W	H
410	S<42>	487.5	301	12	100
411	S<43>	474.5	420	12	100
412	S<44>	461.5	301	12	100
413	S<45>	448.5	420	12	100
414	S<46>	435.5	301	12	100
415	S<47>	422.5	420	12	100
416	S<48>	409.5	301	12	100
417	S<49>	396.5	420	12	100
418	S<50>	383.5	301	12	100
419	S<51>	370.5	420	12	100
420	S<52>	357.5	301	12	100
421	S<53>	344.5	420	12	100
422	S<54>	331.5	301	12	100
423	S<55>	318.5	420	12	100
424	S<56>	305.5	301	12	100
425	S<57>	292.5	420	12	100
426	S<58>	279.5	301	12	100
427	S<59>	266.5	420	12	100
428	S<60>	253.5	301	12	100
429	S<61>	240.5	420	12	100
430	S<62>	227.5	301	12	100
431	S<63>	214.5	420	12	100
432	S<64>	201.5	301	12	100
433	S<65>	188.5	420	12	100
434	S<66>	175.5	301	12	100
435	S<67>	162.5	420	12	100
436	S<68>	149.5	301	12	100
437	S<69>	136.5	420	12	100
438	S<70>	123.5	301	12	100
439	S<71>	110.5	420	12	100
440	S<72>	97.5	301	12	100
441	S<73>	84.5	420	12	100
442	S<74>	71.5	301	12	100
443	S<75>	58.5	420	12	100
444	S<76>	45.5	301	12	100
445	S<77>	32.5	420	12	100
446	S<78>	19.5	301	12	100
447	S<79>	6.5	420	12	100
448	S<80>	-6.5	301	12	100
449	S<81>	-19.5	420	12	100
450	S<82>	-32.5	301	12	100
451	S<83>	-45.5	420	12	100
452	S<84>	-58.5	301	12	100
453	S<85>	-71.5	420	12	100
454	S<86>	-84.5	301	12	100
455	S<87>	-97.5	420	12	100
456	S<88>	-110.5	301	12	100
457	S<89>	-123.5	420	12	100
458	S<90>	-136.5	301	12	100
459	S<91>	-149.5	420	12	100
460	S<92>	-162.5	301	12	100
461	S<93>	-175.5	420	12	100
462	S<94>	-188.5	301	12	100
463	S<95>	-201.5	420	12	100
464	S<96>	-214.5	301	12	100
465	S<97>	-227.5	420	12	100
466	S<98>	-240.5	301	12	100
467	S<99>	-253.5	420	12	100
468	S<100>	-266.5	301	12	100

No.	Pad	X	Y	W	H
469	S<101>	-279.5	420	12	100
470	S<102>	-292.5	301	12	100
471	S<103>	-305.5	420	12	100
472	S<104>	-318.5	301	12	100
473	S<105>	-331.5	420	12	100
474	S<106>	-344.5	301	12	100
475	S<107>	-357.5	420	12	100
476	S<108>	-370.5	301	12	100
477	S<109>	-383.5	420	12	100
478	S<110>	-396.5	301	12	100
479	S<111>	-409.5	420	12	100
480	S<112>	-422.5	301	12	100
481	S<113>	-435.5	420	12	100
482	S<114>	-448.5	301	12	100
483	S<115>	-461.5	420	12	100
484	S<116>	-474.5	301	12	100
485	S<117>	-487.5	420	12	100
486	S<118>	-500.5	301	12	100
487	S<119>	-513.5	420	12	100
488	S<120>	-526.5	301	12	100
489	S<121>	-539.5	420	12	100
490	S<122>	-552.5	301	12	100
491	S<123>	-565.5	420	12	100
492	S<124>	-578.5	301	12	100
493	S<125>	-591.5	420	12	100
494	S<126>	-604.5	301	12	100
495	S<127>	-617.5	420	12	100
496	S<128>	-630.5	301	12	100
497	S<129>	-643.5	420	12	100
498	S<130>	-656.5	301	12	100
499	S<131>	-669.5	420	12	100
500	S<132>	-682.5	301	12	100
501	S<133>	-695.5	420	12	100
502	S<134>	-708.5	301	12	100
503	S<135>	-721.5	420	12	100
504	S<136>	-734.5	301	12	100
505	S<137>	-747.5	420	12	100
506	S<138>	-760.5	301	12	100
507	S<139>	-773.5	420	12	100
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511	S<143>	-825.5	420	12	100
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521	S<153>	-955.5	420	12	100
522	S<154>	-968.5	301	12	100
523	S<155>	-981.5	420	12	100
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525	S<157>	-1007.5	420	12	100
526	S<158>	-1020.5	301	12	100
527	S<159>	-1033.5	420	12	100

No.	Pad	X	Y	W	H
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530	NC	-1072.5	301	12	100
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532	NC	-1201	313.5	18	75
533	NC	-1222	413.5	18	75
534	NC	-1243	313.5	18	75
535	NC	-1264	413.5	18	75
536	NC	-1285	313.5	18	75
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543	G<285>	-1432	413.5	18	75
544	G<283>	-1453	313.5	18	75
545	G<281>	-1474	413.5	18	75
546	G<279>	-1495	313.5	18	75
547	G<277>	-1516	413.5	18	75
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549	G<273>	-1558	413.5	18	75
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552	G<267>	-1621	313.5	18	75
553	G<265>	-1642	413.5	18	75
554	G<263>	-1663	313.5	18	75
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559	G<253>	-1768	413.5	18	75
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565	G<241>	-1894	413.5	18	75
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571	G<229>	-2020	413.5	18	75
572	G<227>	-2041	313.5	18	75
573	G<225>	-2062	413.5	18	75
574	G<223>	-2083	313.5	18	75
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576	G<219>	-2125	313.5	18	75
577	G<217>	-2146	413.5	18	75
578	G<215>	-2167	313.5	18	75
579	G<213>	-2188	413.5	18	75
580	G<211>	-2209	313.5	18	75
581	G<209>	-2230	413.5	18	75
582	G<207>	-2251	313.5	18	75
583	G<205>	-2272	413.5	18	75
584	G<203>	-2293	313.5	18	75
585	G<201>	-2314	413.5	18	75
586	G<199>	-2335	313.5	18	75

No.	Pad	X	Y	W	H
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589	G<193>	-2398	413.5	18	75
590	G<191>	-2419	313.5	18	75
591	G<189>	-2440	413.5	18	75
592	G<187>	-2461	313.5	18	75
593	G<185>	-2482	413.5	18	75
594	G<183>	-2503	313.5	18	75
595	G<181>	-2524	413.5	18	75
596	G<179>	-2545	313.5	18	75
597	G<177>	-2566	413.5	18	75
598	G<175>	-2587	313.5	18	75
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600	G<171>	-2629	313.5	18	75
601	G<169>	-2650	413.5	18	75
602	G<167>	-2671	313.5	18	75
603	G<165>	-2692	413.5	18	75
604	G<163>	-2713	313.5	18	75
605	G<161>	-2734	413.5	18	75
606	G<159>	-2755	313.5	18	75
607	G<157>	-2776	413.5	18	75
608	G<155>	-2797	313.5	18	75
609	G<153>	-2818	413.5	18	75
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611	G<149>	-2860	413.5	18	75
612	G<147>	-2881	313.5	18	75
613	G<145>	-2902	413.5	18	75
614	G<143>	-2923	313.5	18	75
615	G<141>	-2944	413.5	18	75
616	G<139>	-2965	313.5	18	75
617	G<137>	-2986	413.5	18	75
618	G<135>	-3007	313.5	18	75
619	G<133>	-3028	413.5	18	75
620	G<131>	-3049	313.5	18	75
621	G<129>	-3070	413.5	18	75
622	G<127>	-3091	313.5	18	75
623	G<125>	-3112	413.5	18	75
624	G<123>	-3133	313.5	18	75
625	G<121>	-3154	413.5	18	75
626	G<119>	-3175	313.5	18	75
627	G<117>	-3196	413.5	18	75
628	G<115>	-3217	313.5	18	75
629	G<113>	-3238	413.5	18	75
630	G<111>	-3259	313.5	18	75
631	G<109>	-3280	413.5	18	75
632	G<107>	-3301	313.5	18	75
633	G<105>	-3322	413.5	18	75
634	G<103>	-3343	313.5	18	75
635	G<101>	-3364	413.5	18	75
636	G<99>	-3385	313.5	18	75
637	G<97>	-3406	413.5	18	75
638	G<95>	-3427	313.5	18	75
639	G<93>	-3448	413.5	18	75
640	G<91>	-3469	313.5	18	75
641	G<89>	-3490	413.5	18	75
642	G<87>	-3511	313.5	18	75
643	G<85>	-3532	413.5	18	75
644	G<83>	-3553	313.5	18	75
645	G<81>	-3574	413.5	18	75

No.	Pad	X	Y	W	H
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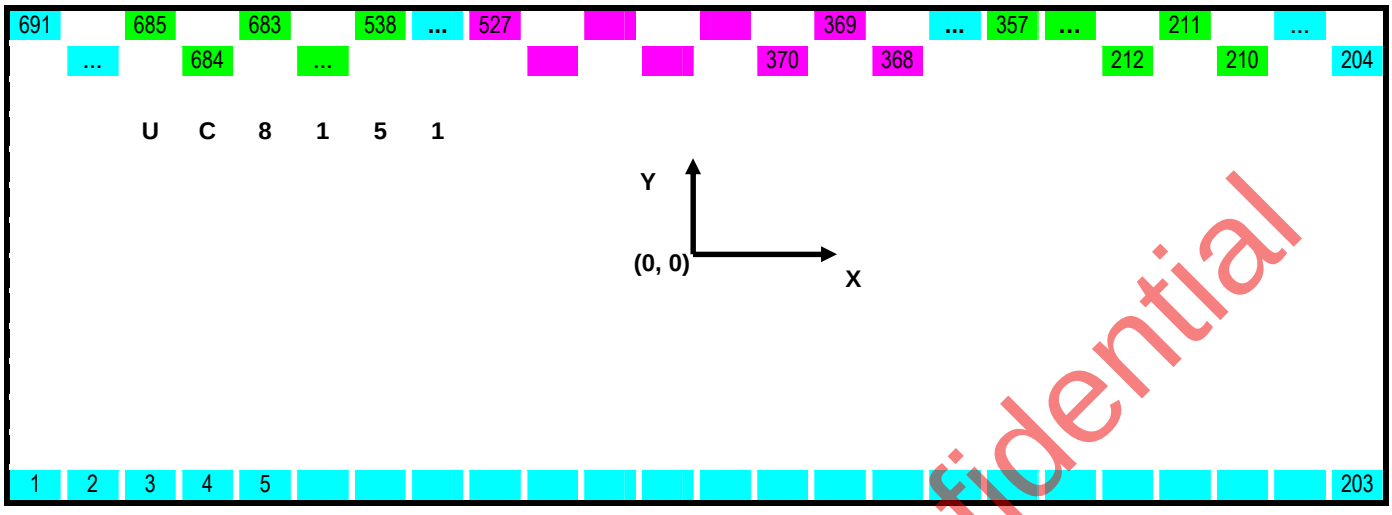
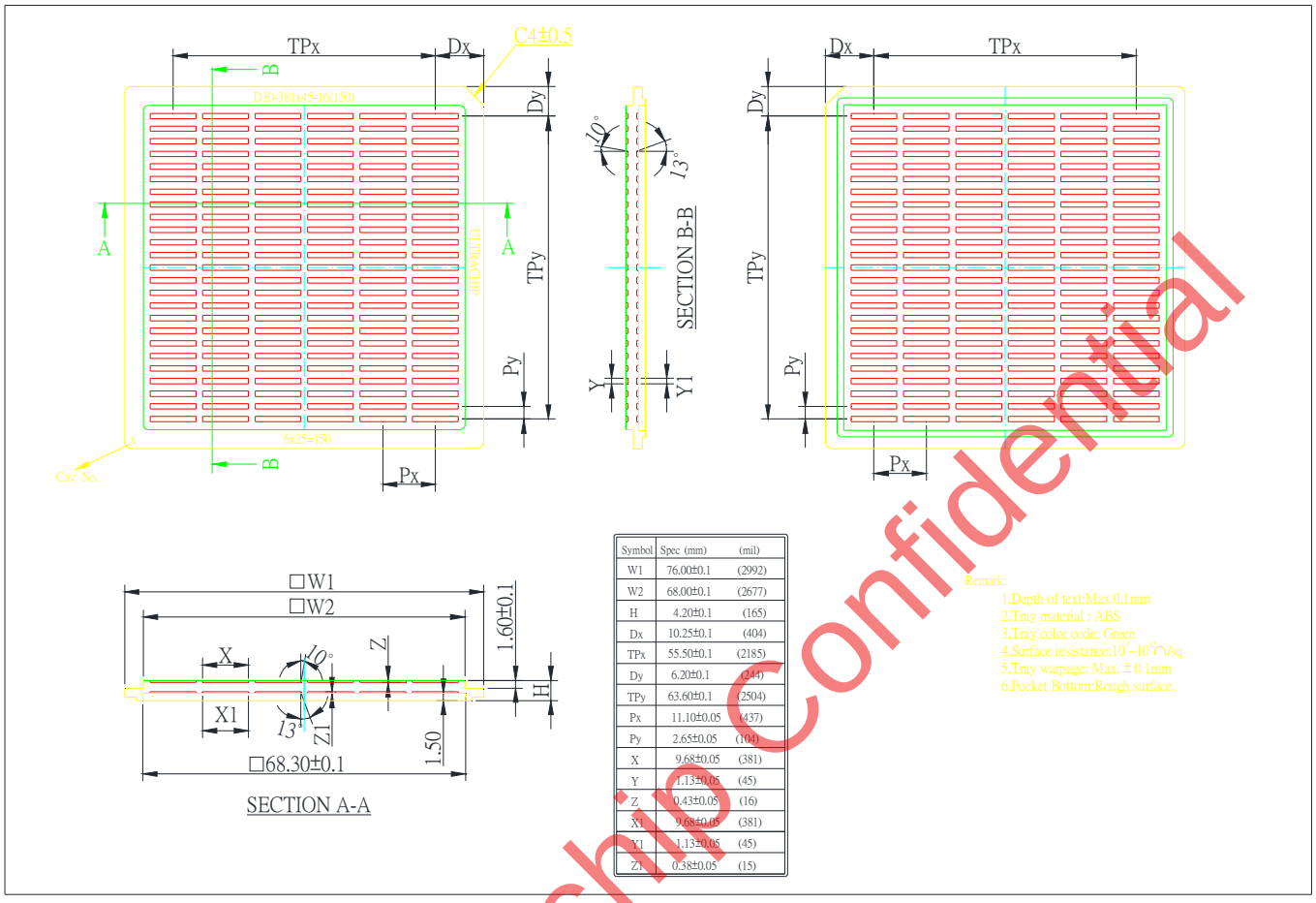
648	G<75>	-3637	313.5	18	75
649	G<73>	-3658	413.5	18	75
650	G<71>	-3679	313.5	18	75
651	G<69>	-3700	413.5	18	75
652	G<67>	-3721	313.5	18	75
653	G<65>	-3742	413.5	18	75
654	G<63>	-3763	313.5	18	75
655	G<61>	-3784	413.5	18	75
656	G<59>	-3805	313.5	18	75
657	G<57>	-3826	413.5	18	75
658	G<55>	-3847	313.5	18	75
659	G<53>	-3868	413.5	18	75
660	G<51>	-3889	313.5	18	75
661	G<49>	-3910	413.5	18	75
662	G<47>	-3931	313.5	18	75
663	G<45>	-3952	413.5	18	75
664	G<43>	-3973	313.5	18	75
665	G<41>	-3994	413.5	18	75
666	G<39>	-4015	313.5	18	75
667	G<37>	-4036	413.5	18	75
668	G<35>	-4057	313.5	18	75
669	G<33>	-4078	413.5	18	75
670	G<31>	-4099	313.5	18	75
671	G<29>	-4120	413.5	18	75
672	G<27>	-4141	313.5	18	75
673	G<25>	-4162	413.5	18	75
674	G<23>	-4183	313.5	18	75
675	G<21>	-4204	413.5	18	75
676	G<19>	-4225	313.5	18	75
677	G<17>	-4246	413.5	18	75
678	G<15>	-4267	313.5	18	75
679	G<13>	-4288	413.5	18	75
680	G<11>	-4309	313.5	18	75
681	G<9>	-4330	413.5	18	75
682	G<7>	-4351	313.5	18	75
683	G<5>	-4372	413.5	18	75
684	G<3>	-4393	313.5	18	75
685	G<1>	-4414	413.5	18	75
686	NC	-4435	313.5	18	75
687	NC	-4456	413.5	18	75
688	NC	-4477	313.5	18	75
689	NC	-4498	413.5	18	75
690	NC	-4540	413.5	18	75
691	NC	-4519	313.5	18	75

Output Pad Location



TRAY INFORMATION

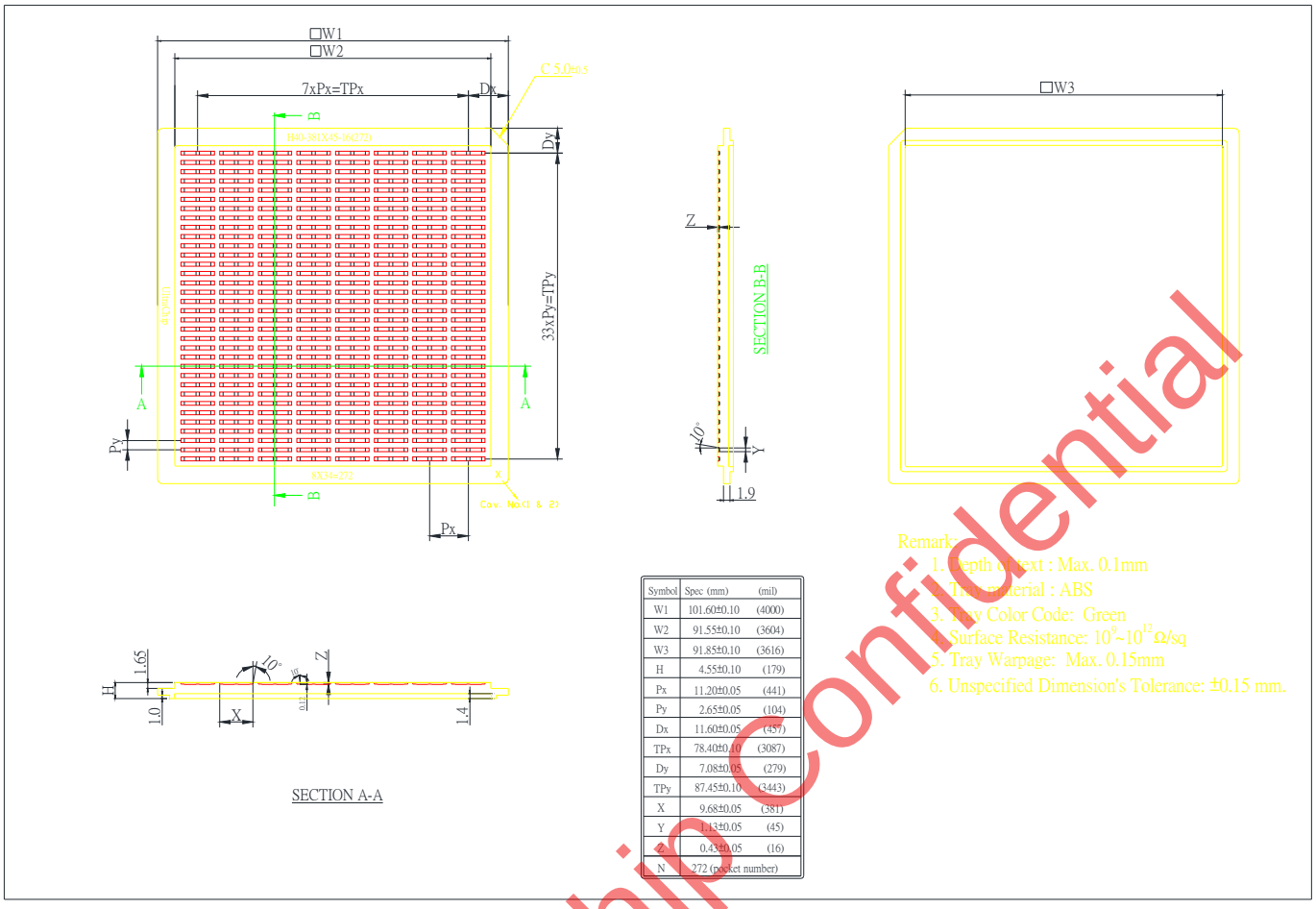
3-inch Tray



Symbol	Spec (mm)	(mil)
W1	76.00±0.1	(2992)
W2	68.00±0.1	(2677)
H	4.20±0.1	(165)
Dx	10.25±0.1	(404)
TPx	55.50±0.1	(2185)
Dy	6.20±0.1	(244)
TPy	63.60±0.1	(2504)
Px	11.10±0.05	(437)
Py	2.65±0.05	(104)
X	9.68±0.05	(381)
Y	1.13±0.05	(45)
Z	0.43±0.05	(16)
X1	9.68±0.05	(381)
Y1	1.13±0.05	(45)
Z1	0.38±0.05	(15)

Remark:
1.Depth of text:Max.0.1mm
2.Tray material : ABS
3.Tray color code: Green
4.Surface resistance:10^{4}~$10^{12}\Omega$/sq
5.Tray warpage: Max. ± 0.1mm
6.Pocket Bottom:Rough surface.

4-inch Tray



Symbol	Spec (mm)	(mil)
W1	101.60±0.10	(4000)
W2	91.55±0.10	(3604)
W3	91.85±0.10	(3616)
H	4.55±0.10	(179)
Px	11.20±0.05	(441)
Py	2.65±0.05	(104)
Dx	11.60±0.05	(457)
TPx	78.40±0.10	(3087)
Dy	7.08±0.05	(279)
TPy	87.45±0.10	(3443)
X	9.68±0.05	(381)
Y	1.13±0.05	(45)
Z	0.43±0.05	(16)
N	272 (pocket number)	

REVISION HISTORY

Revision	Contents	Date
0.6	(First Release)	Apr. 7, 2017