HIGH-VOLTAGE MIXED-SIGNAL IC

UC8157

All-in-one driver IC w/ TCON for
ESL Application

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ES Specifications
Datasheet Revision: 0.6

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INTRODUCTION

The UC8157c is an all-in-one driver with timing controller for ESL. Its output is of 2-bit white/black resolution per pixel. The timing controller provides control signals for both source drivers and gate drivers.

The DC-DC controller allows it to generate the source output voltage VDPS/VDNS (±2.4V~±8V). The chip also includes an output buffer for the supply of the COM electrode (VCOMAC or VCOMDC). The system is configurable through a 3-wire/4-wire (SPI) serial interface.

MAIN APPLICATIONS

- E-tag application

FEATURE HIGHLIGHTS

- System-on-chip (SOC) for ESL
- Timing controller supports several all-resolutions
- Preselectable resolution (SourcexGate):
  - 94x230
  - 94x252
  - 128x296
  - 200x300
- Built-in Frame memory (Max.): 300x200x2bit
- Support LUT1 (VCOM1, White, Black, Gray1, Gray2)
- Source Driver with 2-bit white/black resolution
  - 200 channels
  - Output dynamic range: VDNS, 0, VDPS
  - Output deviation: 0.2 V
  - Left and Right shift capability
- Gate Driver:
  - 300 channel outputs
  - Output voltage VDNG+40
  - Up and Down scan capability
- 3-wire/4-wire (SPI) serial interface
- DC-DC controller for generating the analog power supply
- COM electrode (VCOM AC) level
- Built-in temperature sensor
- Digital supply voltage: 2.3~ 3.6V
- Operating frequency: 20MHz (max)
- COG Package
- COM/SEG bump information
  Bump Pitch: 42μM
  Bump Gap: 24μM ± 3μM
  Bump Area: 114300uM^2

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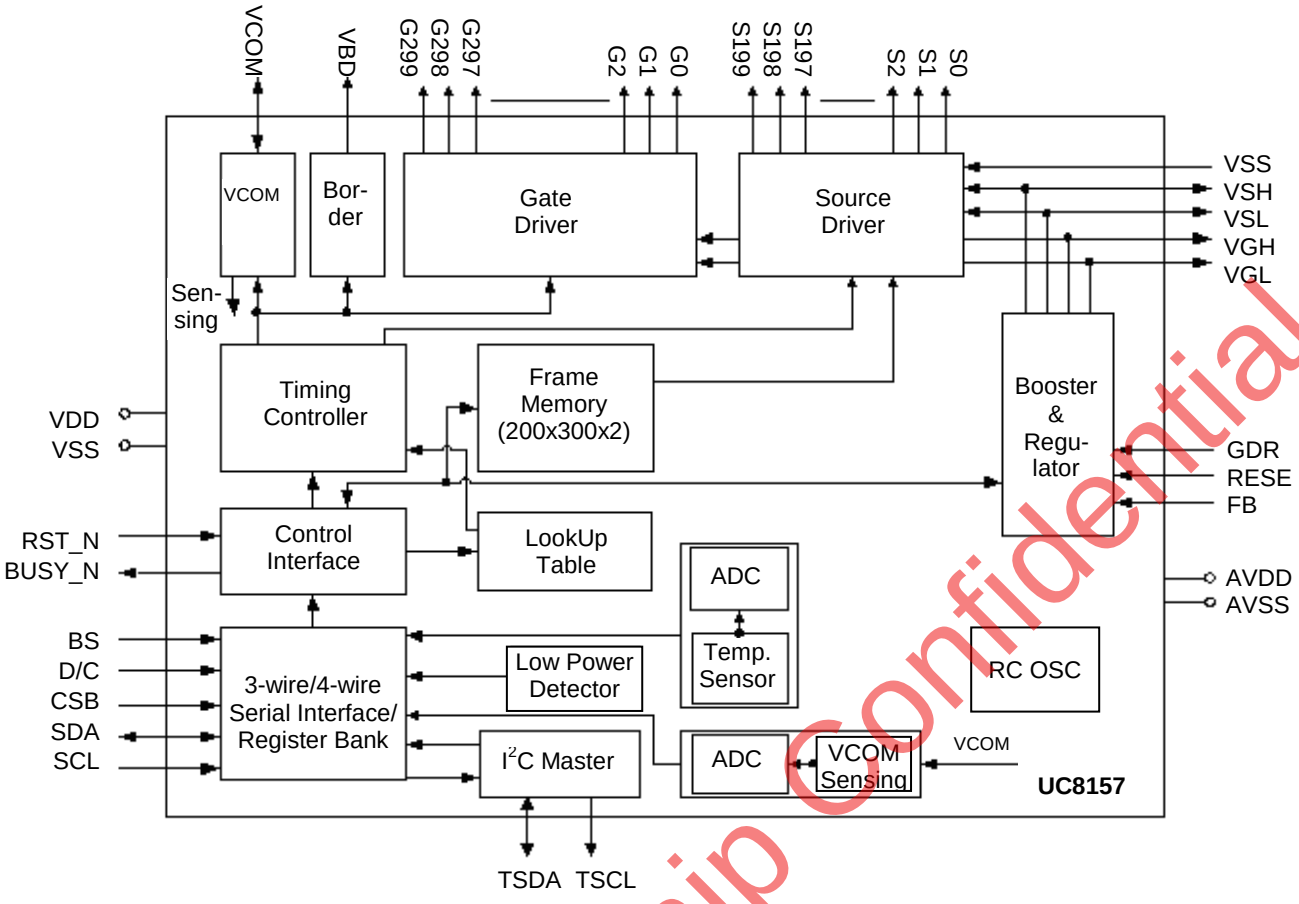
BLOCK DIAGRAM



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ORDERING INFORMATION

Part Number	I^2C	Description
UC8157cGAB-N0P		COG, with 4-inch Tray
UC8157cGAB-N0P3-3		COG, with 3-inch double-sided Tray

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General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

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PIN DESCRIPTION

Type: I: Input, O: Output, I/O: Input/Output, P: Power, C: Capacitor pin

Pin (Pad) Name	Pin Count	Type	Description
POWER SUPPLY			
VDD	7	P	Digital power
VDDA	10	P	Analog power
VDDIO	10	P	IO power
GND	18	P	Digital Ground.
GNDA	17	P	Analog Ground
VDM	4	P	Driver Ground
SERIAL COMMUNICATION INTERFACE			
CSB	1	I (Pull-up)	Serial communication chip select.
SDA	1	I/O	Serial communication data input.
SCL	1	I	Serial communication clock input.
DC	1	I	Serial communication Command/Data input. L: command H: data
CONTROL INTERFACE			
BS	1	I (Pull-up)	Input interface setting. Select 3 wire/ 4 wire SPI interface L: 4-wire IF. **H: 3-wire IF. (Default)**
RST_N	1	I (Pull-up)	Global reset pin. Low: reset. When RST_N become low, driver will reset. All register will be reset to default value, and all driver functions will be disabled. SD output and VCOM will base on previous condition; and they may have two conditions: 0v or floating.
BUSY_N	1	O	This pin indicates the driver status. L: Driver is busy, data/VCOM is transforming. H: non-busy. Host side can send command/data to driver.
TEST1~7	7	--	Test pins. Reserved for testing. Leave them open.
TSCL	2	O	I^2C clock for external temperature sensor.
TSDA	2	I/O	I^2C data for external temperature sensor.

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Pin (Pad) Name	Pin Count	Type	Description
OUTPUT DRIVER			
S[0..199] (S<0>~S<199>)	200	O	Source driver output signals.
G[0..299] (G<0>~G<299>)	300	O	Gate driver output signals.
VBD (VBD<1>~VBD<2>)	2	O	Border output pins. It outputs black WF.
CL	1	I/O	Clock pin for cascade mode. In single-chip mode, keep CL open. In cascade mode, the CL pin of the slave chip should be connected to the CL pin of the master chip.
MS	1	I	Master/Slave selection for cascade mode. Low: Slave, High: Master In single-chip mode, MS should be connect to VDD.
VSYNC	1	I/O	Vsync pin for cascade mode. In single-chip mode, VSYNC should be connected to GND or VDD. In cascade mode, VSYNC pin of slave chip shoulde be connected to VSYNC pin of master chip.
VCOM GENERATOR			
VCOM	16	O	VCOM output. It has the following voltage states: (VDPS+VCM_DC) V, (VCM_DC) V, (VDNS+VCM_DC) V, Floating
POWER CIRCUIT			
GDR	8	O	N-MOS gate control
RESE	2	P	Current sense input for control loop.
FB	2	P	(Keep Open.)
VGH	20	C	Positive Gate voltage.
VGL	24	C	Negative Gate voltage.
VSH	10	C	Positive Source voltage.
VSL	10	C	Negative Source voltage.
MISC. PINS			
NC	40		Not Connected.
Dummy	26		Dummy pins.

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COMMAND TABLE

W/R: 0: Write Cycle 1: Read Cycle C/D: 0: Command / 1: Data D7~D0: –: Don't Care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00h
		0	1	#	#	--	1	#	#	#	#	RES, UD, SHL, SHD_N, RST_N	1Fh
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01h
		0	1	--	--	--	--	--	--	#	#	VDS_EN, VDG_EN	03h
		0	1	--	--	--	--	--	--	#	#	VGHL_LV	00h
3	Power OFF (POF)	0	0	0	0	0	0	0	0	1	0		02h
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1		03h
		0	1	--	--	#	#	--	--	--	--	T_VDS_OFF	00h
5	Power ON (PON)	0	0	0	0	0	0	0	1	0	0		04h
6	Power ON Measure (PMES)	0	0	0	0	0	0	0	1	0	1		05h
7	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06h
		0	1	--	#	#	#	#	#	#	#	BT_PHA[6:0]	0Fh
		0	1	--	#	#	#	#	#	#	#	BT_PHB[6:0]	0Eh
		0	1	--	--	--	#	#	#	#	#	BT_PHC[4:0]	0Dh
8	Display Start Transmission 1 (DTM1) (x-byte command)	0	0	0	0	0	1	0	0	0	0		10h
		0	1	#	#	#	#	#	#	#	#	KPixel1, KPixel2, KPixel3, KPixel4	00h
		0	1	..	..	..	..	..	..	..	..	..	:
		0	1	#	#	#	#	--	--	--	--	KPixel(n-1), KPixel(n)	00h
9	Data Stop (DSP)	0	0	0	0	0	1	0	0	0	1		11h
		1	1	#	--	--	--	--	--	--	--	data_flag	--
10	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12h
11	Vcom1 LUT (LUTC1) (16-byte command, bytes 2~4 repeated 5 times)	0	0	0	0	1	0	0	0	0	0		20h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
12	White LUT (LUTW) (16-byte command, bytes 2~4 repeated 5 times)	0	0	0	0	1	0	0	0	0	1		21h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
13	Black LUT (LUTB) (16-byte command, bytes 2~4 repeated 5 times)	0	0	0	0	1	0	0	0	1	0		22h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
14	Gray1 LUT (LUTG1) (16-byte command, bytes 2~4 repeated 5 times)	0	0	0	0	1	0	0	0	1	1		23h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
15	Gray2 LUT (LUTG2) (16-byte command, bytes 2~4 repeated 5 times)	0	0	0	0	1	0	0	1	0	0		24h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
16	PLL control (PLL)	0	0	0	0	1	1	0	0	0	0		30h
		0	1	--	--	#	#	#	#	#	#	M, N	2Ah
17	Temperature Sensor Calibration (TSC)	0	0	0	1	0	0	0	0	0	0		40h
		1	1	#	#	#	#	#	#	#	#	TSE[D10:D0] / TS[3:0]	00h
		1	1	#	#	#	--	--	--	--	--		
18	Temperature Sensor Selection (TSE)	0	0	0	1	0	0	0	0	0	1		41h
		0	1	#	--	--	--	--	--	--	--	TSE	00h
19	Temperature Sensor Write (TSW)	0	0	0	1	0	0	0	0	1	0		42h
		0	1	#	#	#	#	#	#	#	#	WATTR[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WMSB[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WLSB[7:0]	00h

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#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
20	Temperature Sensor Read (TSR)	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**		**43h**
		1	1	#	#	#	#	#	#	#	#	RMSB[7:0]	00h
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00h
21	Vcom and data interval setting (CDI)	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**		**50h**
		0	1	--	--	#	#	#	#	#	#	SD_BDHZ, DDX, CDI	17h
22	Lower Power Detection (LPD)	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**		**51h**
		1	1	--	--	--	--	--	--	--	#	LPD	--
23	TCON setting (TCON)	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**		**60h**
		0	1	#	#	#	#	#	#	#	#	S2G, G2S	22h
24	Resolution setting (TRES)	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**1**		**61h**
		0	1	#	#	#	#	#	#	#	**0**	HRES	00h
		0	1	--	--	--	--	--	--	--	#	VRES[8:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
25	Revision (REV)	0	0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**		**70h**
		1	1	0	0	0	0	0	0	0	0		00h
26	Get Status (FLG)	0	0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**1**		**71h**
		1	1	--	--	--	--	--	--	#	#	I2C_ERR, I2C_BUSYN, data_flag, PON, POF, BUSY_N	02h
27	Auto Measurement Vcom	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**		**80h**
		0	1	--	--	#	#	--	--	#	#	AMVT, AMV, AMVE	10h
28	Read Vcom Value(VV)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**		**81h**
		1	1	--	--	#	#	#	#	#	#	VV	00h
29	VCM_DC Setting (VDCS)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**		**82h**
		0	1	--	--	#	#	#	#	#	#	VDCS	00h

Note: (1) All other register addresses are invalid or reserved by UltraChip, and should NOT be used.

(2) Any bits shown here as 0 must be written with a 0. All unused bits should also be set to zero. Device malfunction may occur if this is not done.

(3) Commands are processed on the 'stop' condition of the interface.

(4) Registers marked 'W/R' can be read, but the contents are written when the SPI command completes – so the contents can be read and altered. The user can subsequently write the register to restore the contents following an SPI read.

(5) All registers are accessible, (i.e., Host can send command/data to driver), only when BUSY_N =1; except R01h (PWR), R03h (PFS), R04h (PON), R05h (PMES), R06h(BTST), R51h (LPD), and R71h(FLG), which are accessible either when BUSY_N=0 or 1.

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COMMAND DESCRIPTION

W/R: 0: Write Cycle / 1: Read Cycle C/D: 0: Command / 1: Data D7-D0: –: Don't Care

(1) PANEL SETTING (PSR) (REGISTER: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting the panel	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
	0	1	RES1	RES0	--	1	UD	SHL	SHD_N	RST_N

RES[1:0]: Display Resolution setting (source x gate)

00b: 94x230 (Default)	Active source channels: S0 ~ S93. Active gate channels: G0 ~ G229.
01b: 94x252	Active source channels: S0 ~ S93. Active gate channels: G0 ~ G251.
10b: 128x296	Active source channels: S0 ~ S127. Active gate channels: G0 ~ G295.
11b: 200x300	Active source channels: S0 ~ S199. Active gate channels: G0 ~ G299.

UD:

0: Scan down.	First line to Last line: Gn-1 → Gn-2 → Gn-3 → … → G0
1: Scan up. (Default)	First line to Last line: G0 → G1 → G2 → … … . → Gn-1

SHL:

0: Shift left.	First data to Last data: Sn-1 → Sn-2 → Sn-3 → … → S0
1: Shift right. (Default)	First data to Last data: S0 → S1 → S2 → … … . → Sn-1

SHD_N: 0: DC-DC converter will be turned OFF
1: DC-DC converter will be turned ON (Default)

When SHD_N become LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF, and SD output and VCOM will remain previous condition. SHD_N may have two conditions: 0v or floating.

RST_N: 0: The controller is reset. Reset all registers to default value.
1: No effect (Default)

When RST_N becomes LOW, the driver will be reset, all registers will be reset to their default value. All driver functions will be disabled. SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

This command can be active only when BUSY_N = "1".

(2) POWER SETTING (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Selecting Internal/External Power	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
	0	1	-	-	-	-	-	-	VDS_EN	VDG_EN
	0	1	-	-	-	-	-	-	VGHL_LV[1:0]	

VDS_EN: Source power selection
0 : External source power from VDH/VDL pins
1 : Inetrnal DC/DC function for generating VDH/VDL

VDG_EN: Gate power selection
0 : External gate power from VGH/VGL pins
1 : Internal DC/DC function for generating VGH/VGL

VGHL_LV[1:0]: VGHL_LVL / VDNG_LVL power selection.

VGHL_LV	VGHL_LVL power
00 (DEFAULT)	VGH=20V, VGL= -19.3V
01	VGH=19V, VGL= -18.3V
10	VGH=18V, VGL= -17.3V
11	VGH=17V, VGL= -16.3V

This command can be active only when BUSY_N = "1".

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(3) POWER OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning OFF the power	0	0	0	0	0	0	0	0	1	0

After the Power Off command, driver will power off based on the Power Off Sequence, BUSY_N will become ”0”. This command will turn off charge pump, T-con, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD becomes OFF.

SD output and Vcom will base on previous condition. It may have 2 conditions: 0V or floating.

This command can be active only when BUSY_N = “1”.

(4) POWER OFF SEQUENCE SETTING (PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	0
	0	1	-	-	T_VDS_OFF[1:0]		-		-	

T_VDS_OFF[1:0]: Power OFF Sequence of VDPS and VDNS.

00b: 1 frame (Default)
01b: 2 frames
10b: 3 frames
11b: 4 frame

This command can be active only when BUSY_N = “1”.

(5) POWER ON (PON) (REGISTER: R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning ON the power	0	0	0	0	0	0	0	1	0	0

After the Power ON command, the driver will be powered ON following the Power ON Sequence. After the Power ON command and all power sequence are ready, the BUSY_N signal will become “1”. Refer to the Power ON Sequence section.

(6) POWER ON MEASURE (PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning ON the power	0	0	0	0	0	0	0	1	0	1

This command releases BUSY_N restriction for command TSC and command LPD until next Power Off.

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(7) BOOSTER SOFT START (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**
	0	1	-	BTPHA6	BTPHA5	BTPHA4	BTPHA3	BTPHA2	BTPHA1	BTPHA0
	0	1	-	BTPHB6	BTPHB5	BTPHB4	BTPHB3	BTPHB2	BTPHB1	BTPHB0
	0	1	-	-	-	BTPHC4	BTPHC3	BTPHC2	BTPHC1	BTPHC0

BTPHA[6:5]: Soft start period of phase A. **00b: 10mS** 01b: 20mS 10b: 30mS 11b: 40mS

BTPHA[4:3] : Driving strength of phase A

00b: strength 1 **01b: strength 2** 10b: strength 3 11b: strength 4 (strongest)

BTPHA[2:0] : Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHB[6:5] : Soft start period of phase B. **00b: 10mS** 01b: 20mS 10b: 30mS 11b: 40mS

BTPHB[4:3] : Driving strength of phase B

00b: strength 1 **01b: strength 2** 10b: strength 3 11b: strength 4 (strongest)

BTPHB[2:0] : Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS **110b: 3.34uS** 111b: 6.58uS

BTPHC[4:3] : Driving strength of phase C

00b: strength 1 **01b: strength 2** 10b: strength 3 11b: strength 4 (strongest)

BTPHC[2:0] : Minimum OFF time setting of GDR in phase C

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS **101b: 1.54uS** 110b: 3.34uS 111b: 6.58uS

(8) DATA START TRANSMISSION 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**
	0	1	kpixel1[1:0]		kpixel2[1:0]		kpixel3[1:0]		kpixel4[1:0]	
	0	1	**…**		**…**		**…**		**…**	
	0	1	kpixel(n-1)[1:0]		kpixel(n)[1:0]		-	-	-	-

This command starts transmitting data and write them into SRAM. To complete data transmission, command DSP (Data transmission Stop) must be issued. Then the chip will start to send data/VCOM for panel.

KPixel(x)[1:0]:

DDX	KPixel (x) [1:0]	LUT
0	00	White
	01	Gray2
	10	Gray1
	11	Black
1	00	Black
	01	Gray1
	10	Gray2
	11	White

This command can be active only when BUSY_N = “1”.

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(9) DATA STOP (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Stopping data transmission	0	0	0	0	0	1	0	0	0	1
	1	1	data_flag	-	-	-	-	-	-	-

To stop data transmission, this command must be issued to check the data_flag.

Data_flag: Data flag of receiving user data.
0: Driver didn't receive all the data.
1: Driver has already received all the one-frame data.

This command can be active only when BUSY_N = "1". After data start (10h) and data stop (11h) command, BUSY_N signal will become "0".

(10) DISPLAY REFRESH (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Refreshing the display	0	0	0	0	0	1	0	0	1	0

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.

This command can be active only when BUSY_N = "1". After display refresh command, BUSY_N signal will become "0".

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(11) VCOM1 LUT (LUTC1) (R20H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-up Table for Vcom 1 (16-byte command, Bytes 2~4 repeated 5 times)	0	0	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**
	0	1	LEVEL SELECT.		NUMBER OF FRAMES					
	0	1	LEVEL SELECT.		NUMBER OF FRAMES.					
	0	1	TIMES TO REPEAT							
	0	1	:		:					
	0	1	:		:					
	0	1	:							
	0	1	:		:					
	0	1	:		:					
	0	1	:							
	0	1	:		:					
	0	1	:		:					
	0	1	:							
	0	1	:		:					
	0	1	:		:					
	0	1	:							

This command stores VCOM Look-Up Table with 5 groups of data. Each group contains information for one phase and is stored with 3 bytes, while the third byte indicates how many times that phase will repeat.

Bytes 2, 3, 5, 6, 8, 9, 11, 12, 14, 15:

{D7:D6}: Level selection.

00b: VCM_DC
01b: 15V+VCM_DC (VCOMH)
10b: -15V+VCM_DC (VCOML)
11b: Floating

{D5:D0}: Number of Frames.

00 0000b: 0 frame
: :
: :
11 1111b: 63 frames

Bytes 4, 7, 10, 13, 16:

{D7:D0}: Times to repeat

(12) WHITE LUT (LUTW) (R21H)

This command builds Look-up Table for White. Please refer to command (11) Vcom1 LUT (LUTC1) for similar definition details.

(13) BLACK LUT (LUTB) (R22H)

This command builds Look-up Table for Black. Please refer to command (11) Vcom1 LUT (LUTC1) for similar definition details.

(14) GRAY1 LUT (LUTG1) (R23H)

This command builds Look-up Table for Gray 1. Please refer to command (11) Vcom1 LUT (LUTC1) for similar definition details.

(15) GRAY2 LUT (LUTG2) (R24H)

This command builds Look-up Table for Gray 2. Please refer to command (11) Vcom1 LUT (LUTC1) for similar definition details.

For commands (12)~(15), Level selection : 00b: 0V 01b: 15V (VSH) 10b: -15V (VSL) 11b: floating

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(16) PLL CONTROL (PLL) (R30H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Controlling PLL	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**
	0	1	-	-	M[2:0]			N[2:0]		

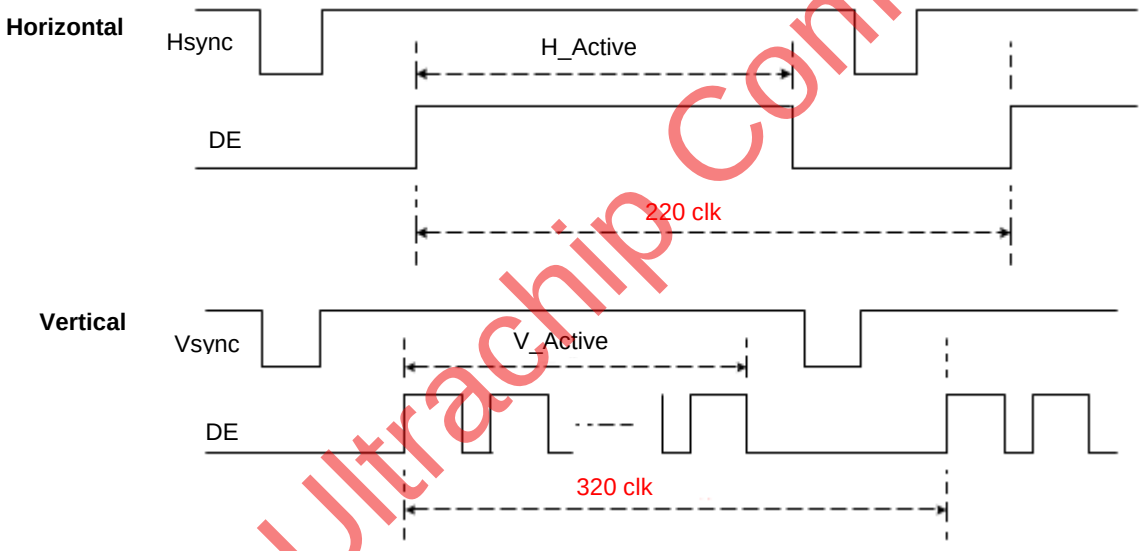
The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

M	N	Frame rate
1	1	20 Hz
	2	10 Hz
	3	7 Hz
	4	5 Hz
	5	4 Hz
	6	3 Hz
	7	3 Hz
2	1	39 Hz
	2	20 Hz
	3	13 Hz
	4	10 Hz
	5	8 Hz
	6	7 Hz
	7	6 Hz

M	N	Frame rate
3	1	59 Hz
	2	29 Hz
	3	20 Hz
	4	15 Hz
	5	12 Hz
	6	10 Hz
	7	8 Hz
4	1	78 Hz
	2	39 Hz
	3	26 Hz
	4	20 Hz
	5	16 Hz
	6	13 Hz
	7	11 Hz

M	N	Frame rate
5	1	98 Hz
	2	**50 Hz (default)**
	3	33Hz
	4	24 Hz
	5	20 Hz
	6	16 Hz
	7	14 Hz
6	1	117 Hz
	2	59 Hz
	3	39 Hz
	4	29 Hz
	5	23 Hz
	6	20 Hz
	7	17 Hz

M	N	Frame rate
7	1	137 Hz
	2	68 Hz
	3	46 Hz
	4	34 Hz
	5	27 Hz
	6	23 Hz
	7	20 Hz



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This command can be active only when BUSY_N = "1".

(17) TEMPERATURE SENSOR CALIBRATION (TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**
	1	1	D10	D9	D8	D7	D6 / TS3	D5 / TS2	D4 / TS1	D3 / TS0
	1	1	D2	D1	D0	-	-	-	-	-

This command reads the temperature sensed by the temperature sensor.

TS[3:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

(18) TEMPERATURE SENSOR ENABLE (TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Calibrate Temperature Sensor	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**
	0	1	TSE	-	-	-	-	-	-	-

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable (default) 1: Disable; using external sensor.

(19) TEMPERATURE SENSOR WRITE (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Calibrate Temperature Sensor	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**
	0	1	WATTR[7:0]							
	0	1	WMSB[7:0]							
	0	1	WLSB[7:0]							

This command reads the temperature sensed by the temperature sensor.

WATTR: **D[7:6]:** I^2C Write Byte Number
00 : 1 byte (head byte only)
01 : 2 bytes (head byte + pointer)
10 : 3 bytes (head byte + pointer + 1st parameter)
11 : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

D[5:3]: User-defined address bits (A2, A1, A0)

D[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor

WLSB[7:0]: LSByte of write-data to external temperature sensor

(20) TEMPERATURE SENSOR READ (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Calibrate Temperature Sensor	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**
	1	1	RMSB[7:0]							
	1	1	RLSB[7:0]							

This command reads the temperature sensed by the temperature sensor.

RMSB[7:0]: MSByte read data from external temperature sensor

RLSB[7:0]: LSByte read data from external temperature sensor

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(21) VCOM AND DATA INTERVAL SETTING (CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Interval between Vcom and Data	0	0	0	1	0	1	0	0	0	0
	0	1	-	-	SD_BDHZ	DDX	CDI[3:0]			

This command indicates the interval of Vcom and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync). This command can be active only when BUSY_N = "1".

SD_BDHZ: Border output selection
0 : Border output normal voltage 1 : Border floating

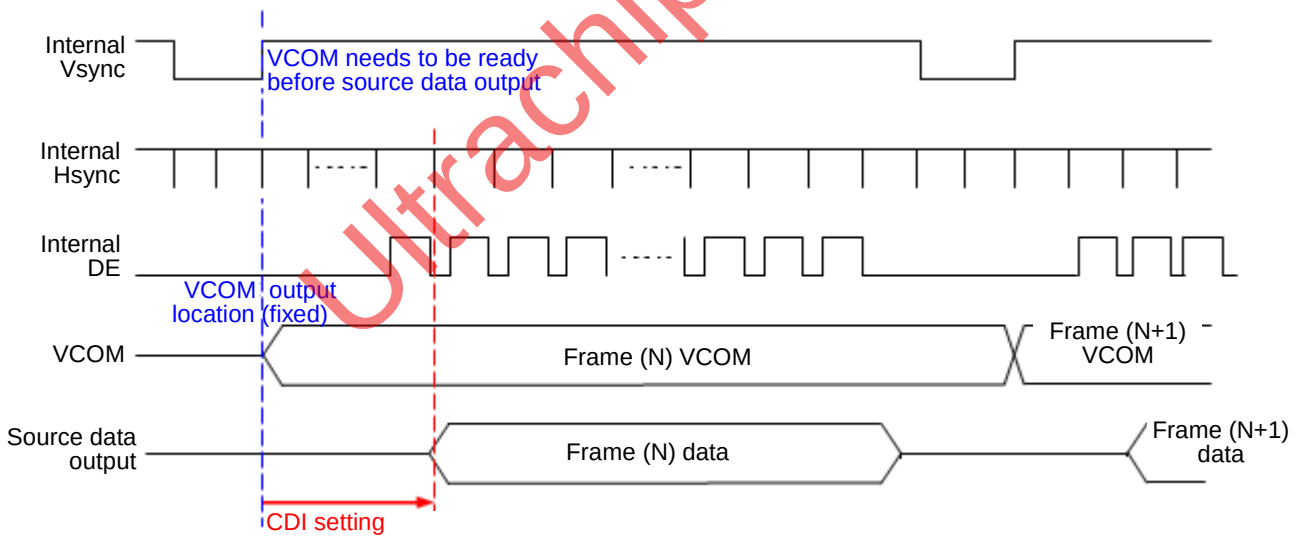
DDX: Mapping selection between pixel data and LUTs.

	KPixel(x)[1:0]	LUT
When DDX=0	00	White
	01	Gray2
	10	Gray1
	11	Black
When DDX=1	00	Black
	01	Gray1
	10	Gray2
	11	White

CDI[3:0]: Vcom and data interval

CDI[3:0]	Vcom and Data Interval
0000 b	17 hsync
0001	16
0010	15
0011	14
0100	13
0101	12
0110	11
0111	10 (Default)

CDI[3:0]	Vcom and Data Interval
1000	9
1001	8
1010	7
1011	6
1100	5
1101	4
1110	3
1111	2



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(22) LOW POWER DETECTION (LPD) (R51H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Detect Low Power	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**
	1	1	-	-	-	-	-	-	-	LPD

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal temperature sensor switch

0: Low power input (V_{DD}<2.5V) **1: Normal status (default)**

(23) TCON SETTING (TCON) (R60H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**
	0	1	S2G[3:0]				G2S[3:0]			

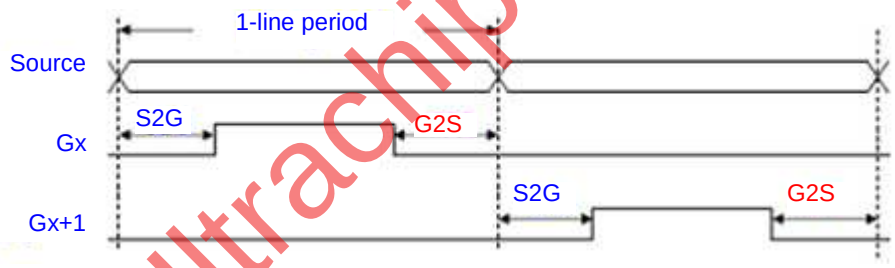
This command defines non-overlap period of Gate and Source. This command can be active only when BUSY_N = "1".

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period
0000 b	4 clock
0001	8
0010	12 (Default)
0011	16
0100	20
0101	24
0110	28
0111	32

S2G[3:0] or G2S[3:0]	Period
1000 b	36
1001	40
1010	44
1011	48
1100	52
1101	56
1110	(Reserved)
1111	(Reserved)

Clock frequency is 2MHz.



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(24) RESOLUTION SETTING (TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Resolution	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**1**
	0	1	HRES[7:1]							**0**
	0	1	-	-	-	-	-	-	-	VRES[8]
	0	1	VRES[7:0]							

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

HRES[7:1]: Horizontal Display Resolution

VRES[8:0]: Vertical Display Resolution

Active channel calculation:

GD : First G active = G0; LAST active GD= first active +VRES -1

SD : First active channel: =S0 ; LAST active SD= first active +HRES-1

Example: 128x296

GD: First G active = G0, LAST active GD= 0+296-1= 295; (G295)

SD: First active channel = S0, LAST active SD= 0+128-1=93; (S127)

This command can be active only when BUSY_N = "1".

(25) REVISION (REV) (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Chip Revision	0	0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**
	1	1	**0**	**0**	**0**	**0**	**0**			

This command can be active only when BUSY_N = "1".

(26) GET STATUS (FLG) (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read Flags	0	0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**1**
	1	1	-	-	I^2C_ERR	I^2C_ BUSYN	data_ flag	PON	POF	BUSY_N

This command reads the IC status.

I^2C_ERR: I^2C master error status

I^2C_BUSYN: I^2C master busy status (low active)

data_flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY_N: Driver busy status (low active)

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(27) AUTO MEASURE VCOM (AMV) (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure Vcom	0	0	1	0	0	0	0	0	0	0
	0	1	-	-	AMVT[1:0]		-	-	AMV	AMVE

This command reads the IC status.

AMVT[1:0]: Auto Measure Vcom Time

00b: 3s
10b: 8s
01b: 5s (default)
11b: 10s

AMV: 0 – Get Vcom value with the VV command (R81h)
1 – Get Vcom value in analog signal.

AMVE: Auto Measure Vcom Enable (/Disable)

0 – No effect
1 – Trigger auto Vcom sensing.

This command can be active only when BUSY_N = "1".

(28) VCOM VALUE (VV) (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure Vcom	0	0	1	0	0	0	0	0	0	1
	1	1	-	-	VV[5:0]					

This command gets the Vcom value.

VV[5:0]: Vcom Value

VV[5:0]	Vcom value
00 0000b	0 V (Default)
00 0001b	-0.1 V
00 0010b	-0.2 V
:	:
01 0100b	-2.0 V
:	:
10 1000b	-4.0 V
10 1001b	-4.1 V
:	:
11 1111b	-6.3 V

This command can be active only when BUSY_N = "1".

(29) VCM_DC SETTING (VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set VCM_DC	0	0	1	0	0	0	0	0	1	0
	0	1	-	-	VDCS[5:0]					

This command sets VCOM_DC value

VDCS[5:0]: Vcom Value

VDCS[5:0]	Vcom value
00 0000b	0 V (Default)
00 0001b	-0.1 V
00 0010b	-0.2 V
00 0011b	-0.3 V
:	:
01 1101b	-2.9 V
(others)	-3.0 V

This command can be active only when BUSY_N = "1".

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HOST INTERFACES

3-WIRE SPI

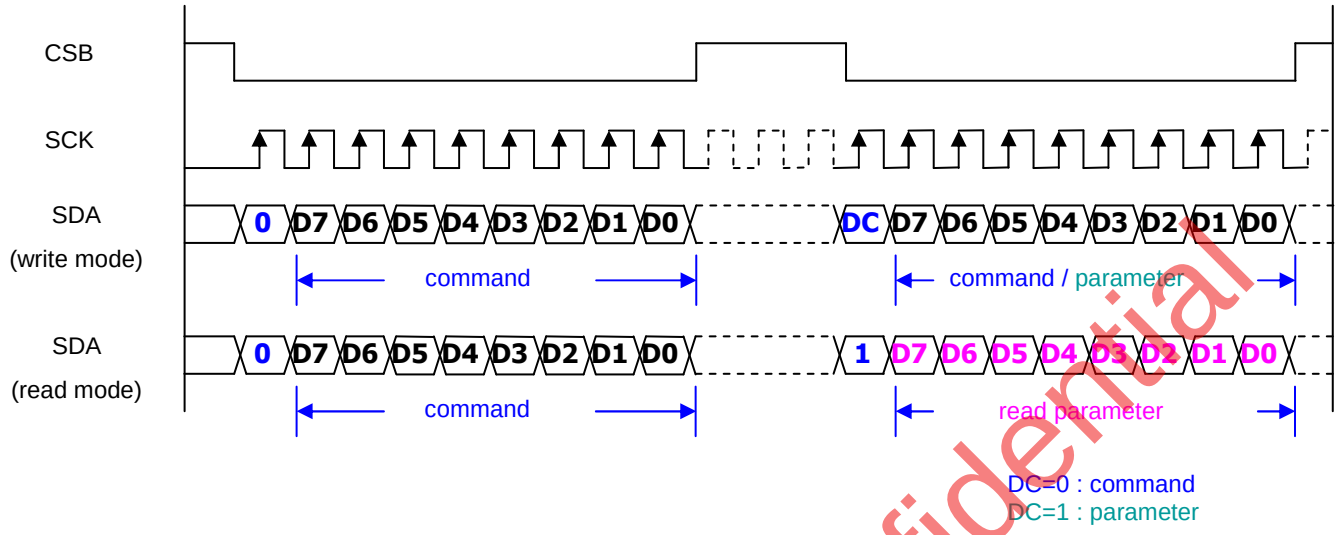

Figure : 3-wire SPI Typical Waveform – BS=1

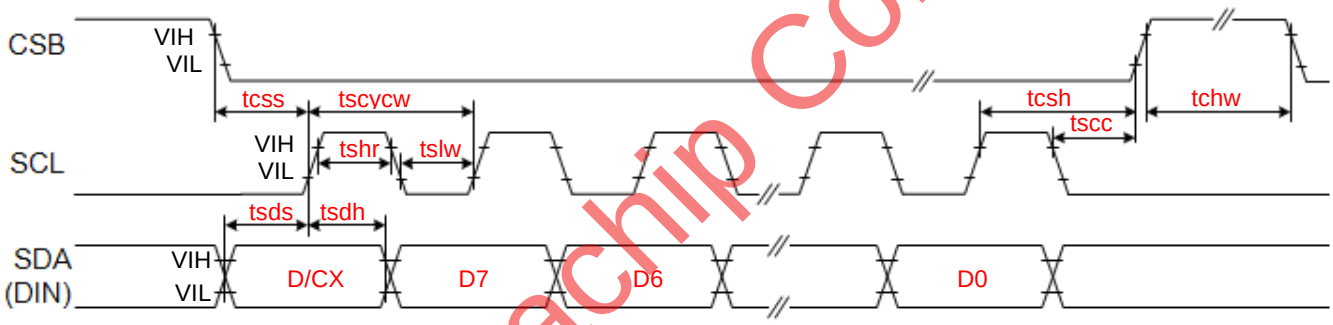

Figure : 3-wire Serial Interface – Write

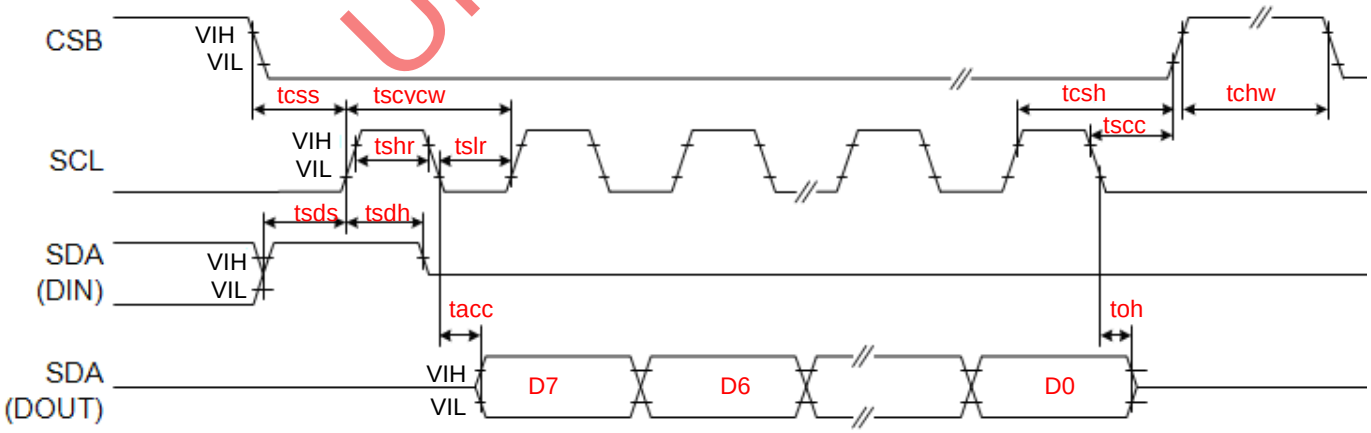

Figure : 3-wire Serial Interface – Read

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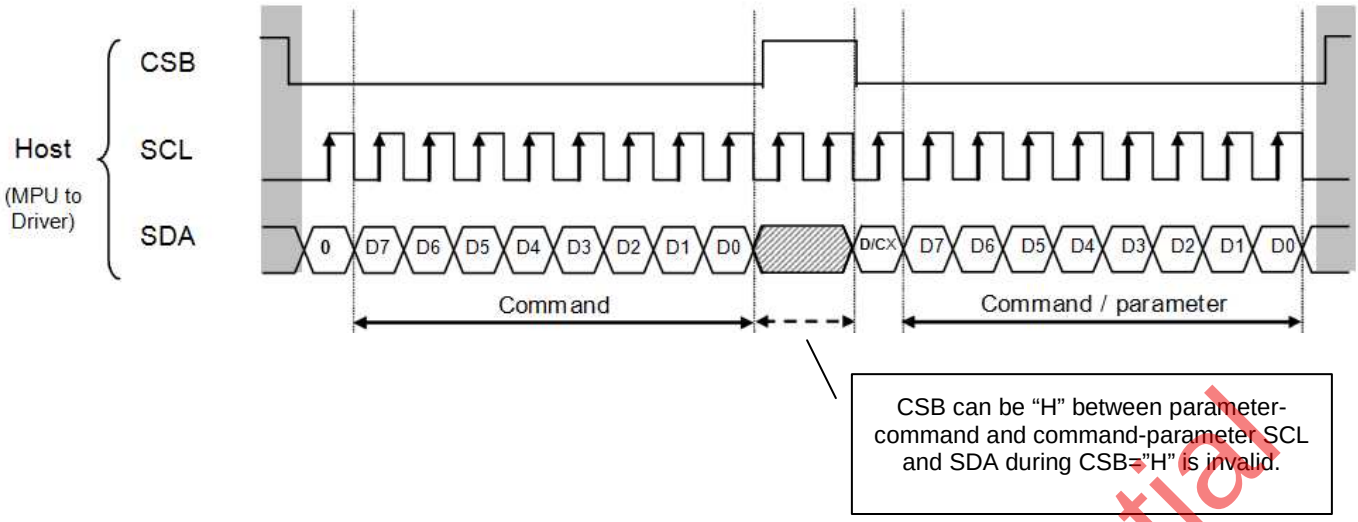

CSB can be “H” between parameter-command and command-parameter SCL and SDA during CSB=”H” is invalid.

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4-WIRE SPI

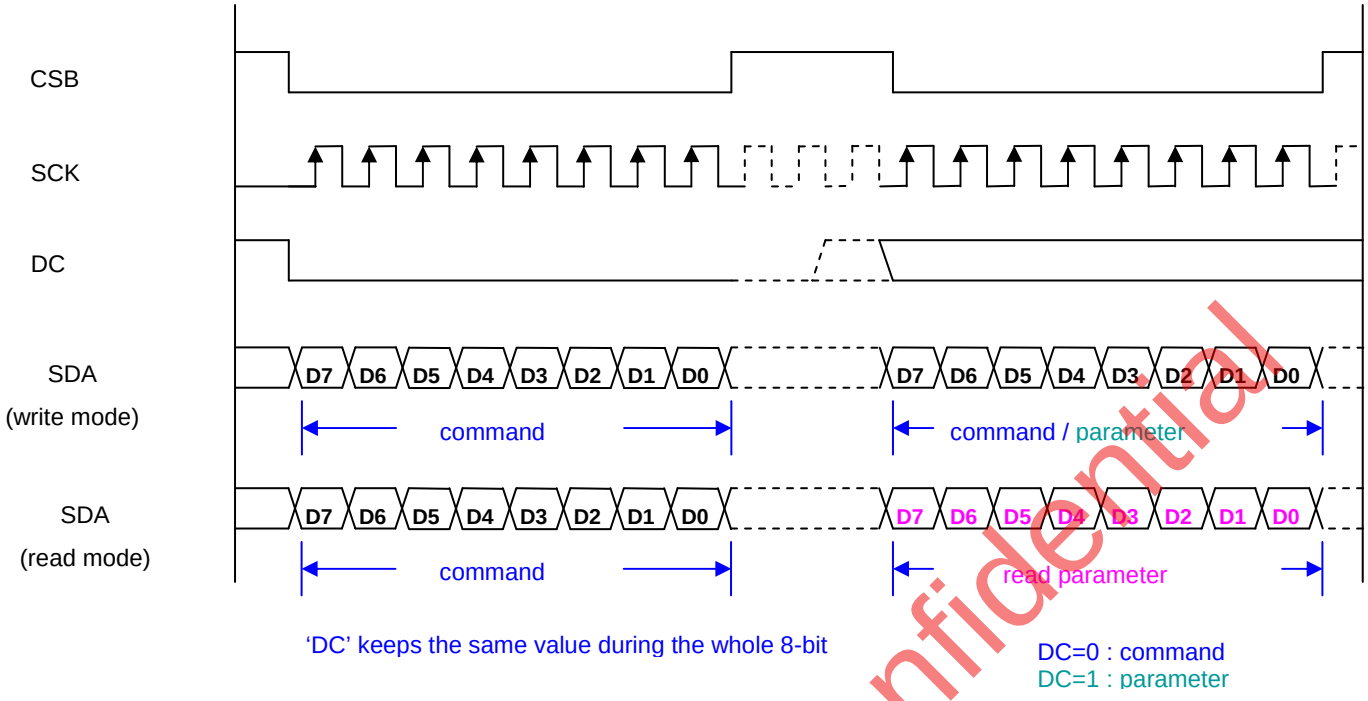

Figure : 4-wire SPI Typical Waveform – BS=0

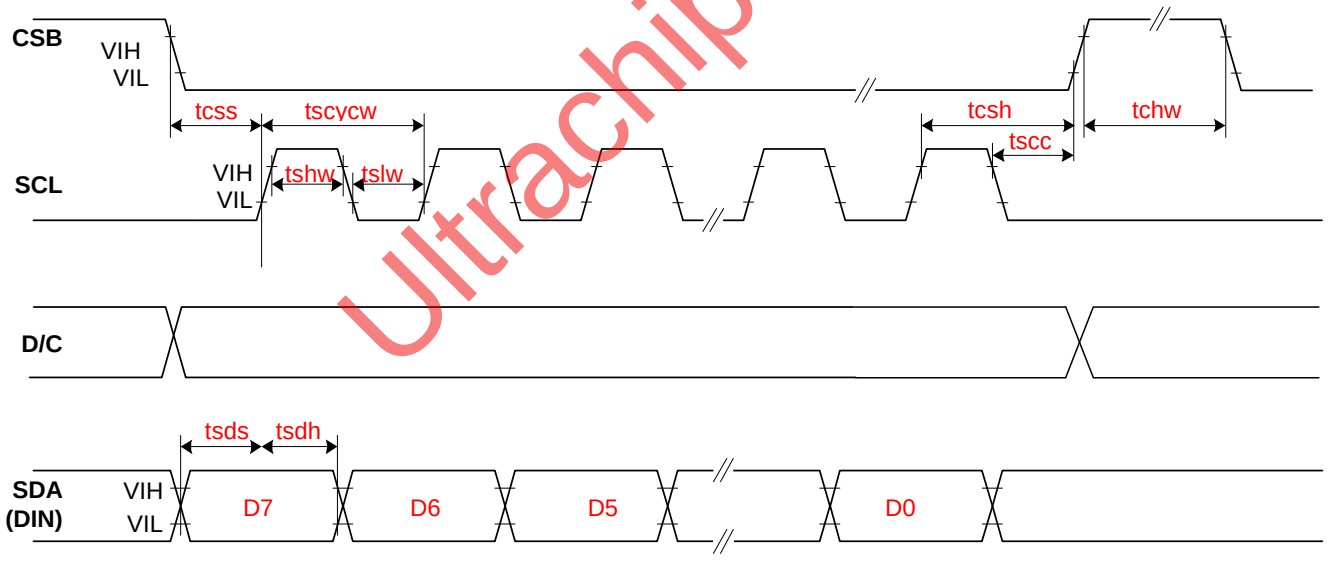

Figure : 4-wire Serial Interface – Read

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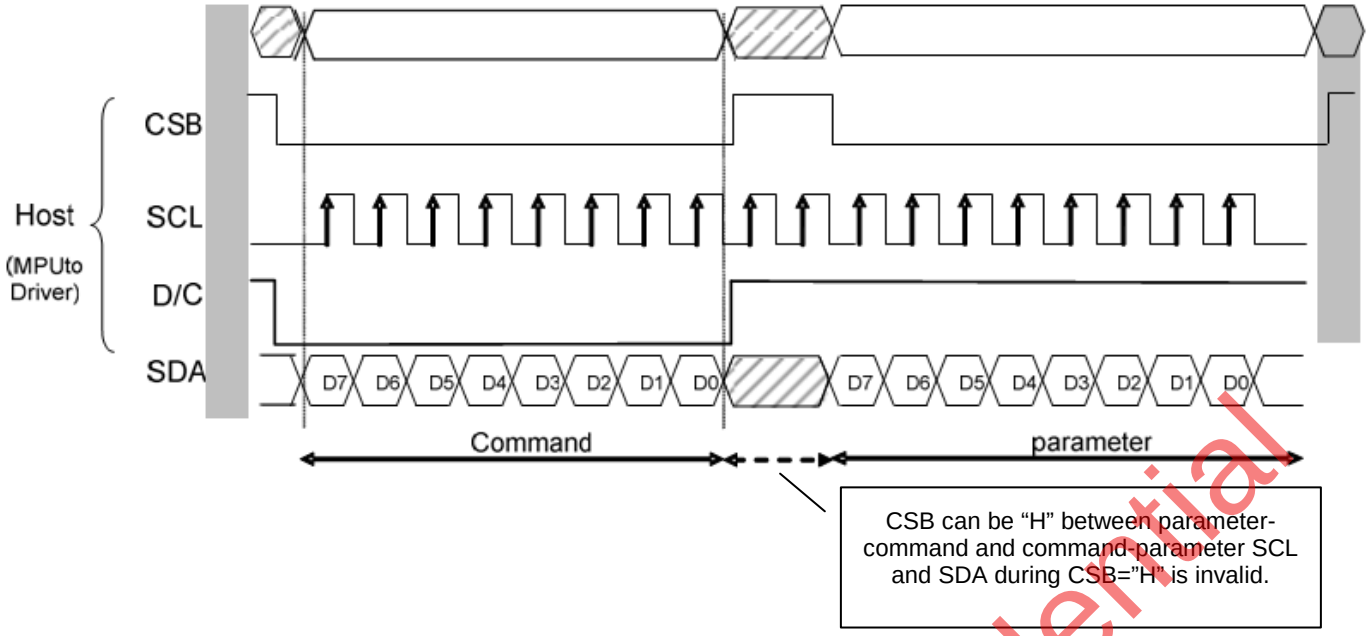

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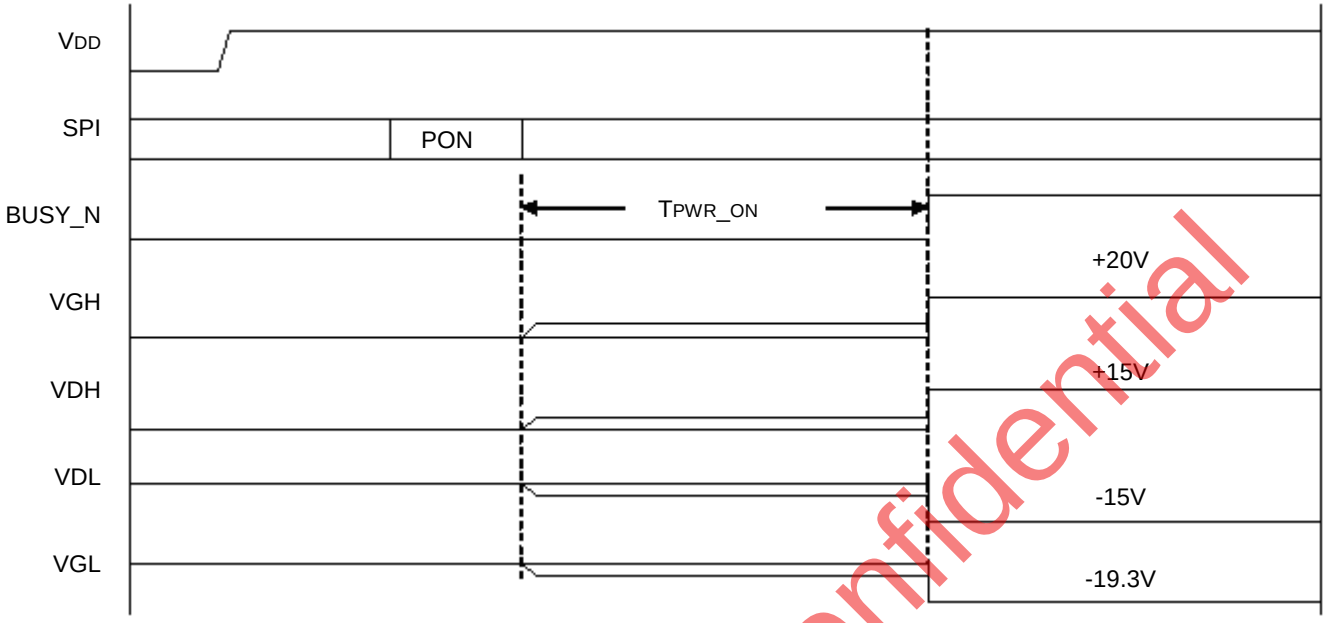
POWER MANAGEMENT

Power ON Sequence



TPWR_ON=~80mS (default)

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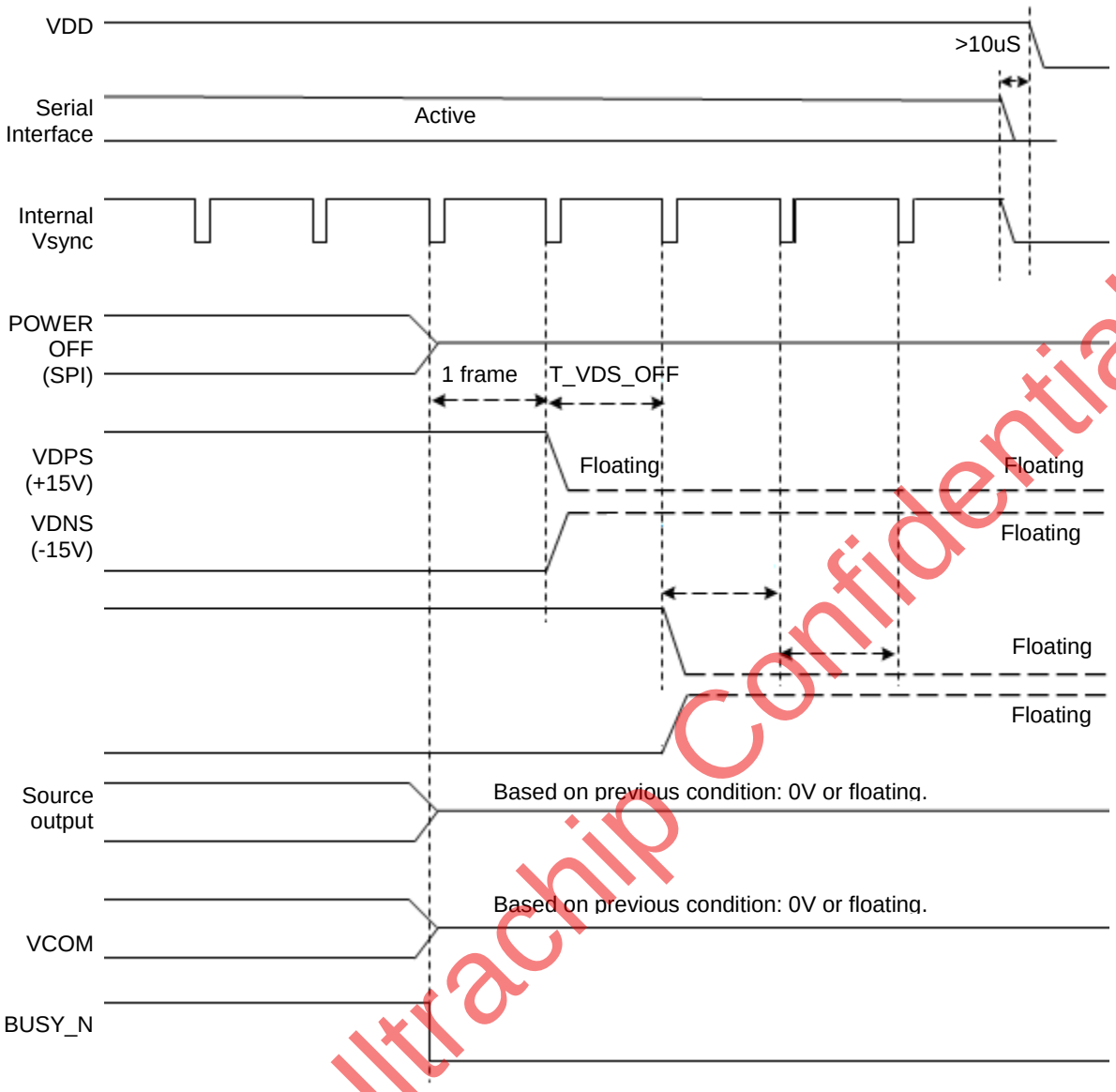
Power OFF Sequence



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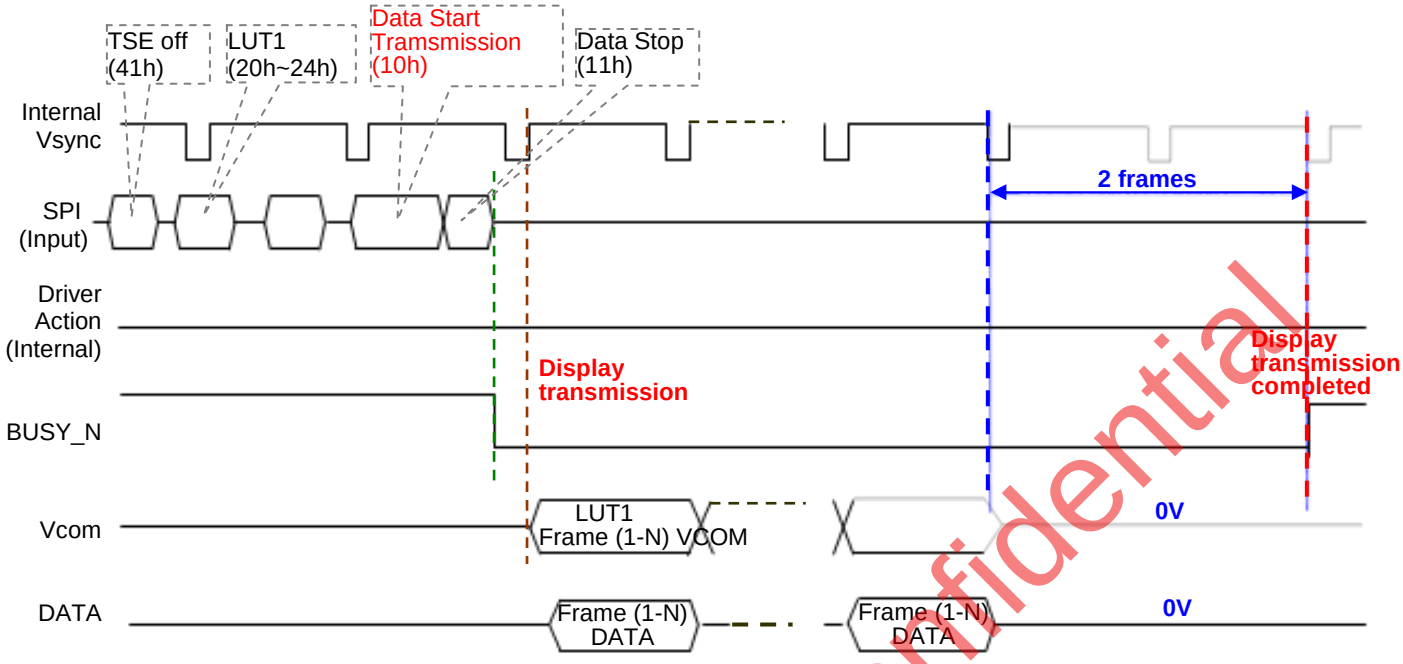
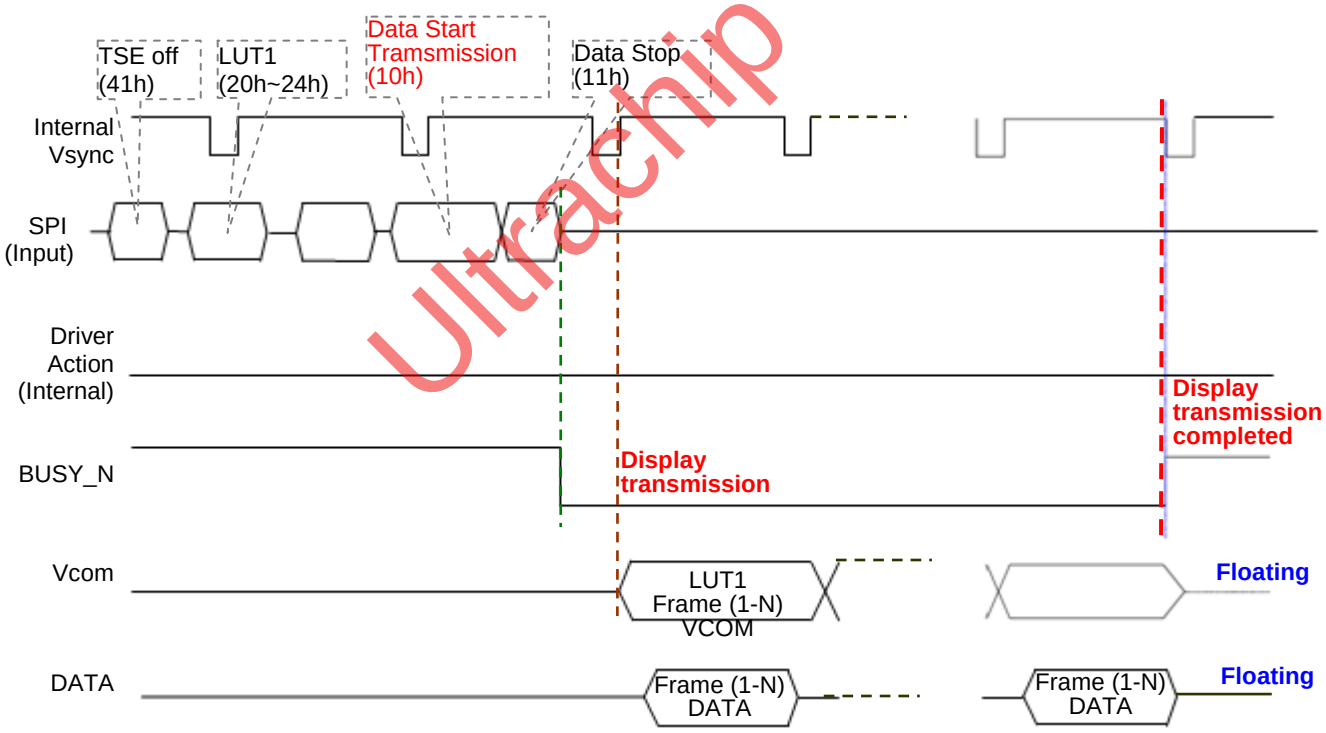
Data Transmission Waveform

Example 1: LUT all states (5 states) complete or phase number=0, the driver will send 2 frame VCOM and data to 0 V.



Example 2: While level selection in LUT is "11", the driver will float VCOM and data.



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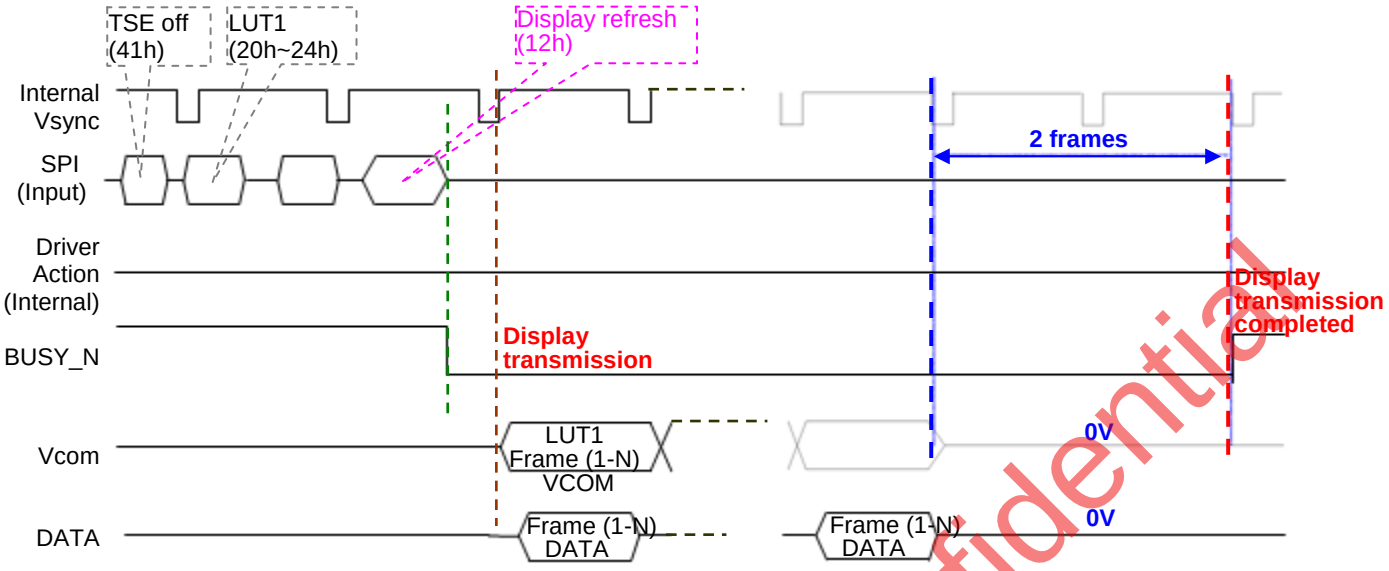
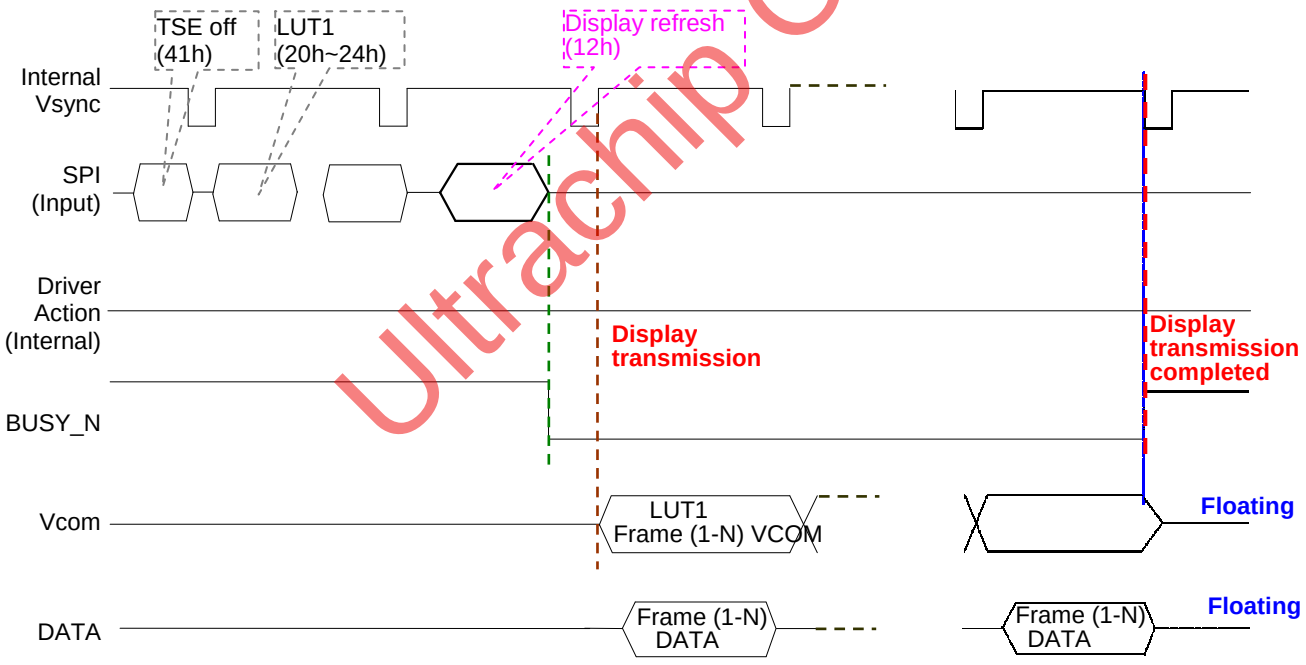
Display Refresh Waveform

Example 1: LUT all states (5 states) complete or phase number=0, the driver will send 2 frame VCOM and data to 0 V.



Example2: While level selection in LUT is "11", the driver will float VCOM and data.



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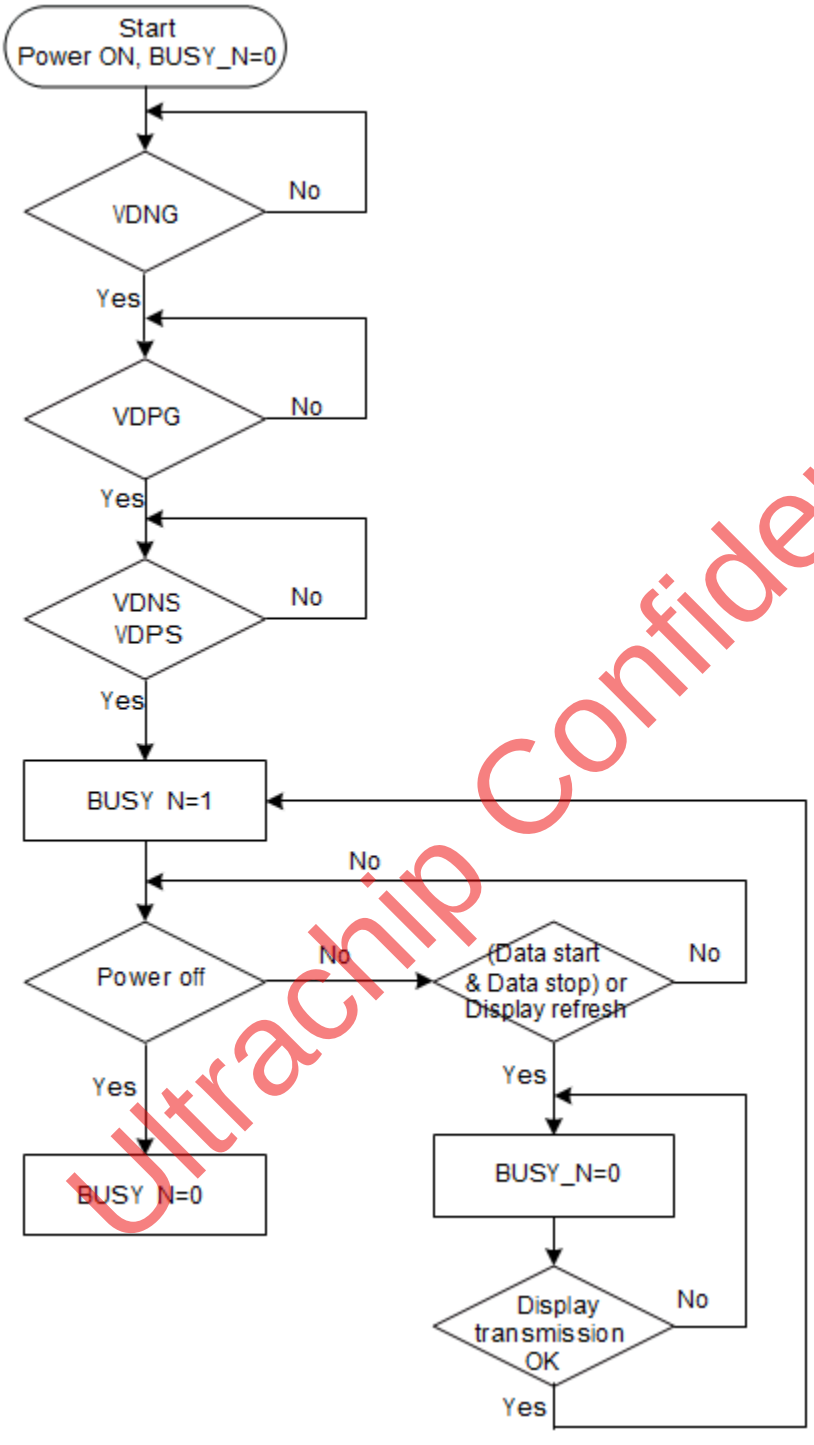
BUSY_N Signal Flow Chart



BUSY_N Signal Flow Chart

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ABSOLUTE MAXIMUM RATINGS

V_{DD}= 2~3.6V (Typ. 3.3V), GND=0V, VDH=3~9V (Typ. 6V), VDL=0~6V (Typ. 3V), T_A=0~70°C (Typ. 25°C)

Signal	Item	Min	Max.	Unit
V_{DD}, V_{IO}, $V_{DD}1$, V_{PP}	Logic Supply voltage	- 0.3	+6.0	V
V_I	Digital input range	-0.3	V_{DDIO}+40	V
V_{DPS}-V_{DNS}	Supply range	V_{DNG}-0.3	V_{DPG}+0.3	V
Source				
V_{DPS}	Analog supply voltage – positive	+20		V
V_{DNS}	Analog supply voltage -- nagetive	-20		V
Gate				
V_{DPS}	Analog supply voltage – positive	-0.3	V_{DNG}+40	V
V_{DNS}	Analog supply voltage -- nagetive	V_{DPG}-40	0.3	V
I_{VDPS}	Input rush current for V_{DPS}	(TBD)	(TBD)	mA
I_{VDNS}	Input rush current for V_{DNS}	(TBD)	(TBD)	mA
T_{STG}	Storage temperature range	-55	+125	°C

Warning:

If ICs are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

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DC CHARACTERISTICS

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
VIO	IO supply voltage		2.3	3.3	3.6	V
VDD	Supply voltage		2.3	3.3	3.6	V
VDD1	DCDC driver supply voltage	DRVU, DRVD	2.3	3.3	3.6	V
VIL	LOW Level input voltage	Digital input pins	0	--	0.3xVDD	V
VIH	HIGH Level input voltage	Digital input pins	0.7xVIO	--	VIO	V
VOH	HIGH Level output voltage	Digital input pins, IOH=400uA	VIO-0.4	--	--	V
VOHD	HIGH Level output voltage	Digital input pins, IOH=400uA, DRVD, DRVU	VDD1-0.4	--	--	V
VOL	LOW Level Output voltage	Digital input pins, IOL=-400uA	0	--	0.4	V
IIN	Input leakage current	Digital input pins except pull-up, pull-down pin	-1	--	1	uA
RIN	Pull-up/down impedance			200		KΩ
Top	Operating temperature		-30		85	°C
VDPS	Supply Voltage	For source driver/VCOM		15		V
dVDPS	Supply voltage dev		-300	0	+300	mV
VDNS	Supply Voltage	For source driver/VCOM		-15		V
dVDNS	Supply voltage dev		-300	0	+300	mV
Idd	Analog Operating Current	No load,		TBD		mA
Vvd	Voltage Deviation of Outputs		--	±20	±35	mV
Vdr	Dynamic Range of Output		0.1	--	VDPS-0.1	V
VDPG-VDNG	Voltage Range of VDPG - VDNG		12		40	V
VDNG	VDNG voltage Range	For gate driver	-20		-17	V
dVDNG	VDNG Supply voltage dev		-400	0	+400	mV
VDPG	VDPG voltage Range	For gate driver	17		VDNG+40	V
dVDPG	VDPG Supply voltage dev		-400	0	+400	mV
IOPR	Operating Current	VDD=3.3 DC/DC ON No waveform transitions No loading No RAM Read/Write		2		mA
ISLP	Sleep Current	VDD=3.3 All stopped (Power OFF mode)			1	uA

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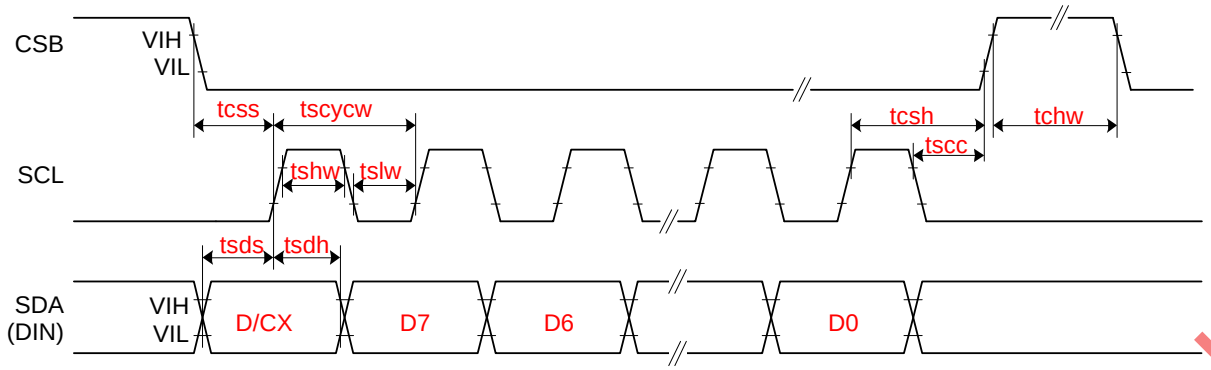
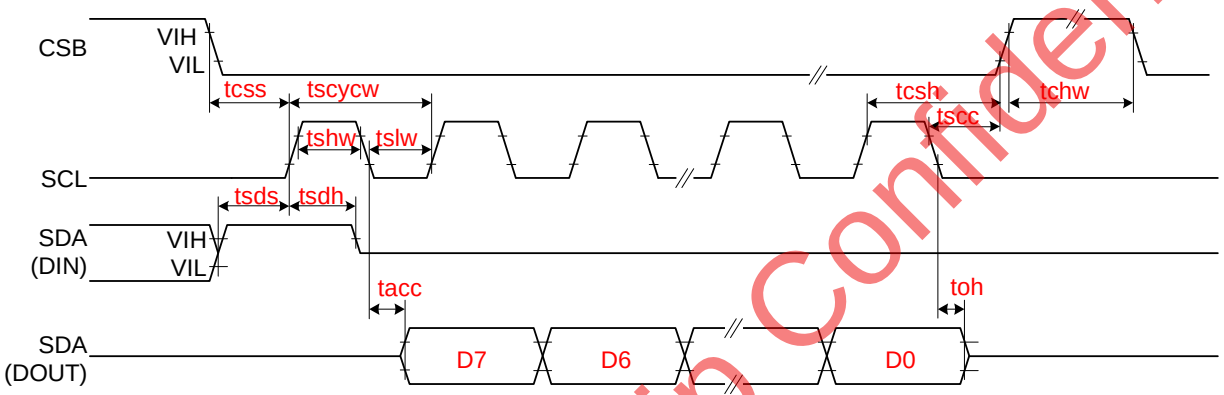
AC CHARACTERISTICS



3-wire Serial Interface – Write



3-wire Serial Interface – Read

SYMBOL	SIGNAL			MIN.	TYP.	MAX.	UNIT
SERIAL COMMUNICATION							
tCSS	CSB	Chip select setup time		60			ns
tCSH		Chip select hold time		65			ns
tSCC		Chip select setup time		20			ns
tCHW		Chip select setup time		40			ns
tSCYCW	SCL	Serial clock cycle (Write)		100			ns
tSHW		SCL “H” pulse width (Write)		35			ns
tSLW		SCL “L” pulse width (Write)		35			ns
tSCYCR		Serial clock cycle (Read)		150			ns
tSHR		SCL “H” pulse width (Read)		60			ns
tSLR		SCL “L” pulse width (Read)		60			ns
tSDS	SDA (DIN) (DOUT)	Data setup time		30			ns
tSDH		Data hold time		30			ns
tACC		Access time		10			ns
tOH		Output disable time		15			ns

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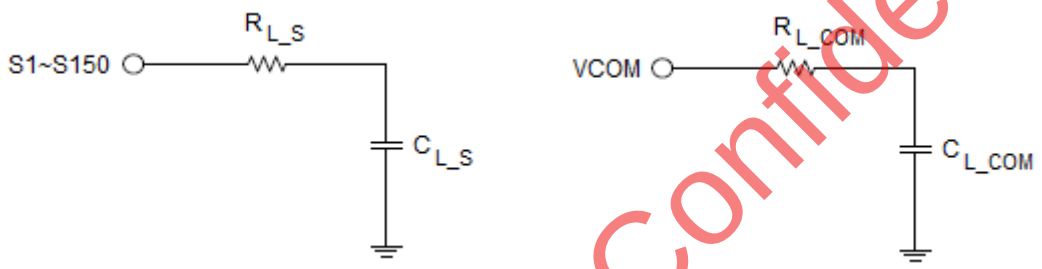
SYMBOL	SIGNAL			MIN.	TYP.	MAX.	UNIT
DRIVER							
trS		Source driver rise time	99% final value		5		us
tFS		Source driver fall time			5		us
trG		Gate driver rise time	99% final value		5		us
tFG		Gate driver fall time			5		us
trCOM		VCOM rise time	99% final value		1		ms
tFCOM		VCOM fall time			1		ms
RC LOADING							
RL_S		Source driver output loading			13.362		K Ω
CL_S					39.194		pf
RL_G		Gate driver output loading			12.329		KΩ
CL_G					32.095		pf
RL_com		VCOM output loading			61.26		Ω
CL_com					3365.7		pf



RC Loading

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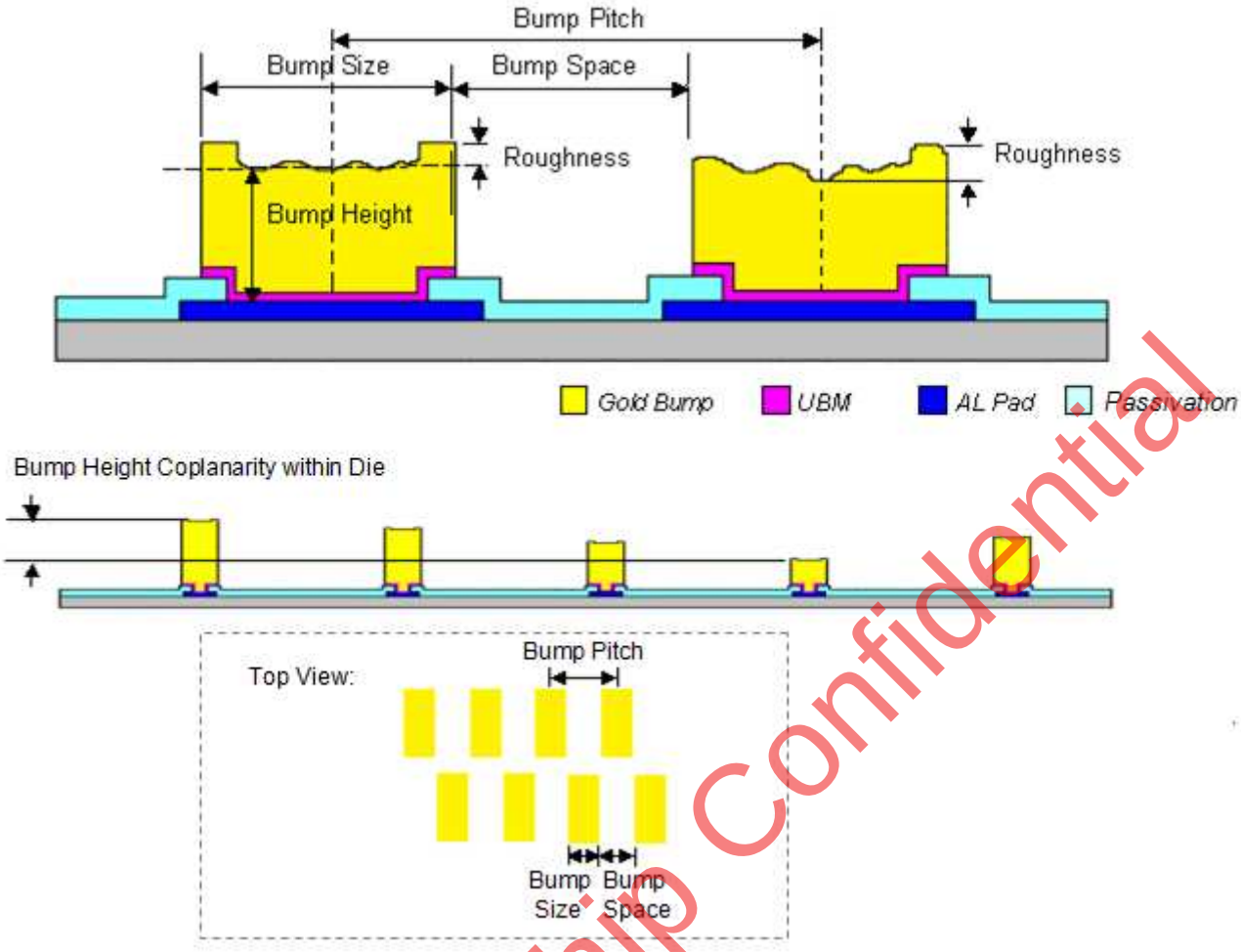
PHYSICAL DIMENSIONS



Die Size:	(13090μM ± 40μM) x (1530μM ± 40μM)
Die Thickness:	300μM ± 20μM
Die TTV:	(D_{MAX} – D_{MIN}) within die ⩽ 2μM
Bump Height:	12 μM ± 3μM
	(H_{MAX} – H_{MIN}) within die ⩽ 2μM
Hardness:	65Hv ± 15Hv
Bump Size:	18μM x 75μM ± 2μM
Bump Pitch:	42μM
Bump Gap:	24μM ± 3μM
Bump Area:	1350μM^2
Total Bump Area:	114300μM^2
Area Ratio:	1.761 : 1 (Output pad : Input pad)
	1 : 1 (Side power pad)
Coordinate origin:	Chip center
Pad reference:	Pad center

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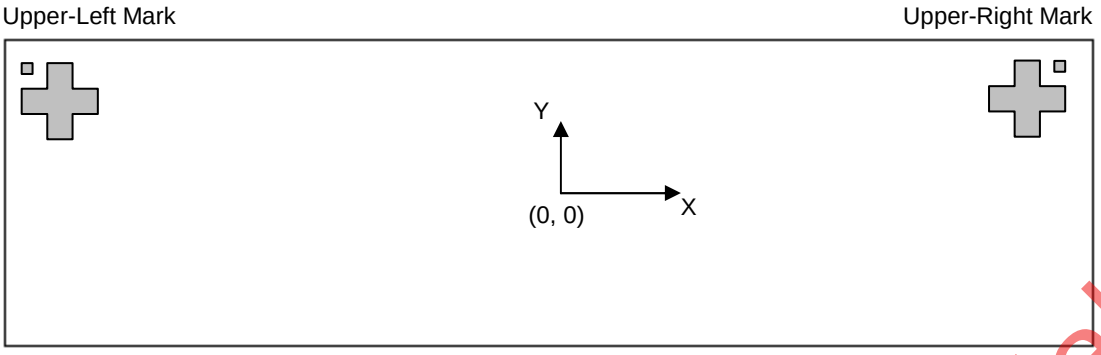
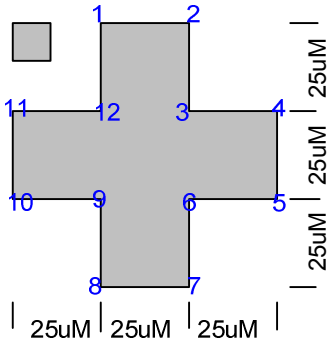
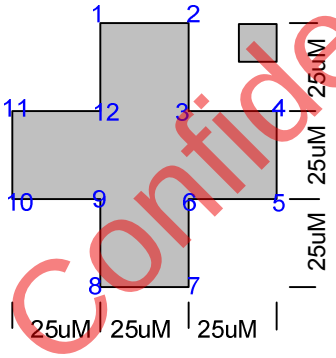
ALIGNMENT MARK INFORMATION

Location:



Shapes and Points:





Point Coordinates:

Point	Upper-Left Mark		Upper-Right Mark	
	X	Y	X	Y
Center	-6382	642	6382	642
1	-6394.5	679.5	6369.5	679.5
2	-6369.5	679.5	6394.5	679.5
3	-6369.5	654.5	6394.5	654.5
4	-6344.5	654.5	6419.5	654.5
5	-6344.5	629.5	6419.5	629.5
6	-6369.5	629.5	6394.5	629.5
7	-6369.5	604.5	6394.5	604.5
8	-6394.5	604.5	6369.5	604.5
9	-6394.5	629.5	6369.5	629.5
10	-6419.5	629.5	6344.5	629.5
11	-6419.5	654.5	6344.5	654.5
12	-6394.5	654.5	6369.5	654.5

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PAD COORDINATES

No.	Name	X	Y	W	H
1	NC	-6180	-680	40	50
2	VCOM	-6120	-680	40	50
3	VCOM	-6060	-680	40	50
4	VCOM	-6000	-680	40	50
5	VCOM	-5940	-680	40	50
6	VCOM	-5880	-680	40	50
7	VCOM	-5820	-680	40	50
8	VCOM	-5760	-680	40	50
9	VCOM	-5700	-680	40	50
10	VDM	-5640	-680	40	50
11	VGL	-5580	-680	40	50
12	VGL	-5520	-680	40	50
13	VGL	-5460	-680	40	50
14	VGL	-5400	-680	40	50
15	VGL	-5340	-680	40	50
16	VGL	-5280	-680	40	50
17	VGL	-5220	-680	40	50
18	VGL	-5160	-680	40	50
19	VGL	-5100	-680	40	50
20	VGL	-5040	-680	40	50
21	VGL	-4980	-680	40	50
22	VGL	-4920	-680	40	50
23	VGL	-4860	-680	40	50
24	VGL	-4800	-680	40	50
25	VGL	-4740	-680	40	50
26	VGL	-4680	-680	40	50
27	GNDA	-4620	-680	40	50
28	VSL	-4560	-680	40	50
29	VSL	-4500	-680	40	50
30	VSL	-4440	-680	40	50
31	VSL	-4380	-680	40	50
32	VSL	-4320	-680	40	50
33	VSL	-4260	-680	40	50
34	VSL	-4200	-680	40	50
35	VSL	-4140	-680	40	50
36	VSL	-4080	-680	40	50
37	VSL	-4020	-680	40	50
38	GNDA	-3960	-680	40	50
39	VGH	-3900	-680	40	50
40	VGH	-3840	-680	40	50
42	VGH	-3780	-680	40	50
41	VGH	-3720	-680	40	50
43	VGH	-3660	-680	40	50
44	VGH	-3600	-680	40	50
45	VGH	-3540	-680	40	50
46	VGH	-3480	-680	40	50
47	VGH	-3420	-680	40	50
48	VGH	-3360	-680	40	50
49	VGH	-3300	-680	40	50
50	VGH	-3240	-680	40	50
51	GNDA	-3180	-680	40	50
52	VSH	-3120	-680	40	50
53	VSH	-3060	-680	40	50
54	VSH	-3000	-680	40	50
55	VSH	-2940	-680	40	50
56	VSH	-2880	-680	40	50
57	VSH	-2820	-680	40	50
58	VSH	-2760	-680	40	50

No.	Name	X	Y	W	H
59	VSH	-2700	-680	40	50
60	VSH	-2640	-680	40	50
61	VSH	-2580	-680	40	50
62	GNDA	-2520	-680	40	50
63	DUMMY	-2460	-680	40	50
64	DUMMY	-2400	-680	40	50
65	DUMMY	-2340	-680	40	50
66	DUMMY	-2280	-680	40	50
67	DUMMY	-2220	-680	40	50
68	DUMMY	-2160	-680	40	50
69	DUMMY	-2100	-680	40	50
70	DUMMY	-2040	-680	40	50
71	DUMMY	-1980	-680	40	50
72	DUMMY	-1920	-680	40	50
73	DUMMY	-1860	-680	40	50
74	DUMMY	-1800	-680	40	50
75	DUMMY	-1740	-680	40	50
76	DUMMY	-1680	-680	40	50
77	DUMMY	-1620	-680	40	50
78	DUMMY	-1560	-680	40	50
79	GND	-1500	-680	40	50
80	VDM	-1440	-680	40	50
81	VDM	-1380	-680	40	50
82	GND	-1320	-680	40	50
83	GND	-1260	-680	40	50
84	GND	-1200	-680	40	50
85	GND	-1140	-680	40	50
86	GND	-1080	-680	40	50
87	GND	-1020	-680	40	50
88	GND	-960	-680	40	50
89	GND	-900	-680	40	50
90	GND	-840	-680	40	50
91	GND	-780	-680	40	50
92	GND	-720	-680	40	50
93	GNDA	-660	-680	40	50
94	GNDA	-600	-680	40	50
95	GNDA	-540	-680	40	50
96	GNDA	-480	-680	40	50
97	GNDA	-420	-680	40	50
98	GNDA	-360	-680	40	50
99	GNDA	-300	-680	40	50
100	GNDA	-240	-680	40	50
101	GNDA	-180	-680	40	50
102	GNDA	-120	-680	40	50
103	VDDA	-60	-680	40	50
104	VDDA	0	-680	40	50
105	VDDA	60	-680	40	50
106	VDDA	120	-680	40	50
107	VDDA	180	-680	40	50
108	VDDA	240	-680	40	50
109	VDDA	300	-680	40	50
110	VDDA	360	-680	40	50
111	VDDA	420	-680	40	50
112	VDDA	480	-680	40	50
113	VDD	540	-680	40	50
114	VDD	600	-680	40	50
115	VDD	660	-680	40	50
116	VDD	720	-680	40	50

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No.	Name	X	Y	W	H
117	VDD	780	-680	40	50
118	VDD	840	-680	40	50
119	VDD	900	-680	40	50
120	TEST1	960	-680	40	50
121	TEST2	1020	-680	40	50
122	VDDIO	1080	-680	40	50
123	VDDIO	1140	-680	40	50
124	VDDIO	1200	-680	40	50
125	VDDIO	1260	-680	40	50
126	TEST3	1320	-680	40	50
127	DUMMY	1380	-680	40	50
128	DUMMY	1440	-680	40	50
129	DUMMY	1500	-680	40	50
130	DUMMY	1560	-680	40	50
131	DUMMY	1620	-680	40	50
132	SDA	1680	-680	40	50
133	SCL	1740	-680	40	50
134	GND	1800	-680	40	50
135	CSB	1860	-680	40	50
136	VDDIO	1920	-680	40	50
137	DUMMY	1980	-680	40	50
138	GND	2040	-680	40	50
139	DC	2100	-680	40	50
140	VDDIO	2160	-680	40	50
141	DUMMY	2220	-680	40	50
142	GND	2280	-680	40	50
143	RST_N	2340	-680	40	50
144	BUSY_N	2400	-680	40	50
145	CL	2460	-680	40	50
146	VDDIO	2520	-680	40	50
147	VSYNC	2580	-680	40	50
148	GND	2640	-680	40	50
149	DUMMY	2700	-680	40	50
150	VDDIO	2760	-680	40	50
151	BS	2820	-680	40	50
152	GND	2880	-680	40	50
153	DUMMY	2940	-680	40	50
154	VDDIO	3000	-680	40	50
155	DUMMY	3060	-680	40	50
156	GND	3120	-680	40	50
157	MS	3180	-680	40	50
158	VDDIO	3240	-680	40	50
159	TSDA	3300	-680	40	50
160	TSDA	3360	-680	40	50
161	TSCL	3420	-680	40	50
162	TSCL	3480	-680	40	50
163	TEST4	3540	-680	40	50
164	TEST5	3600	-680	40	50
165	TEST6	3660	-680	40	50
166	TEST7	3720	-680	40	50
167	VGH	3780	-680	40	50
168	VGH	3840	-680	40	50
169	VGH	3900	-680	40	50
170	VGH	3960	-680	40	50
171	VGH	4020	-680	40	50
172	VGH	4080	-680	40	50
173	VGH	4140	-680	40	50
174	VGH	4200	-680	40	50
175	VGL	4260	-680	40	50
176	VGL	4320	-680	40	50

No.	Name	X	Y	W	H
177	VGL	4380	-680	40	50
178	VGL	4440	-680	40	50
179	VGL	4500	-680	40	50
180	VGL	4560	-680	40	50
181	VGL	4620	-680	40	50
182	VGL	4680	-680	40	50
183	GNDA	4740	-680	40	50
184	FB	4800	-680	40	50
185	FB	4860	-680	40	50
186	GNDA	4920	-680	40	50
187	RESE	4980	-680	40	50
188	RESE	5040	-680	40	50
189	GNDA	5100	-680	40	50
190	GDR	5160	-680	40	50
191	GDR	5220	-680	40	50
192	GDR	5280	-680	40	50
193	GDR	5340	-680	40	50
194	GDR	5400	-680	40	50
195	GDR	5460	-680	40	50
196	GDR	5520	-680	40	50
197	GDR	5580	-680	40	50
198	VDM	5640	-680	40	50
199	VCOM	5700	-680	40	50
200	VCOM	5760	-680	40	50
201	VCOM	5820	-680	40	50
202	VCOM	5880	-680	40	50
203	VCOM	5940	-680	40	50
204	VCOM	6000	-680	40	50
205	VCOM	6060	-680	40	50
206	VCOM	6120	-680	40	50
207	NC	6180	-680	40	50
208	NC	6170	561.5	18	75
209	NC	6149	681.5	18	75
210	NC	6128	561.5	18	75
211	NC	6107	681.5	18	75
212	NC	6086	561.5	18	75
213	NC	6065	681.5	18	75
214	G<0>	6044	561.5	18	75
215	G<2>	6023	681.5	18	75
216	G<4>	6002	561.5	18	75
217	G<6>	5981	681.5	18	75
218	G<8>	5960	561.5	18	75
219	G<10>	5939	681.5	18	75
220	G<12>	5918	561.5	18	75
221	G<14>	5897	681.5	18	75
222	G<16>	5876	561.5	18	75
223	G<18>	5855	681.5	18	75
224	G<20>	5834	561.5	18	75
225	G<22>	5813	681.5	18	75
226	G<24>	5792	561.5	18	75
227	G<26>	5771	681.5	18	75
228	G<28>	5750	561.5	18	75
229	G<30>	5729	681.5	18	75
230	G<32>	5708	561.5	18	75
231	G<34>	5687	681.5	18	75
232	G<36>	5666	561.5	18	75
233	G<38>	5645	681.5	18	75
234	G<40>	5624	561.5	18	75
235	G<42>	5603	681.5	18	75
236	G<44>	5582	561.5	18	75

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No.	Name	X	Y	W	H
237	G<46>	5561	681.5	18	75
238	G<48>	5540	561.5	18	75
239	G<50>	5519	681.5	18	75
240	G<52>	5498	561.5	18	75
241	G<54>	5477	681.5	18	75
242	G<56>	5456	561.5	18	75
243	G<58>	5435	681.5	18	75
244	G<60>	5414	561.5	18	75
245	G<62>	5393	681.5	18	75
246	G<64>	5372	561.5	18	75
247	G<66>	5351	681.5	18	75
248	G<68>	5330	561.5	18	75
249	G<70>	5309	681.5	18	75
250	G<72>	5288	561.5	18	75
251	G<74>	5267	681.5	18	75
252	G<76>	5246	561.5	18	75
253	G<78>	5225	681.5	18	75
254	G<80>	5204	561.5	18	75
255	G<82>	5183	681.5	18	75
256	G<84>	5162	561.5	18	75
257	G<86>	5141	681.5	18	75
258	G<88>	5120	561.5	18	75
259	G<90>	5099	681.5	18	75
260	G<92>	5078	561.5	18	75
261	G<94>	5057	681.5	18	75
262	G<96>	5036	561.5	18	75
263	G<98>	5015	681.5	18	75
264	G<100>	4994	561.5	18	75
265	G<102>	4973	681.5	18	75
266	G<104>	4952	561.5	18	75
267	G<106>	4931	681.5	18	75
268	G<108>	4910	561.5	18	75
269	G<110>	4889	681.5	18	75
270	G<112>	4868	561.5	18	75
271	G<114>	4847	681.5	18	75
272	G<116>	4826	561.5	18	75
273	G<118>	4805	681.5	18	75
274	G<120>	4784	561.5	18	75
275	G<122>	4763	681.5	18	75
276	G<124>	4742	561.5	18	75
277	G<126>	4721	681.5	18	75
278	G<128>	4700	561.5	18	75
279	G<130>	4679	681.5	18	75
280	G<132>	4658	561.5	18	75
281	G<134>	4637	681.5	18	75
282	G<136>	4616	561.5	18	75
283	G<138>	4595	681.5	18	75
284	G<140>	4574	561.5	18	75
285	G<142>	4553	681.5	18	75
286	G<144>	4532	561.5	18	75
287	G<146>	4511	681.5	18	75
288	G<148>	4490	561.5	18	75
289	G<150>	4469	681.5	18	75
290	G<152>	4448	561.5	18	75
291	G<154>	4427	681.5	18	75
292	G<156>	4406	561.5	18	75
293	G<158>	4385	681.5	18	75
294	G<160>	4364	561.5	18	75
295	G<162>	4343	681.5	18	75
296	G<164>	4322	561.5	18	75

No.	Name	X	Y	W	H
297	G<166>	4301	681.5	18	75
298	G<168>	4280	561.5	18	75
299	G<170>	4259	681.5	18	75
300	G<172>	4238	561.5	18	75
301	G<174>	4217	681.5	18	75
302	G<176>	4196	561.5	18	75
303	G<178>	4175	681.5	18	75
304	G<180>	4154	561.5	18	75
305	G<182>	4133	681.5	18	75
306	G<184>	4112	561.5	18	75
307	G<186>	4091	681.5	18	75
308	G<188>	4070	561.5	18	75
309	G<190>	4049	681.5	18	75
310	G<192>	4028	561.5	18	75
311	G<194>	4007	681.5	18	75
312	G<196>	3986	561.5	18	75
313	G<198>	3965	681.5	18	75
314	G<200>	3944	561.5	18	75
315	G<202>	3923	681.5	18	75
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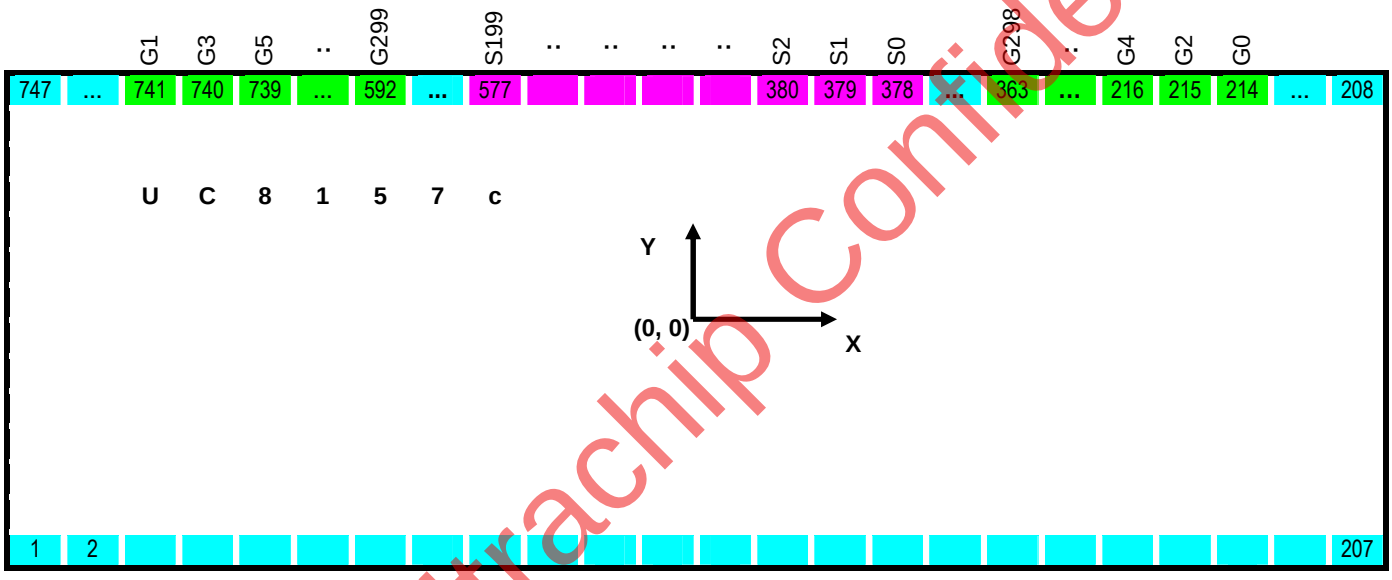
730	G<23>	-5813	561.5	18	75
731	G<21>	-5834	681.5	18	75
732	G<19>	-5855	561.5	18	75

No.	Name	X	Y	W	H
733	G<17>	-5876	681.5	18	75
734	G<15>	-5897	561.5	18	75
735	G<13>	-5918	681.5	18	75
736	G<11>	-5939	561.5	18	75
737	G<9>	-5960	681.5	18	75
738	G<7>	-5981	561.5	18	75
739	G<5>	-6002	681.5	18	75
740	G<3>	-6023	561.5	18	75
741	G<1>	-6044	681.5	18	75
742	NC	-6065	561.5	18	75
743	NC	-6086	681.5	18	75
744	NC	-6107	561.5	18	75
745	NC	-6128	681.5	18	75
746	NC	-6149	561.5	18	75
747	NC	-6170	681.5	18	75



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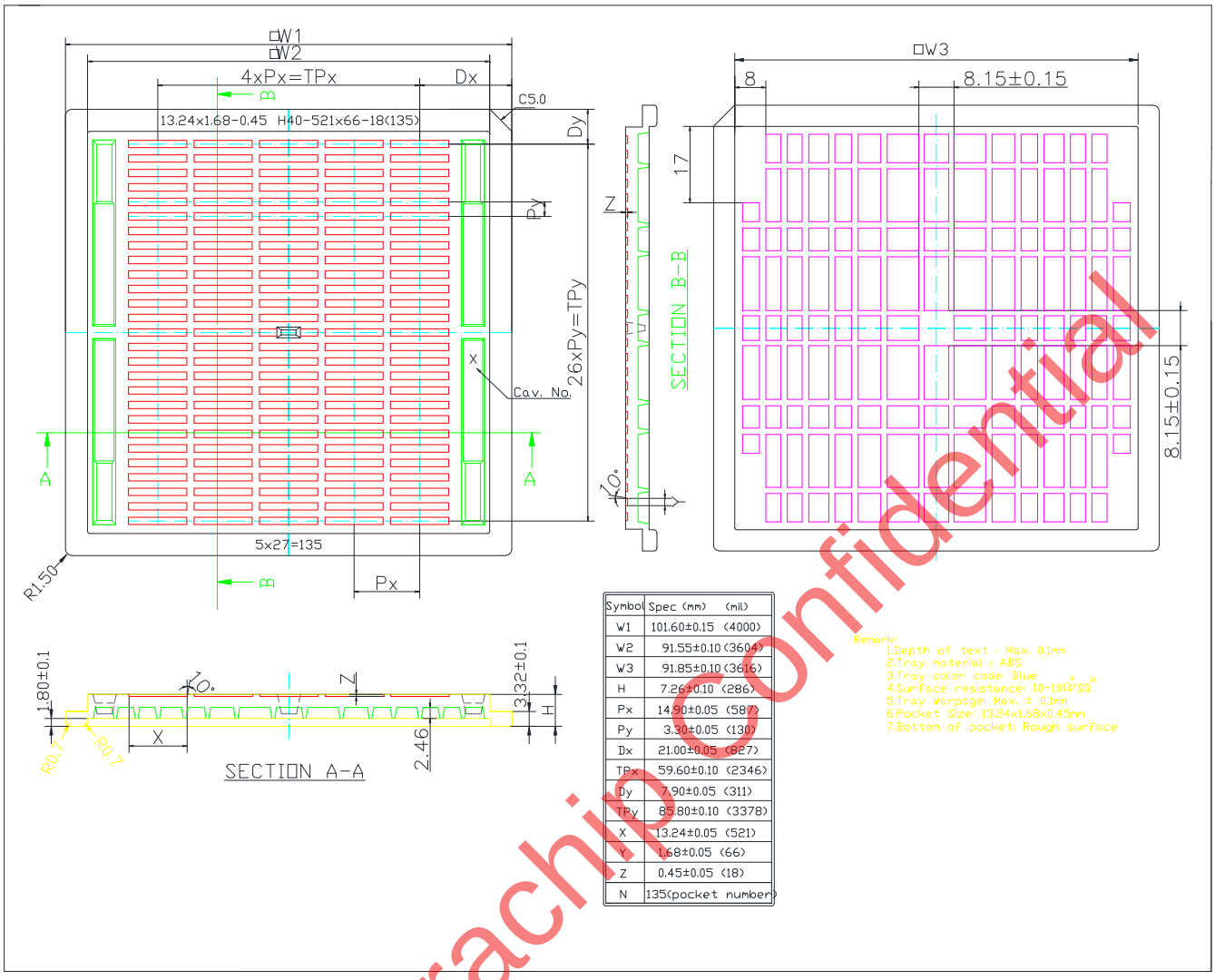
TRAY INFORMATION



Symbol	Spec (mm) (mil)
W1	101.60±0.15 (4000)
W2	91.55±0.10 (3604)
W3	91.85±0.10 (3616)
H	7.26±0.10 (286)
Px	14.90±0.05 (587)
Py	3.30±0.05 (130)
Dx	21.00±0.05 (827)
TPx	59.60±0.10 (2346)
Dy	7.90±0.05 (311)
TPy	85.80±0.10 (3378)
X	13.24±0.05 (521)
Y	1.68±0.05 (66)
Z	0.45±0.05 (18)
N	135(pocket number)

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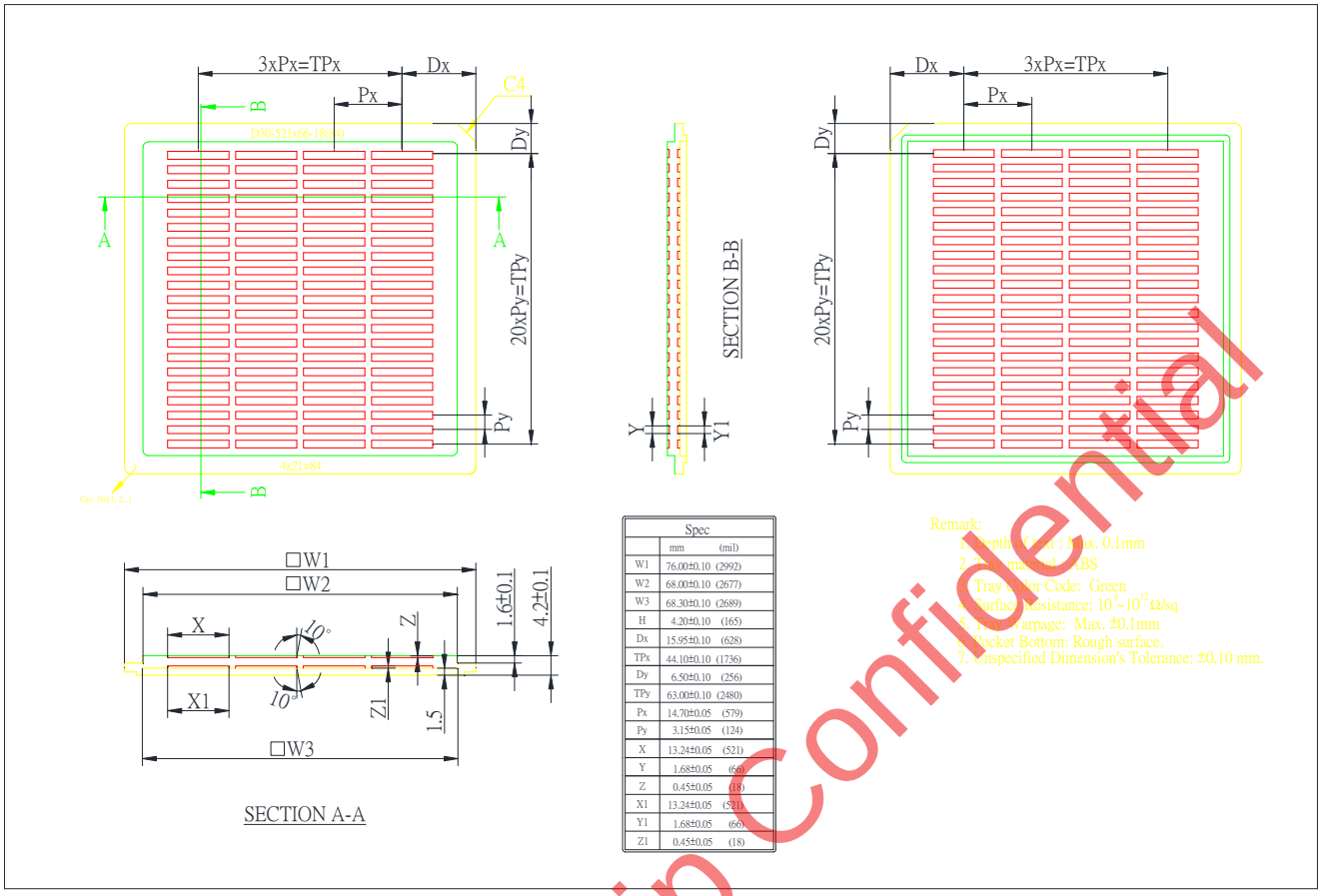
3-inch-Tray Drawing



Spec		
	mm	(mil)
W1	76.00±0.10	(2992)
W2	68.00±0.10	(2677)
W3	68.30±0.10	(2689)
H	4.20±0.10	(165)
Dx	15.95±0.10	(628)
TPx	44.10±0.10	(1736)
Dy	6.50±0.10	(256)
TPy	63.00±0.10	(2480)
Px	14.70±0.05	(579)
Py	3.15±0.05	(124)
X	13.24±0.05	(521)
Y	1.68±0.05	(66)
Z	0.45±0.05	(18)
X1	13.24±0.05	(521)
Y1	1.68±0.05	(66)
Z1	0.45±0.05	(18)

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REVISION HISTORY

Revision	Contents	Date
0.6	First Release	Feb. 5, 2014

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