

HIGH-VOLTAGE MIXED-SIGNAL IC

UC8159

All-in-one driver IC w/ Timing Controller for
Color Application

Preliminary Specifications
Datasheet Revision: 0.5 (for EIH only)

IC Version: c_B
July 7, 2016

ULTRACHIP

The Coolest EPD Driver, Ever!

Specifications and information herein are subject to change without notice.

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UC8159

All-in-one driver IC with Timing Controller for Color Application

INTRODUCTION

The UC8159 is an all-in-one gate source driver with an integrated timing controller for ESL application. The source is capable of 3-bit outputs per pixel to support white/black/color. The timing controller provides control signals for the source driver and gate drivers.

The integrated DC-DC converter generates all the necessary source and gate output voltages for VSH_LV/VSL_LV (+/-3V ~ +/-15V), VSH/VSL(+/-15V) and VGH/VGL (+/-17V ~ +/-20V). The chip also includes an output buffer for the supply of the common electrode (VCOMAC or VCOMDC). The system is configurable through a 3-wire/4-wire (SPI) serial.

MAIN APPLICATIONS

- E-tag application

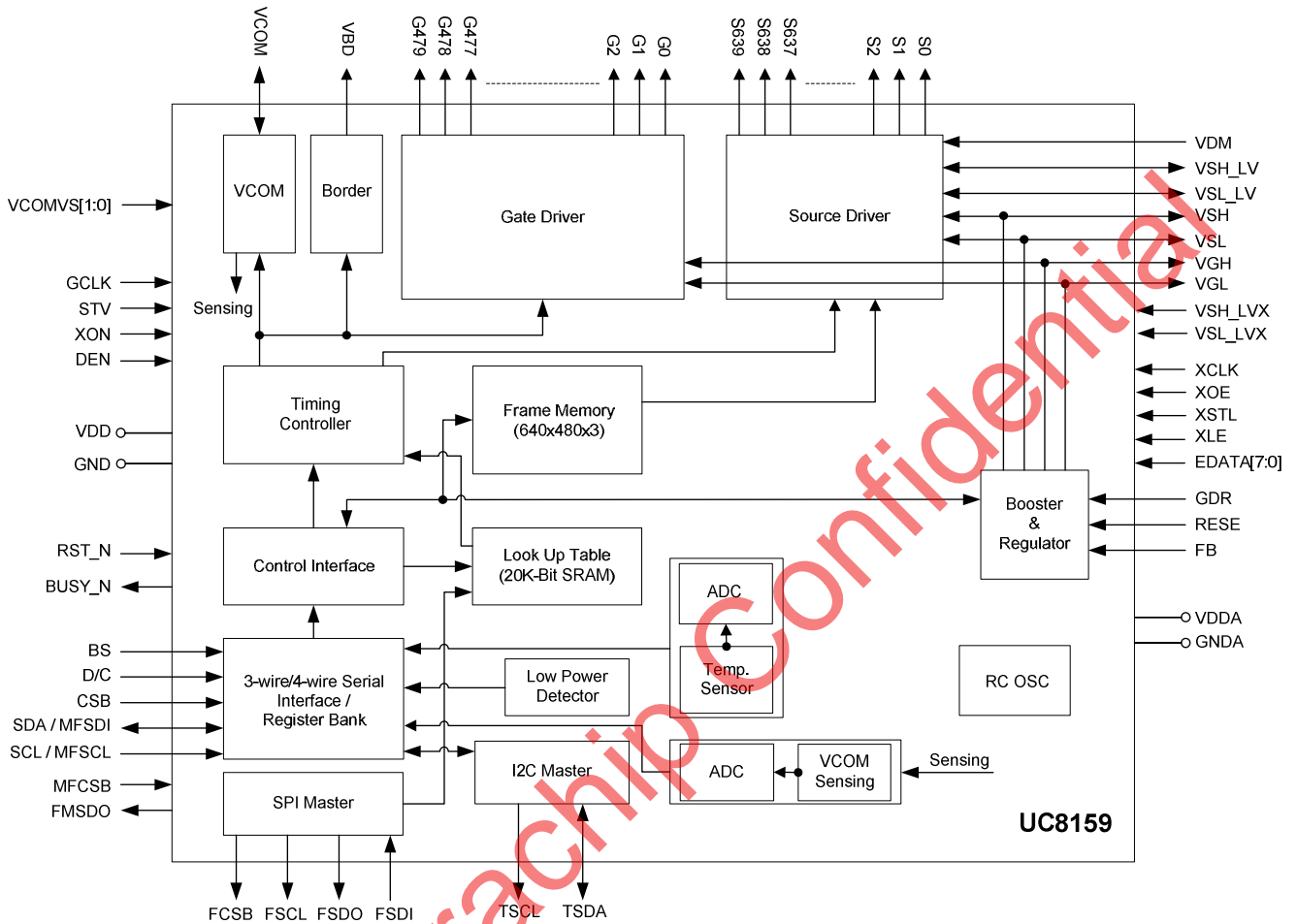
FEATURE HIGHLIGHTS

- System-on-chip (SOC) for ESL, including:
- Timing controller support of several resolutions
- Preselect res (640x480, 600x450, 640x448, 600x448)
- Built in Frame memory maximum (640x480x3bit)
- Support LUT (VCOM, LUT0~LUT7, XON)
- 640 outputs source driver with 3-bit white/black/red resolution

- Output dynamic voltage : VSH, VSH_LV, VSH_LVX, 0, VSL_LVX, VSL_LV, VSL
- Output deviation: 0.2V
- 640 channels outputs
- Left and Right shift capability
- 480 outputs gate driver:
 - 480 channels outputs
 - Up and Down shift capability
 - Output voltage VDN+40
- 3-wire/4-wire (SPI) serial interface for system configuration
- DC-DC controller for generating the analog power supply
- Common electrode (VCOM AC or VCOM DC) level
- External SPI flash/EEPROM for WF
- Built-in temperature sensor
- Support I²C interface for external temperature sensor
- Support low power detection
- Digital supply voltage: 2.3~ 3.6V
- Support frame rate: 200 Hz (max)
- Support pure source & gate driver function
- COG Package

Remark: Contact UltraChip for a visual inspection document (03-DOC-093).

BLOCK DIAGRAM



ORDERING INFORMATION

| Part Number | I ² C | Description |
|-------------------|------------------|--------------------------------------|
| UC8159cGAB-M0P1-4 | No | with 4" Tray, Wafer Thickness: 180uM |

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

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PIN DESCRIPTION

Type: C: Capacitor pin, I: Input, I/O: Input/Output, M: Mark, O: Output,
 PWR: Power, PI: Power Input, PO: Power Output, PS: Power Setting, S: Shorted line

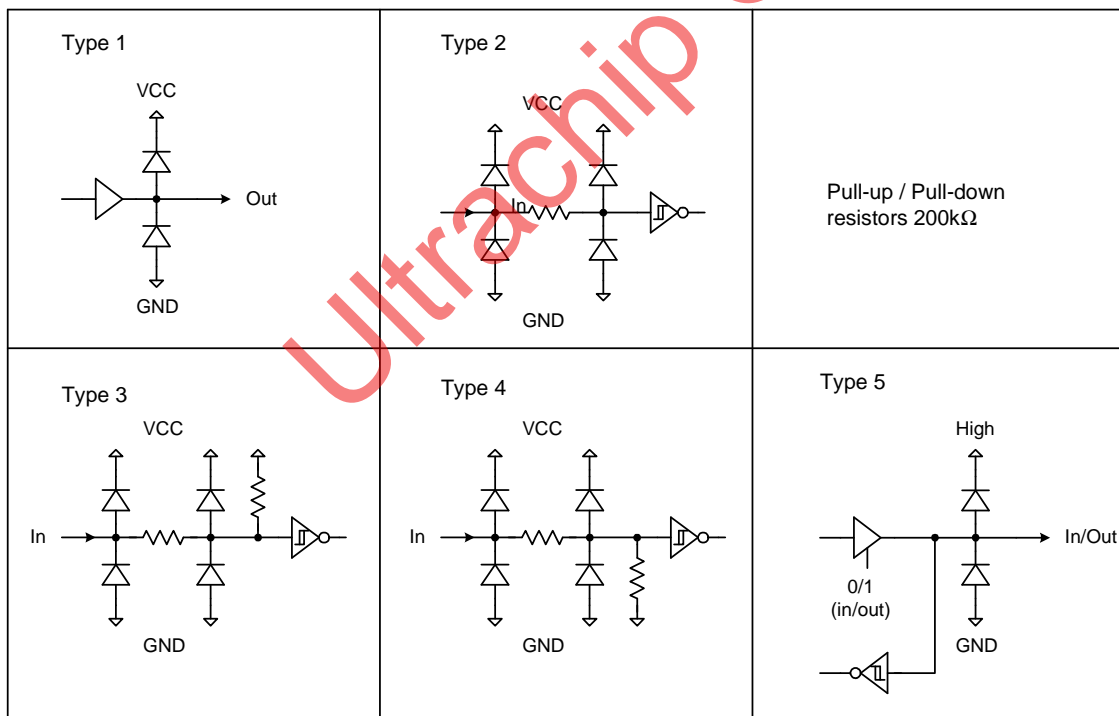
| Pin (Pad) Name | Pin Count | Type | Description |
|-----------------------------|-----------|---------------------------------|---|
| SERIAL INTERFACE | | | |
| CSB | 1 | I, Type2 | Serial communication chip select. |
| SDA / MFSDI* | 1 | I/O, Type5 | Serial communication data input. It would bypass to MFSDI by R65H command. |
| SCL / MFSCCL* | 1 | I, Type2 | Serial communication clock input. It would bypass to MFSCCL by R65H command. |
| D/C (DC) | 1 | I, Type2 | Serial communication command/parameter input. L: command H: parameter |
| FMSDO* | 1 | O, Type1 | Serial communication data output. It would bypass to FMSDO by R65H command. |
| MFCBSB* | 1 | I, Type2 | Serial communication chip select. It would bypass to MFCBSB by R65H command. |
| FCSB | 1 | O, Type1 | Serial communication chip select for External Flash/EEPROM. |
| FSCL | 1 | O, Type1 | Serial communication clock output for External Flash/EEPROM. |
| FSDI | 1 | I, Type4 (Pull-down) | Serial communication data input for External Flash/EEPROM. |
| FSDO | 1 | O, Type1 | Serial communication data output for External Flash/EEPROM. |
| CONTROL INTERFACE | | | |
| BS | 1 | I, Type2 | Input interface setting. Select 3 wire/ 4 wire SPI interface L: 4-wire IF H: 3-wire IF |
| RST_N | 1 | I, Type3 (Pull-up), Type3 | Global reset pin. Low reset. When RST_N become low, driver will reset. All register will reset to default value. All driver functions will be disabled. SD output and VCOM will remain previous condition. It may have two conditions: 0v or floating. |
| BUSY_N | 1 | O, Type1 | This pin indicates the driver status. L: Driver is busy, data/VCOM is transforming. H: non-busy. Host side can send command/data to driver. |
| TSCL | 2 | O | I ² C clock for external temperature sensor. (A pull-up resistor is necessary). |
| TSDA | 2 | I/O | I ² C data for external temperature sensor. (A pull-up resistor is necessary). |
| SOURCE / GATE DRIVER | | | |
| S[0..639] | 640 | O | Source driver output signals. |
| G[0..479] | 480 | O | Gate driver output signals. |
| VBD (VBD<0>~<1>) | 2 | O | Border output pin. |

| Pin (Pad) Name | Pin Count | Type | Description |
|------------------------------|-----------|----------|--|
| VCOM | 16 | O | VCOM output. VCOM has four voltage states: 1. (VSH+VCM_DC) V 2. (VCM_DC) V 3. (VSL+VCM_DC) V 4. Floating |
| POWER CIRCUIT | | | |
| GDR | 6 | O | This pin is N-MOS gate control. |
| RESE | 2 | PWR | Current sense input for control loop. |
| FB | 2 | PWR | Keep open |
| VGH | 20 | C | Positive gate voltage |
| VGL | 23 | C | Negative gate voltage |
| VSH | 10 | C | Positive source voltage (+15V) |
| VSL | 10 | C | Negative source voltage (-15V) |
| VSH_LV | 10 | C | Positive source voltage (+3.0V ~ +15.0V). |
| VSL_LV | 10 | C | Negative source voltage (-3.0V ~ -15.0V). |
| VSH_LVX | 8 | C | Positive source voltage (external mode only) (+3.0V ~ +15.0V). |
| VSL_LVX | 8 | C | Negative source voltage (external mode only) (-3.0V ~ -15.0V). |
| PURE DRIVER INTERFACE | | | |
| DEN | 1 | I, Type2 | Pure driver mode pin. L: Disable pure driver mode. H: Enable pure driver mode. |
| XCLK | 1 | I, Type2 | Source driver clock input. Data inputs are captured on the rising edge of clock signal. |
| XOE | 1 | I, Type2 | Source driver outputs enabled when OE is logic "H", Outputs forced to GND when OE is logic "L". It is asynchronous to clock CLK. |
| XSTL | 1 | I, Type2 | Source driver data shift start pulse |
| XLE | 1 | I, Type2 | Source driver parallel latch enable, transparent when high. It is asynchronous to clock CLK |
| EDATA[7:0] | 8 | I, Type2 | Source driver 8-bit data |
| GCLK | 1 | I, Type2 | Gate driver shift clock pin. The shift register data are shifted synchronously with each rising edge of GCLK. |
| STV | 1 | I, Type2 | Gate driver start pulse |
| XON | 1 | I, Type2 | Driver XON pin. 0: Force all gate ON (VGH) 1: Normal gate function |
| VCOMVS[1:0] VCOMVS<0>~<1> | 2 | I, Type2 | VCOM voltage selection 00b: VCM_DC 01b: VDPS+VCM_DC 10b: VDNS+VCM_DC 11b: floating |

| Pin (Pad) Name | Pin Count | Type | Description |
|---------------------|-----------|------|---|
| POWER SUPPLY | | | |
| VDD | 12 | PWR | Digital voltage supply (2.3V ~ 3.6V) |
| VDDA | 12 | PWR | Analog voltage supply (2.3V ~ 3.6V) |
| VDDD | 6 | PWR | Voltage input (1.8V) |
| VDDDO | 6 | PWR | Voltage output (1.8V) |
| VDDIO | 8 | PWR | I/O voltage supply (2.3V ~ 3.6V) |
| VDM | 6 | PWR | Driver ground |
| VPPM | 6 | | Connect to GND. |
| TEST1~15 | 15 | | Test pins for Ultrachip only, Leave it Float. |
| TESTVDD | 1 | | Test pin for Ultrachip only, Connect to VSS. |
| DUMMY | 13 | | Dummy pins |
| FSOURCE | 3 | PWR | Leave it float. |
| GND | 25 | PWR | Digital ground. |
| GND A | 22 | PWR | Analog ground. |
| PATH1 | 2 | S | Internally linked together. |

Remark:

- (1) Pull-up / Pull-down resistors 200KΩ
- (2) I/O Pin Structure:



COMMAND TABLE

W/R: 0: Write Cycle 1: Read Cycle **C/D**: 0: Command / 1: Data **D7~D0**: -: Don't Care #: Valid Data

| # | Command | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Registers | Default | |
|----|--|-----|-----|----|----|----|----|----|----|----|-----|--|----------------------------|-----|
| 1 | Panel Setting (PSR) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 00h | |
| | | 0 | 1 | # | # | -- | -- | # | # | # | # | RES[1:0], UD, SHL, SHD_N, RST_N | 07h | |
| | | 0 | 1 | -- | -- | -- | -- | -- | -- | -- | -- | | 00h | |
| 2 | Power Setting (PWR) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | 01h | |
| | | 0 | 1 | -- | -- | # | # | # | # | # | # | EDATA_SEL, EDATA_SET, VCM_HZ, VS_EN, VSC_EN, VG_EN | 08h | |
| | | 0 | 1 | -- | -- | -- | -- | -- | -- | # | # | VGHL_LV[1:0] | 01h | |
| | | 0 | 1 | -- | -- | # | # | # | # | # | # | VSHC_LVL[5:0] | 05h | |
| | | 0 | 1 | -- | -- | # | # | # | # | # | # | VSLC_LVL[5:0] | 05h | |
| 3 | Power OFF (POF) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | | 02h | |
| 4 | Power OFF Sequence Setting (PFS) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | | 03h | |
| | | 0 | 1 | -- | -- | # | # | -- | -- | -- | -- | T_VDS_OFF[1:0] | 00h | |
| 5 | Power ON (PON) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | | 04h | |
| 6 | Booster Soft Start (BTST) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | | 06h | |
| | | 0 | 1 | # | # | # | # | # | # | # | # | BT_PHA[7:0] | 17h | |
| | | 0 | 1 | # | # | # | # | # | # | # | # | BT_PHB[7:0] | 17h | |
| | | 0 | 1 | -- | -- | # | # | # | # | # | # | BT_PHC[5:0] | 17h | |
| 7 | Deep Sleep (DSLPL) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | | 07h | |
| | | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | Check code | A5h | |
| 8 | Data Start Transmission 1 (DTM1) (x-byte command) | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | | 10h | |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | KPixel1[2:0], KPixel2[2:0] | 00h | |
| | | 0 | 1 | : | : | : | : | : | : | : | : | : | : | : |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | Kpixel[2M-1][2:0], Kpixel[2M][2:0] | 00h | |
| 9 | Data Stop (DSP) | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | | 11h | |
| | | 1 | 1 | # | -- | -- | -- | -- | -- | -- | -- | Data_flag | -- | |
| 10 | Display Refresh (DRF) | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | | 12h | |
| 11 | Image Process Command (IPC) | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | | 13h | |
| | | 0 | 1 | -- | -- | -- | # | -- | # | # | # | IP_EN, IP_SEL[2:0] | 00h | |
| 12 | VCOM LUT (LUTC) (221-byte command, bytes 2~12 repeated 20 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | | 20h | |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | Phase repeat times [7:0] | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 1stLVL[1:0], 2nd, 3rd, 4th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 5th, 6th, 7th, 8th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 1stFrameNumber[7:0] | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 2nd | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 3rd | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 4th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 5th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 6th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 7th | 00h |
| 0 | 1 | # | # | # | # | # | # | # | # | # | 8th | 00h | | |

| # | Command | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Registers | Default | |
|----|---|-----|-----|----|----|----|----|----|----|----|----|-----------|--------------------------|-----|
| 13 | LUT Blue (LUTB) (261-byte command, bytes 2~14 repeated 20 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | | 21h | |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | Phase repeat times [7:0] | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 1stLVL[2:0], 2nd, | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 3rd, 4th | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 5th, 6th, | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 7th, 8th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 1stFrameNumber[7:0] | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 2nd | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 3rd | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 4th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 5th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 6th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 7th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 8th | 00h |
| 14 | LUT White (LUTW) (261-byte command, bytes 2~14 repeated 20 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | | 22h | |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | Phase repeat times [7:0] | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 1stLVL[2:0], 2nd, | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 3rd, 4th | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 5th, 6th, | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 7th, 8th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 1stFrameNumber[7:0] | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 2nd | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 3rd | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 4th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 5th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 6th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 7th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 8th | 00h |
| 15 | LUTGray1 (LUTG1) (261-byte command, bytes 2~14 repeated 20 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | | 23h | |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | Phase repeat times [7:0] | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 1stLVL[2:0], 2nd, | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 3rd, 4th | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 5th, 6th, | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 7th, 8th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 1stFrameNumber[7:0] | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 2nd | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 3rd | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 4th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 5th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 6th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 7th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 8th | 00h |

| # | Command | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Registers | Default | |
|----|---|-----|-----|----|----|----|----|----|----|----|----|-----------|--------------------------|-----|
| 16 | LUTGray2 (LUTG2) (261-byte command, bytes 2~14 repeated 20 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | | 24h | |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | Phase repeat times [7:0] | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 1stLVL[2:0], 2nd, | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 3rd, 4th | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 5th, 6th, | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 7th, 8th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 1stFrameNumber[7:0] | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 2nd | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 3rd | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 4th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 5th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 6th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 7th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 8th | 00h |
| 17 | LUT Red0 (LUTR0) (261-byte command, bytes 2~14 repeated 20 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | | 25h | |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | Phase repeat times [7:0] | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 1stLVL[2:0], 2nd, | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 3rd, 4th | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 5th, 6th, | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 7th, 8th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 1stFrameNumber[7:0] | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 2nd | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 3rd | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 4th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 5th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 6th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 7th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 8th | 00h |
| 18 | LUT Red1 (LUTR1) (261-byte command, bytes 2~14 repeated 20 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | | 26h | |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | Phase repeat times [7:0] | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 1stLVL[2:0], 2nd, | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 3rd, 4th | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 5th, 6th, | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 7th, 8th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 1stFrameNumber[7:0] | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 2nd | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 3rd | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 4th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 5th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 6th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 7th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 8th | 00h |

| # | Command | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Registers | Default | |
|----|---|-----|-----|----|----|----|----|----|----|----|----|-----------|--------------------------|-----|
| 19 | LUT Red2 (LUTR2) (261-byte command, bytes 2~14 repeated 20 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | | 27h | |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | Phase repeat times [7:0] | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 1stLVL[2:0], 2nd, | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 3rd, 4th | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 5th, 6th, | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 7th, 8th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 1stFrameNumber[7:0] | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 2nd | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 3rd | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 4th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 5th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 6th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 7th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 8th | 00h |
| 20 | LUT Red3 (LUTR3) (261-byte command, bytes 2~14 repeated 20 times) | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | | 28h | |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | Phase repeat times [7:0] | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 1stLVL[2:0], 2nd, | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 3rd, 4th | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 5th, 6th, | 00h |
| | | 0 | 1 | -- | # | # | # | -- | # | # | # | # | 7th, 8th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 1stFrameNumber[7:0] | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 2nd | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 3rd | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 4th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 5th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 6th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 7th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 8th | 00h |
| 21 | LUT XON (LUTXON) (201-byte command, bytes 2~11 repeated 20 times) | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | | 29h | |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | Phase repeat times [7:0] | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 1stXON[0], 2nd, ..., 8th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 1stFrameNumber[7:0] | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 2nd | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 3rd | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 4th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 5th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 6th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 7th | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | 8th | 00h |
| 22 | PLL control (PLL) | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | 30h | |
| | | 0 | 1 | -- | -- | # | # | # | # | # | # | # | M[2:0], N[2:0] | 3Ch |
| 23 | Temperature Sensor Command (TSC) | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | | 40h | |
| | | 1 | 1 | # | # | # | # | # | # | # | # | # | D[10:3] / TS[7:1] | 00h |
| | | 1 | 1 | # | # | # | -- | -- | -- | -- | -- | -- | D[2:0] / TS[0] | 00h |
| 24 | Temperature Sensor Calibration (TSE) | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | | 41h | |
| | | 0 | 1 | # | -- | -- | -- | # | # | # | # | # | TSE, TO[3:0] | 00h |
| 25 | Temperature Sensor Write (TSW) | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | | 42h | |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | WATTR[7:0] | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | WMSB[7:0] | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | # | WLSB[7:0] | 00h |

| # | Command | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Registers | Default |
|----|--------------------------------------|-----|-----|----|----|----|----|----|----|----|----|---|---------|
| 26 | Temperature Sensor Read (TSR) | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | | 43h |
| | | 1 | 1 | # | # | # | # | # | # | # | # | RMSB[7:0] | 00h |
| | | 1 | 1 | # | # | # | # | # | # | # | # | RLSB[7:0] | 00h |
| 27 | Vcom and data interval setting (CDI) | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | | 50h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | VBD[2:0], DDX, CDI[3:0] | F7h |
| 28 | Lower Power Detection (LPD) | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | | 51h |
| | | 1 | 1 | -- | -- | -- | -- | -- | -- | -- | # | LPD | 01h |
| 29 | TCON setting (TCON) | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | | 60h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | S2G[3:0], G2S[3:0] | 22h |
| 30 | TCON resolution (TRES) | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | | 61h |
| | | 0 | 1 | -- | -- | -- | -- | -- | -- | # | # | HRES[9:0] | 00h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | | 00h |
| | | 0 | 1 | -- | -- | -- | -- | -- | -- | -- | # | VRES[8:0] | 00h |
| 31 | SPI flash control (DAM) | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | | 65h |
| | | 0 | 1 | -- | -- | -- | -- | -- | -- | -- | # | DAM | 00h |
| 32 | Revision (REV) | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | | 70h |
| | | 1 | 1 | # | # | # | # | # | # | # | # | LUTVER[7:0] | 00h |
| | | 1 | 1 | # | # | # | # | # | # | # | # | LUTVER[15:8] | 00h |
| 33 | Get Status (FLG) | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | | 71h |
| | | 1 | 1 | -- | -- | # | # | # | # | # | # | I ² C_ERR, I ² C_BUSYN, DATA_FLAG, PON, POF, BUSY_N | 02h |
| 34 | Auto Measurement Vcom (AMV) | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 80h |
| | | 0 | 1 | -- | -- | # | # | # | # | # | # | AMVT[1:0], AMVX, AMVS, AMV, AMVE | 10h |
| 35 | Read Vcom Value(VV) | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | 81h |
| | | 1 | 1 | -- | # | # | # | # | # | # | # | VV[6:0] | 00h |
| 36 | VCM_DC Setting (VDCS) | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | | 82h |
| | | 0 | 1 | -- | # | # | # | # | # | # | # | VDCS[6:0] | 02h |
| 37 | Power Saving (PWS) | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | | E3h |
| | | 0 | 1 | # | # | # | # | # | # | # | # | VCOM_W[3:0], SD_W[3:0] | 00h |

- Note:**
- (1) All other register addresses are invalid or reserved by UltraChip, and should NOT be used.
 - (2) Any bits shown here as 0 must be written with a 0. All unused bits should also be set to zero. Device malfunction may occur if this is not done.
 - (3) Commands are processed on the 'stop' condition of the interface.
 - (4) Registers marked 'W/R' can be read, but the contents are written when the SPI command completes – so the contents can be read and altered. The user can subsequently write the register to restore the contents following an SPI read.
 - (5) All write commands are "UNAVAILABLE" when BUSY_N=0 is asserted by reset, DSP (R11h), DRF (R12h) or IPC (R13h). All read commands are always "AVAILABLE".
 - * AVAILABLE means that Host can send command/parameter to driver.
 - * UNAVAILABLE means that Host cannot send command/parameter to driver.

COMMAND DESCRIPTION

W/R: 0: Write Cycle / 1: Read Cycle **C/D**: 0: Command / 1: Data **D7-D0**: -: Don't Care

(1) PANEL SETTING (PSR) (R00H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------------|-----|-----|------|------|----|----|----|-----|-------|-------|
| Setting the panel | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 1 | RES1 | RES0 | - | - | UD | SHL | SHD_N | RST_N |
| | 0 | 1 | - | - | - | - | - | - | - | - |

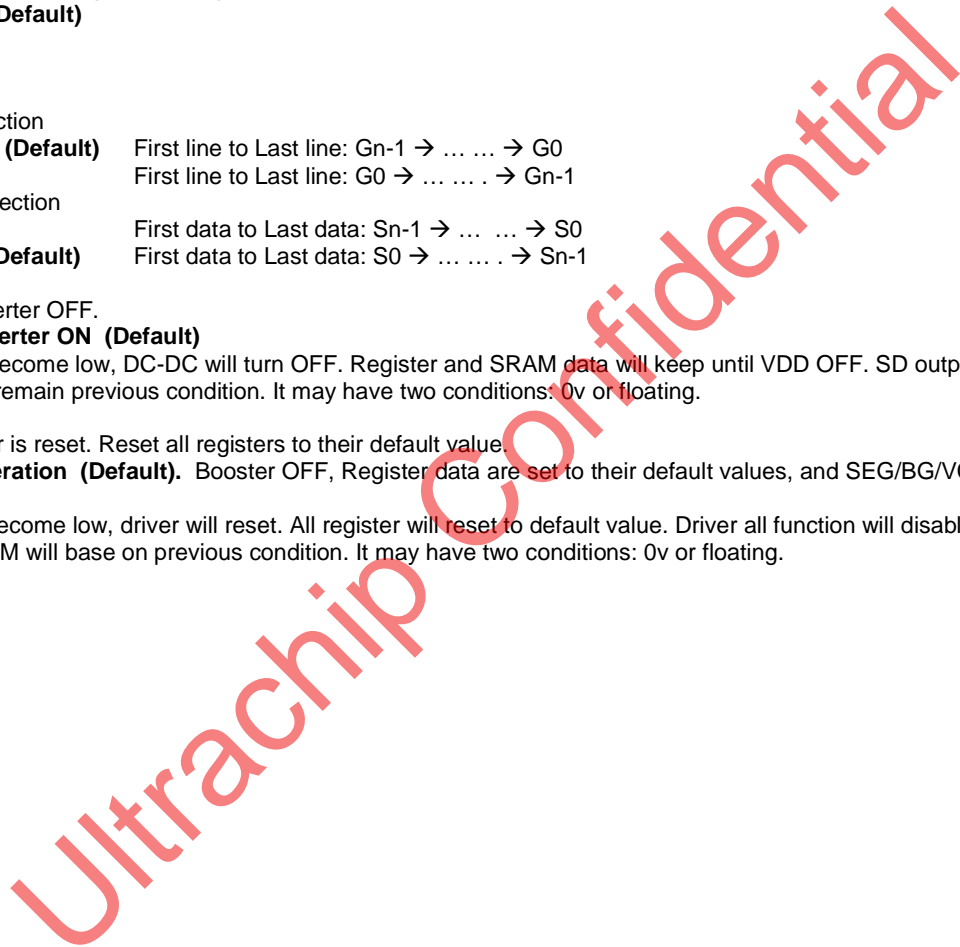
RES[1:0]: Display Resolution setting (source x gate)
00b: 640x480 (Default)
 01b: 600x450
 10b: 640x448
 11b: 600x448

UD: Gate Scan Direction
0: Scan down. (Default) First line to Last line: Gn-1 → ... → G0
 1: Scan up. First line to Last line: G0 → ... → Gn-1

SHL: Source Shift Direction
 0: Shift left. First data to Last data: Sn-1 → ... → S0
1: Shift right. (Default) First data to Last data: S0 → ... → Sn-1

SHD_N: Booster Switch
 0: DC-DC converter OFF.
1: DC-DC converter ON (Default)
 When SHD_N become low, DC-DC will turn OFF. Register and SRAM data will keep until VDD OFF. SD output and VCOM will remain previous condition. It may have two conditions: 0v or floating.

RST_N: Soft Reset
 0: The controller is reset. Reset all registers to their default value.
1: Noormal operation (Default). Booster OFF, Register data are set to their default values, and SEG/BG/VCOM: 0V
 When RST_N become low, driver will reset. All register will reset to default value. Driver all function will disable. SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.



(2) POWER SETTING (PWR) (R01H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
|-----------------------------------|-----|-----|----|----|---------------|-----------|--------|-------|-------------|-------|-----|
| Selecting Internal/External Power | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01h |
| | 0 | 1 | - | - | EDATA_SEL | EDATA_SET | VCM_HZ | VS_EN | VSC_EN | VG_EN | 08h |
| | 0 | 1 | - | - | - | - | - | - | VG_LVL[1:0] | | 01h |
| | 0 | 1 | - | - | VSHC_LVL[5:0] | | | | | | 05h |
| | 0 | 1 | - | - | VSLC_LVL[5:0] | | | | | | 05h |

EDATA_SEL: EDATA selection for pure driver mode
0 : When EDATA_SET=1, pixel bit =2`b11 output VSH_LV level (default)
1 : When EDATA_SET=1, pixel bit =2`b11 output VSL_LV level

EDATA_SET: EDATA setting for pure driver mode
0 : 3-bit data mode for pure driver (default)
1 : 2-bit data mode for pure driver

VCM_HZ: VCOM Hi-Z function
0: VCOM normal output.
1: VCOM floating. (default)

VS_EN: Source power selection.
0 : External source power from VSH and VSL pin. (default)
1 : Internal DCDC function for generate source power.

VSC_EN: Source LV power selection.
0 : External source LV power from VSH_LV and VSL_LV pin. (default)
1 : Internal DCDC function for generate source LV power.

VG_EN: Gate power selection.
0 : External gate power from VGH and VGL pin. (default)
1 : Internal DCDC function for generate gate power.

VG_LVL[1:0]: Internal VGH / VGL Voltage Level Selection.

| VG_LVL[1:0] | Gate Voltage Level |
|-------------|-------------------------------------|
| 00 | VGH=20V, VGL= -20V |
| 01 | VGH=19V, VGL= -19V (Default) |
| 10 | VGH=18V, VGL= -18V |
| 11 | VGH=17V, VGL= -17V |

VSHC_LVL[5:0]: Internal VSH LV Voltage Level Selection for Red LUT.

| VSHC_LVL[5:0] | VSH LV Voltage Level |
|---------------|------------------------|
| 000000 | 3.0 V |
| 000001 | 3.2 V |
| 000010 | 3.4 V |
| 000011 | 3.6 V |
| 000100 | 3.8 V |
| 000101 | 4.0 V (Default) |
| : | : |
| 11 1100 | 15.0 V |

VSLC_LVL[5:0]: Internal VSL LV Voltage Selection for Red LUT.

| VSLC_LVL[5:0] | VSL LV Voltage Level |
|---------------|-------------------------|
| 000000 | -3.0 V |
| 000001 | -3.2 V |
| 000010 | -3.4 V |
| 000011 | -3.6 V |
| 000100 | -3.8 V |
| 000101 | -4.0 V (Default) |
| " | : |
| 11 1100 | -15.0 V |

(3) POWER OFF (POF) (R02H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------------|-----|-----|----|----|----|----|----|----|----|----|
| Turning OFF the power | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

After power off command, driver will power off based on the Power OFF Sequence, BUSY_N signal will become "0".

The Power OFF command will turn off DCDC, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off.

SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

(4) POWER OFF SEQUENCE SETTING (PFS) (R03H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------|-----|-----|----|----|----------------|----|----|----|----|----|
| Setting Power OFF sequence | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| | 0 | 1 | - | - | T_VDS_OFF[1:0] | - | - | - | - | - |

T_VDS_OFF[1:0]: Power OFF Sequence of VSH /VSL and VGH/VGL..

00b: 1 frame (Default)

01b: 2 frames

10b: 3 frames

11b: 4 frame

(5) POWER ON (PON) (REGISTER: R04H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------|-----|-----|----|----|----|----|----|----|----|----|
| Turning ON the power | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

After the Power ON command, driver will power on based on the Power ON Sequence.

After power on command and all power sequence are ready, then BUSY_N signal will become "1".

(6) BOOSTER SOFT START (BTST) (R06H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------|-----|-----|--------|--------|--------|--------|--------|--------|--------|--------|
| Setting Booster Soft Start | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| | 0 | 1 | BTPHA7 | BTPHA6 | BTPHA5 | BTPHA4 | BTPHA3 | BTPHA2 | BTPHA1 | BTPHA0 |
| | 0 | 1 | BTPHB7 | BTPHB6 | BTPHB5 | BTPHB4 | BTPHB3 | BTPHB2 | BTPHB1 | BTPHB0 |
| | 0 | 1 | - | - | BTPHC5 | BTPHC4 | BTPHC3 | BTPHC2 | BTPHC1 | BTPHC0 |

| | | |
|---|---|---|
| BTPHA7[7:6] BTPHB7[7:6] | BTPHA[5:3], BTPHB[5:3], BTPHC[5:3] | BTPHA[2:0] BTPHB[2:0] BTPHC[2:0] |
| Soft Start Phase Period (mS) | Driving Strength | Minimum OFF Time (uS) |
| 00b: 10 mS 01b: 20 10b: 30 11b: 40 | 00b: (reserved) 001b: (reserved) 010b: 1 011b: 2 100b: 3 101b: 4 110b: 5 111b: 6 (strongest) | 000b: 0.26 uS 001b: 0.31 010b: 0.36 011b: 0.52 100b: 0.77 101b: 1.61 110b: 3.43 111b: 6.77 |

(7) DEEP SLEEP (DSLPL) (R07H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------|-----|-----|----|----|----|----|----|----|----|----|
| Deep Sleep | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |

07h
A5h

This command makes the chip enter the deep-sleep mode. The deep sleep mode could return to stand-by mode by hardware reset assertion.

The only one parameter is a check code, the command would be executed if check code is A5h.

(8) DATA START TRANSMISSION 1 (DTM1) (R10H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------|-----|-----|----|--------------------|----|----|----|------------------|----|----|
| Starting data transmission | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| | 0 | 1 | - | KPixel1 [2:0] | | | - | KPixel2 [2:0] | | |
| | 0 | 1 | : | : | | | : | : | | |
| | 0 | 1 | - | Kpixel(2M-1) [2:0] | | | - | Kpixel(2M) [2:0] | | |

10h
00h
00h
00h

This command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a DataStop command (R11H). Then the chip will start to send data/VCOM for panel.

Kpixel[1~2M][2:0] :

| | Source Driver Output | |
|-------------|----------------------|-------|
| | DDX=1 (Default) | DDX=0 |
| KPixel[2:0] | LUT | LUT |
| 000 | Black | White |
| 001 | Gray1 | Gray2 |
| 010 | Gray2 | Gray1 |
| 011 | White | Black |
| 100 | Red0 | Red3 |
| 101 | Red1 | Red2 |
| 110 | Red2 | Red1 |
| 111 | Red3 | Red0 |

(9) DATA STOP (DSP) (R11H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------|-----|-----|-----------|----|----|----|----|----|----|----|
| Stopping data transmission | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| | 1 | 1 | data_flag | - | - | - | - | - | - | - |

11h
00h

To stop data transmission, this command must be issued to check the data_flag.

Data_flag: Data flag of receiving user data.

- 0: Driver didn't receive all the data.
- 1: Driver has already received all the one-frame data (DTM1).

After "Data Start" (10h) or "Data Stop" (11h) commands, BUSY_N signal will become "0" until display update is finished.

(10) DISPLAY REFRESH (DRF) (R12H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------------|-----|-----|----|----|----|----|----|----|----|----|
| Refreshing the display | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |

12h

After this command is issued, driver will refresh display (data/VCOM) according to SRAM data and LUT.

After Display Refresh command, BUSY_N signal will become "0" until display update is finished.

(11) IMAGE PROCESS COMMAND (IPC) (R13H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------------|-----|-----|----|----|----|-------|----|-------------|----|----|
| Image Process Setting | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| | 0 | 1 | - | - | - | IP_EN | - | IP_SEL[2:0] | | |

13h
00h

After this command is issued, image process engine will find thin lines/pixels from frame SRAM and update the frame SRAM for applying new gray level waveform.

IP_EN: Image process enable.
 0: No action.
 1: Image process enable (automatically return to '0' after image process is finished).

IP_SEL[2:0]: Image process selection.
 000 : Deal with 1-pixel width
 001 : Deal with 2-pixel width
 010 : Deal with 3-pixel width
 011 : Deal with 1-pixel and 2-pixel width
 100 : Deal with 1-pixel, 2-pixel and 3-pixel width
 Others : Deal with 1-pixel width

After "Image Process Command" (13h), BUSY_N signal will become "0" until image process is finished.

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(12) VCOM LUT (LUTC) (R20H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
|---|-----|-----|--------------------------|-----------------------|-----------------------|-----------------------|----|----|----|----|-----|-----|
| Build Look-Up Table for VCOM (221-byte command, bytes 2~12 repeated 20 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20h | |
| | 0 | 1 | Phase repeat times [7:0] | | | | | | | | 00h | |
| | 0 | 1 | 1st level sele. [1:0] | 2nd level sele. [1:0] | 3rd level sele. [1:0] | 4th level sele. [1:0] | | | | | | 00h |
| | 0 | 1 | 5th level sele. [1:0] | 6th level sele. [1:0] | 7th level sele. [1:0] | 8th level sele. [1:0] | | | | | | 00h |
| | 0 | 1 | 1st Frame Number [7:0] | | | | | | | | 00h | |
| | 0 | 1 | 2nd Frame Number [7:0] | | | | | | | | 00h | |
| | 0 | 1 | 3rd Frame Number [7:0] | | | | | | | | 00h | |
| | 0 | 1 | 4th Frame Number [7:0] | | | | | | | | 00h | |
| | 0 | 1 | 5th Frame Number [7:0] | | | | | | | | 00h | |
| | 0 | 1 | 6th Frame Number [7:0] | | | | | | | | 00h | |
| | 0 | 1 | 7th Frame Number [7:0] | | | | | | | | 00h | |
| | 0 | 1 | 8th Frame Number [7:0] | | | | | | | | 00h | |

This command builds up VCOM Look-Up Table (LUT). This LUT includes 20 kinds of states, each state is of 11 bytes, as tabove.

Each state is made up 8 phases. And each phase is combined with "Repeat number", "Level selection", and "Frame Number".

Byte 2: repeat number.

Bytes 3 ~ 4: Level selection of each phase.

Bytes 5 ~12: Frame number of each phase.

Bytes 2, 13, 24, 35, 46, ... : Times to Repeat

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255 times

Bytes 3~4, 14~15, 25~26, 36~37, 47~48, ... : Level Selection.

00b: VCM_DC

01b: 15V + VCM_DC (VCOMH)

10b: -15V + VCM_DC (VCOML)

11b: Floating

Bytes 5~12, 16~23, 27~34, 38~45, 49~56, ... : Number of Frames

0000 0000b ~ 1111 1111b: 0 ~ 255 frames

Example:

| Byte | D7~D0 | Remark |
|------|-------------|--|
| 2 | 0000 1000 | Repeat 8 times |
| 3 | 01 00 10 00 | 1st level: VCOMH, 2nd level: -VCM_DC, 3rd level: VCOML, 4th level: -VCM_DC |
| 4 | 01 00 10 00 | 5th level: VCOMH, 6th level: -VCM_DC, 7th level: VCOML, 8th level: -VCM_DC |
| 5 | 0000 0010 | 1st frame number: 2 |
| 6 | 0000 0001 | 2nd frame number: 1 |
| 7 | 0000 0011 | 3rd frame number: 3 |
| 8 | 0000 0001 | 4th frame number: 1 |
| 9 | 0000 0100 | 5th frame number: 4 |
| 10 | 0000 0001 | 6th frame number: 1 |
| 11 | 0000 0101 | 7th frame number: 5 |
| 12 | 0000 0001 | 8th frame number: 1 |

(13) BLACK LUT (LUTB) (R21H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
|--|-----|-----|--------------------------|-----------------------|----|----|----|-----------------------|----|----|-----|-----|
| Build Look-Up Table for Black (261-byte command, bytes 2~14 repeated 20 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21h | |
| | 0 | 1 | Phase repeat times [7:0] | | | | | | | | | 00h |
| | 0 | 1 | - | 1st level sele. [2:0] | | | - | 2nd level sele. [2:0] | | | 00h | |
| | 0 | 1 | - | 3rd level sele. [2:0] | | | - | 4th level sele. [2:0] | | | 00h | |
| | 0 | 1 | - | 5th level sele. [2:0] | | | - | 6th level sele. [2:0] | | | 00h | |
| | 0 | 1 | - | 7th level sele. [2:0] | | | - | 8th level sele. [2:0] | | | 00h | |
| | 0 | 1 | 1st Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 2nd Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 3rd Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 4th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 5th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 6th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 7th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 8th Frame Number [7:0] | | | | | | | | | 00h |

This command builds LUTB for black. This LUT includes 20 kinds of states, each state is of 13 bytes as above.

Each state is made up 8 phases. And each phase is combined with "repeat number", "Level selection", and "frame number".

Byte 2: repeat number.

Bytes 3 ~ 6: Level selection of each phase.

Bytes 7 ~14: Frame number of each phase.

Bytes 2, 15, 28, 41, 54, ... : Times to Repeat

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255 times

Bytes 3~6, 16~19, 29~32, 42~45, 55~58, ... : Level Selection.

000b: 0V

001b: 15V (VSH)

010b: -15V (VSL)

011b: VSH_LV

100b: VSL_LV

101b: VSH_LVX (external source power from VSH_LVX pin)

110b: VSL_LVX (external source power from VSL_LVX pin)

111b: Floating

Bytes 7~14, 20~27, 33~40, 46~53, 59~66, ... : Number of Frames

0000 0000b ~ 1111 1111b: 0 ~ 255 frames

Example:

| | | |
|--------|-----------|--------------------------------------|
| Byte 2 | 0000 0100 | repeat 4 times |
| 3 | 0001 0010 | 1st level: VSH, 2nd level: VSL |
| 4 | 0011 0100 | 3rd level: VSH_LV, 4th level: VSL_LV |
| 5 | 0001 0010 | 5th level: VSH, 6th level: VSL |
| 6 | 0011 0100 | 7th level: VSH_LV, 8th level: VSL_LV |
| 7 | 0000 0001 | 1st frame number: 1 |
| 8 | 0000 0010 | 2nd frame number: 2 |
| 9 | 0000 0011 | 3rd frame number: 3 |
| 10 | 0000 0100 | 4th frame number: 4 |
| 11 | 0000 0101 | 5th frame number: 5 |
| 12 | 0000 0110 | 6th frame number: 6 |
| 13 | 0000 0101 | 7th frame number: 5 |
| 14 | 0000 0001 | 8th frame number: 1 |

(14) LUT WHITE (LUTW) (R22H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
|--|-----|-----|--------------------------|-----------------------|----|----|----|-----------------------|----|----|-----|-----|
| Build Look-Up Table for Gray1 (261-byte command, bytes 2~14 repeated 20 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 23h | |
| | 0 | 1 | Phase repeat times [7:0] | | | | | | | | | 00h |
| | 0 | 1 | - | 1st level sele. [2:0] | | | - | 2nd level sele. [2:0] | | | 00h | |
| | 0 | 1 | - | 3rd level sele. [2:0] | | | - | 4th level sele. [2:0] | | | 00h | |
| | 0 | 1 | - | 5th level sele. [2:0] | | | - | 6th level sele. [2:0] | | | 00h | |
| | 0 | 1 | - | 7th level sele. [2:0] | | | - | 8th level sele. [2:0] | | | 00h | |
| | 0 | 1 | 1st Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 2nd Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 3rd Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 4th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 5th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 6th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 7th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 8th Frame Number [7:0] | | | | | | | | | 00h |

This command builds LUT for White. Please refer to command (13) LUTB for similar definition details.

(15) GRAY1 LUT (LUTG1) (R23H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
|--|-----|-----|--------------------------|-----------------------|----|----|----|-----------------------|----|----|-----|-----|
| Build Look-Up Table for Gray1 (261-byte command, bytes 2~14 repeated 20 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 23h | |
| | 0 | 1 | Phase repeat times [7:0] | | | | | | | | | 00h |
| | 0 | 1 | - | 1st level sele. [2:0] | | | - | 2nd level sele. [2:0] | | | 00h | |
| | 0 | 1 | - | 3rd level sele. [2:0] | | | - | 4th level sele. [2:0] | | | 00h | |
| | 0 | 1 | - | 5th level sele. [2:0] | | | - | 6th level sele. [2:0] | | | 00h | |
| | 0 | 1 | - | 7th level sele. [2:0] | | | - | 8th level sele. [2:0] | | | 00h | |
| | 0 | 1 | 1st Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 2nd Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 3rd Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 4th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 5th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 6th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 7th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 8th Frame Number [7:0] | | | | | | | | | 00h |

This command builds LUT for Gray 1. Please refer to command (13) LUTB for similar definition details.

(16) GRAY2 LUT (LUTG2) (R24H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
|--|-----|-----|--------------------------|-----------------------|----|----|----|-----------------------|----|----|-----|-----|
| Build Look-Up Table for Gray2 (261-byte command, bytes 2~14 repeated 20 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 24h | |
| | 0 | 1 | Phase repeat times [7:0] | | | | | | | | | 00h |
| | 0 | 1 | - | 1st level sele. [2:0] | | | - | 2nd level sele. [2:0] | | | 00h | |
| | 0 | 1 | - | 3rd level sele. [2:0] | | | - | 4th level sele. [2:0] | | | 00h | |
| | 0 | 1 | - | 5th level sele. [2:0] | | | - | 6th level sele. [2:0] | | | 00h | |
| | 0 | 1 | - | 7th level sele. [2:0] | | | - | 8th level sele. [2:0] | | | 00h | |
| | 0 | 1 | 1st Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 2nd Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 3rd Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 4th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 5th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 6th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 7th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 8th Frame Number [7:0] | | | | | | | | | 00h |

This command builds LUT for Gray 2. Please refer to command (13) LUTB for similar definition details.

(17) RED0 LUT (LUTR0) (R25H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
|---|-----|-----|--------------------------|-----------------------|----|----|----|-----------------------|----|----|-----|-----|
| Build Look-Up Table for Red0 (261-byte command, bytes 2~14 repeated 20 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 25h | |
| | 0 | 1 | Phase repeat times [7:0] | | | | | | | | | 00h |
| | 0 | 1 | - | 1st level sele. [2:0] | | | - | 2nd level sele. [2:0] | | | 00h | |
| | 0 | 1 | - | 3rd level sele. [2:0] | | | - | 4th level sele. [2:0] | | | 00h | |
| | 0 | 1 | - | 5th level sele. [2:0] | | | - | 6th level sele. [2:0] | | | 00h | |
| | 0 | 1 | - | 7th level sele. [2:0] | | | - | 8th level sele. [2:0] | | | 00h | |
| | 0 | 1 | 1st Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 2nd Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 3rd Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 4th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 5th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 6th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 7th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 8th Frame Number [7:0] | | | | | | | | | 00h |

This command builds LUT for Red 0. Please refer to command (13) LUTB for similar definition details.

(18) RED1 LUT (LUTR1) (R26H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
|---|-----|-----|--------------------------|-----------------------|----|----|----|-----------------------|----|----|-----|-----|
| Build Look-Up Table for Red1 (261-byte command, bytes 2~14 repeated 20 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 26h | |
| | 0 | 1 | Phase repeat times [7:0] | | | | | | | | | 00h |
| | 0 | 1 | - | 1st level sele. [2:0] | | | - | 2nd level sele. [2:0] | | | 00h | |
| | 0 | 1 | - | 3rd level sele. [2:0] | | | - | 4th level sele. [2:0] | | | 00h | |
| | 0 | 1 | - | 5th level sele. [2:0] | | | - | 6th level sele. [2:0] | | | 00h | |
| | 0 | 1 | - | 7th level sele. [2:0] | | | - | 8th level sele. [2:0] | | | 00h | |
| | 0 | 1 | 1st Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 2nd Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 3rd Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 4th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 5th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 6th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 7th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 8th Frame Number [7:0] | | | | | | | | | 00h |

This command builds LUT for Red 1. Please refer to command (13) LUTB for similar definition details.

(19) RED2 LUT (LUTR2) (R27H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
|---|-----|-----|--------------------------|-----------------------|----|----|----|-----------------------|----|----|-----|-----|
| Build Look-Up Table for Red2 (261-byte command, bytes 2~14 repeated 20 times) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 27h | |
| | 0 | 1 | Phase repeat times [7:0] | | | | | | | | | 00h |
| | 0 | 1 | - | 1st level sele. [2:0] | | | - | 2nd level sele. [2:0] | | | 00h | |
| | 0 | 1 | - | 3rd level sele. [2:0] | | | - | 4th level sele. [2:0] | | | 00h | |
| | 0 | 1 | - | 5th level sele. [2:0] | | | - | 6th level sele. [2:0] | | | 00h | |
| | 0 | 1 | - | 7th level sele. [2:0] | | | - | 8th level sele. [2:0] | | | 00h | |
| | 0 | 1 | 1st Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 2nd Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 3rd Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 4th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 5th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 6th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 7th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 8th Frame Number [7:0] | | | | | | | | | 00h |

This command builds LUT for Red 2. Please refer to command (13) LUTB for similar definition details.

(20) RED3 LUT (LUTR3) (R28H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
|---|-----|-----|--------------------------|-----------------------|----|----|----|-----------------------|----|----|-----|-----|
| Build Look-Up Table for Red3 (261-byte command, bytes 2~14 repeated 20 times) | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 28h | |
| | 0 | 1 | Phase repeat times [7:0] | | | | | | | | | 00h |
| | 0 | 1 | - | 1st level sele. [2:0] | | | - | 2nd level sele. [2:0] | | | 00h | |
| | 0 | 1 | - | 3rd level sele. [2:0] | | | - | 4th level sele. [2:0] | | | 00h | |
| | 0 | 1 | - | 5th level sele. [2:0] | | | - | 6th level sele. [2:0] | | | 00h | |
| | 0 | 1 | - | 7th level sele. [2:0] | | | - | 8th level sele. [2:0] | | | 00h | |
| | 0 | 1 | 1st Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 2nd Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 3rd Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 4th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 5th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 6th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 7th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 8th Frame Number [7:0] | | | | | | | | | 00h |

This command builds LUT for Red 3. Please refer to command (13) LUTB for similar definition details.

(21) XON LUT (LUTXON) (R29H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
|--|-----|-----|--------------------------|---------|---------|---------|---------|---------|---------|---------|-----|-----|
| Build Look-Up Table for XON (201-byte command, bytes 2~11 repeated 20 times) | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 29h | |
| | 0 | 1 | Phase repeat times [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 1st XON | 2nd XON | 3rd XON | 4th XON | 5th XON | 6th XON | 7th XON | 8th XON | 00h | |
| | 0 | 1 | 1st Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 2nd Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 3rd Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 4th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 5th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 6th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 7th Frame Number [7:0] | | | | | | | | | 00h |
| | 0 | 1 | 8th Frame Number [7:0] | | | | | | | | | 00h |

This command builds LUT for XON. This LUT includes 20 kinds of states, each state is of 10 bytes as above.

Each state is made up 8 phases. And each phase is combined with "repeat number", "XON selection", and "frame number".

Byte 2: Repeat number.

Bytes 3: Level selection of each phase.

Bytes 4 ~11: Frame number of each phase.

Bytes 2, 12, 22, 32, 42, ... : Times to Repeat

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255 times

Bytes 3, 13, 23, 43, 53, ... : XON Selection.

0: All gate ON (VGH)

1: Normal gate scan function

Bytes 4~11, 14~21, 24~31, 34~41, 44~51, ... : Number of Frames

0000 0000b ~ 1111 1111b: 0 ~ 255 frames

(22) PLL CONTROL (PLL) (R30H)

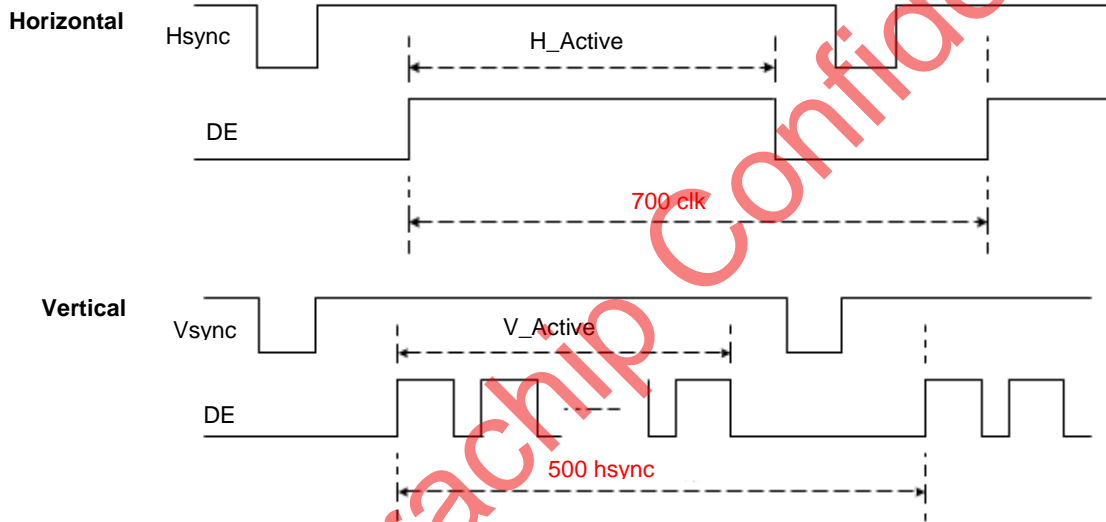
| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------|-----|-----|----|----|--------|----|----|--------|----|----|
| Controlling PLL | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| | 0 | 1 | - | - | M[2:0] | | | N[2:0] | | |

30h
3Ch

The command controls the PLL clock frequency. The PLL structure supports the following frame rates:

(FR: Frame Rate, Unit: Hz)

| M | N | FR | M | N | FR | M | N | FR | M | N | FR | M | N | FR | M | N | FR | M | N | FR |
|---|---|----|---|---|----|---|---|----|---|---|-----|---|---|-----|---|---|-----|---|---|-----|
| 1 | 1 | 29 | 2 | 1 | 57 | 3 | 1 | 86 | 4 | 1 | 114 | 5 | 1 | 143 | 6 | 1 | 171 | 7 | 1 | 200 |
| | 2 | 14 | | 2 | 29 | | 2 | 43 | | 2 | 59 | | 2 | 71 | | 2 | 86 | | 2 | 100 |
| | 3 | 10 | | 3 | 19 | | 3 | 29 | | 3 | 38 | | 3 | 48 | | 3 | 57 | | 3 | 67 |
| | 4 | 5 | | 4 | 14 | | 4 | 21 | | 4 | 29 | | 4 | 36 | | 4 | 43 | | 4 | 50 |
| | 5 | 7 | | 5 | 11 | | 5 | 17 | | 5 | 23 | | 5 | 29 | | 5 | 34 | | 5 | 40 |
| | 6 | 6 | | 6 | 10 | | 6 | 14 | | 6 | 19 | | 6 | 24 | | 6 | 29 | | 6 | 33 |
| | 7 | 5 | | 7 | 8 | | 7 | 12 | | 7 | 16 | | 7 | 20 | | 7 | 24 | | 7 | 29 |



(23) TEMPERATURE SENSOR COMMAND (TSC) (R40H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------------|-----|-----|----------|----------|----------|----------|----------|----------|----------|----------|
| Sensing Temperature | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 1 | 1 | D10 | D9 / TS7 | D8 / TS6 | D7 / TS5 | D6 / TS4 | D5 / TS3 | D4 / TS2 | D3 / TS1 |
| | 1 | 1 | D2 / TS0 | D1 | D0 | - | - | - | - | - |

This command reads the temperature sensed by the temperature sensor.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

| TS[7:0] | Temperature (°C) |
|------------|------------------|
| 0000 0000b | 0 |
| 0000 0001b | 0.5 |
| 0000 0010b | 1 |
| 0000 0011b | 1.5 |
| : | : |
| 0111 1000b | 60 |

BUSY_N become low after TSC command. When BUSY_N become high, Parameter can be read.



(24) TEMPERATURE SENSOR INTERNAL/EXTERNAL (TSE) (R41H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------------------|-----|-----|-----|----|----|----|---------|----|----|----|
| Calibrate Temperature Sensor | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| | 0 | 1 | TSE | - | - | - | TO[3:0] | | | |

41h
00h

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Select internal temperature sensor (default)

1: Select external temperature sensor.

TO[3:0]: Temperature Offset

| TO[3:0] | Temperature Offset |
|---------|--------------------|
| 0000 | +0 (Default) |
| 0001 | +0.5 |
| 0010 | +1.0 |
| 0011 | +1.5 |
| 0100 | +2.0 |
| 0101 | +2.5 |
| 0110 | +3.0 |
| 0111 | +3.5 |

| TO[3:0] | Temperature Offset |
|---------|--------------------|
| 1000 | -4.0 |
| 1001 | -3.5 |
| 1010 | -3.0 |
| 1011 | -2.5 |
| 1100 | -2.0 |
| 1101 | -1.5 |
| 1110 | -1.0 |
| 1111 | -0.5 |

(25) TEMPERATURE SENSOR WRITE (TSW) (R42H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------------------|-----|-----|------------|----|----|----|----|----|----|----|
| Temperature Sensor Write | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| | 0 | 1 | WATTR[7:0] | | | | | | | |
| | 0 | 1 | WMSB[7:0] | | | | | | | |
| | 0 | 1 | WLSB[7:0] | | | | | | | |

42h
00h
00h
00h

This command could write data to the external temperature sensor.

WATTR: **D[7:6]:** I²C Write Byte Number
 00: 1 byte (head byte only)
 01: 2 bytes (head byte + pointer)
 10: 3 bytes (head byte + pointer + 1st parameter)
 11: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

D[5:3]: User-defined address bits (A2, A1, A0)

D[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor

WLSB[7:0]: LSByte of write-data to external temperature sensor

(26) TEMPERATURE SENSOR READ (TSR) (R43H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------------------|-----|-----|-----------|----|----|----|----|----|----|----|
| Temperature Sensor Read | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| | 0 | 1 | RMSB[7:0] | | | | | | | |
| | 0 | 1 | RLSB[7:0] | | | | | | | |

42h
00h
00h

This command could read data from the external temperature sensor.

RMSB[7:0]: MSByte of read-data from external temperature sensor

RLSB[7:0]: LSByte of read-data from external temperature sensor

(27) VCOM AND DATA INTERVAL SETTING (CDI) (R50H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------------------------|-----|-----|----------|----|----|-----|----------|----|----|----|
| Set Interval between Vcom and Data | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| | 0 | 1 | VBD[2:0] | | | DDX | CDI[3:0] | | | |

This command indicates the interval of Vcom and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

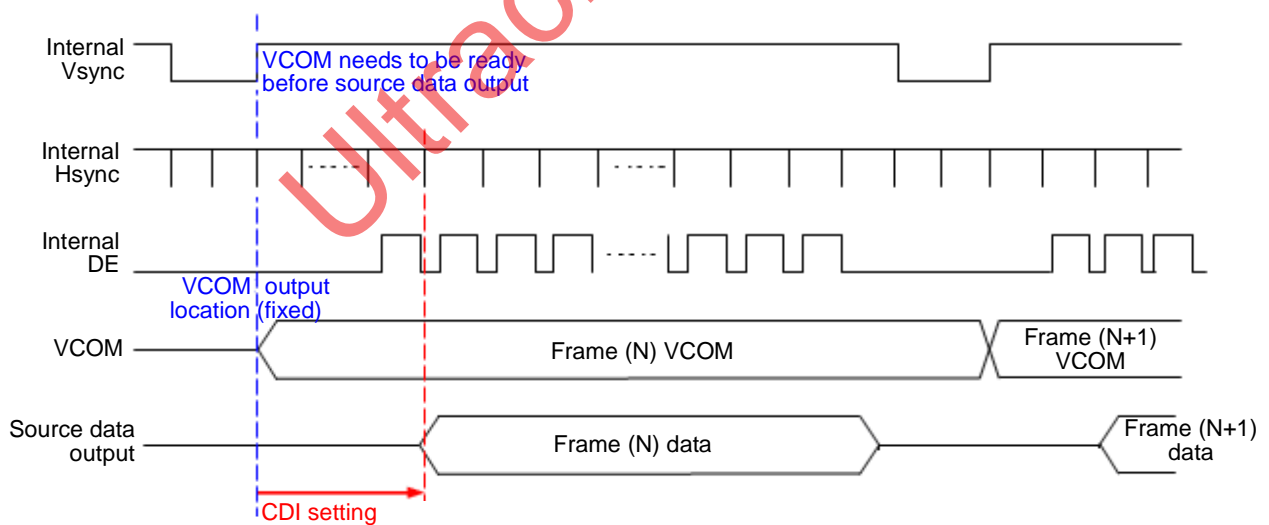
VBD[2:0]: Border output selection

DDX: Data polarity.

| | Border Output | |
|----------|-----------------|----------|
| | DDX=1 (Default) | DDX=0 |
| VBD[2:0] | LUT | LUT |
| 000 | Black | White |
| 001 | Gray1 | Gray2 |
| 010 | Gray2 | Gray1 |
| 011 | White | Black |
| 100 | Red0 | Floating |
| 101 | Red1 | Red2 |
| 110 | Red2 | Red1 |
| 111 | Floating | Red0 |

CDI[3:0]: Vcom and data interval

| CDI[3:0] | Vcom and Data Interval | CDI[3:0] | Vcom and Data Interval |
|----------|------------------------|----------|------------------------|
| 0000 b | 17 hsync | 1000 | 9 |
| 0001 | 16 | 1001 | 8 |
| 0010 | 15 | 1010 | 7 |
| 0011 | 14 | 1011 | 6 |
| 0100 | 13 | 1100 | 5 |
| 0101 | 12 | 1101 | 4 |
| 0110 | 11 | 1110 | 3 |
| 0111 | 10 (Default) | 1111 | 2 |



(28) LOW POWER DETECTION (LPD) (R51H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------|-----|-----|----|----|----|----|----|----|----|-----|
| Detect Low Power | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| | 1 | 1 | - | - | - | - | - | - | - | LPD |

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal temperature sensor switch

0: Low power input ($V_{DD} < 2.5V$)

1: Normal status (default)

(29) TCON SETTING (TCON) (R60H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------------|-----|-----|----------|----|----|----|----------|----|----|----|
| Sensing Temperature | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 1 | S2G[3:0] | | | | G2S[3:0] | | | |

This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

| S2G[3:0] or G2S[3:0] | Period | S2G[3:0] or G2S[3:0] | Period |
|----------------------|---------------------|----------------------|--------|
| 0000 b | 4 | 1000 | 36 |
| 0001 | 8 | 1001 | 40 |
| 0010 | 12 (Default) | 1010 | 44 |
| 0011 | 16 | 1011 | 48 |
| 0100 | 20 | 1100 | 52 |
| 0101 | 24 | 1101 | 56 |
| 0110 | 28 | 1110 | 60 |
| 0111 | 32 | 1111 | 64 |

Period = 500 nS.



(30) RESOLUTION SETTING (TRES) (R61H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------------|-----|-----|-----------|----|----|----|----|----|-----------|---------|
| Set Display Resolution | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| | 0 | 1 | - | - | - | - | - | - | HRES[9:8] | |
| | 0 | 1 | HRES[7:0] | | | | | | | |
| | 0 | 1 | - | - | - | - | - | - | - | VRES[8] |
| | 0 | 1 | VRES[7:0] | | | | | | | |

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

HRES[9:0]: Horizontal Display Resolution

VRES[8:0]: Vertical Display Resolution

Resolution setting (R61H) has higher priority than RES[1:0] (R00H). Horizontal resolution should be even number.

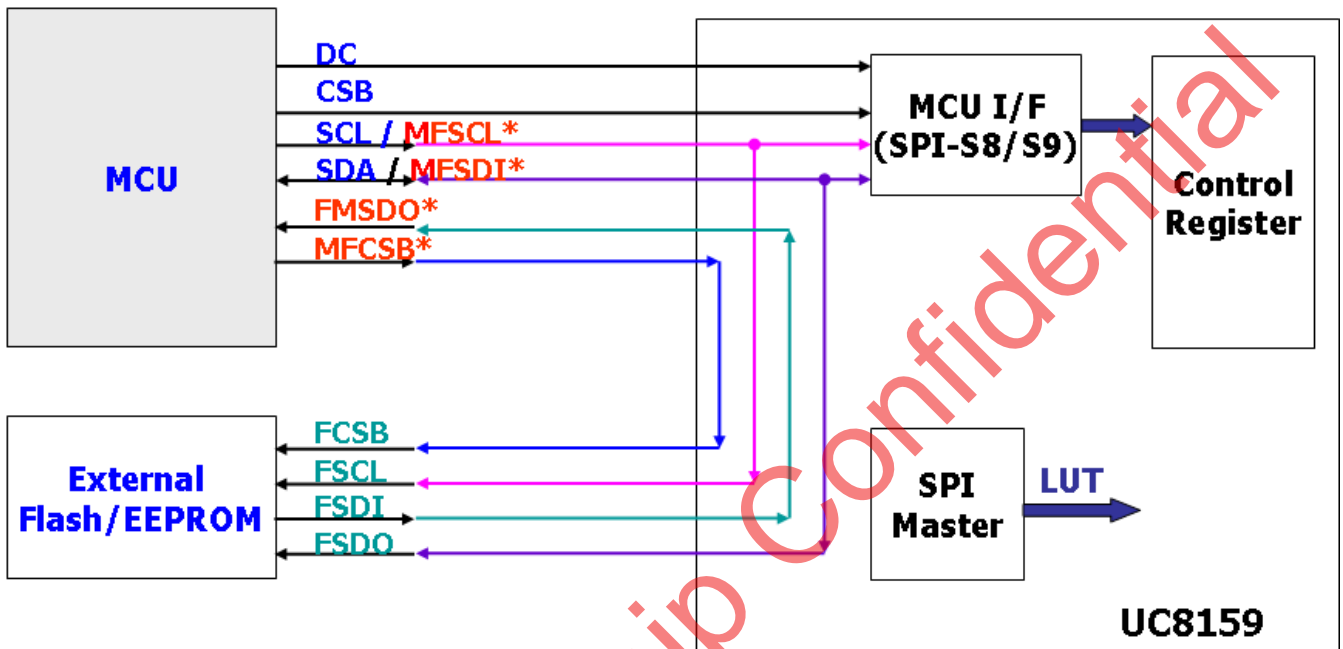
(31) SPI FLASH CONTROL (DAM) (R65H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------------|-----|-----|----|----|----|----|----|----|----|-----|
| Control SPI Flash | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| | 0 | 1 | - | - | - | - | - | - | - | DAM |

This command defines how MCU host directly access external flash/EEPROM mode.

DAM: 0: Disable (Default)

1: Enable. By pass MFSCS*, MFSDI*, FMSDO*, and MFCSB* to external flash.



MCU and External SPI Flash/EEPROM Connection in DAM mode

(32) REVISION (REV) (R70H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------------|-----|-----|--------------|----|----|----|----|----|----|----|
| LUT / Chip Revision | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| | 1 | 1 | LUTVER[7:0] | | | | | | | |
| | 1 | 1 | LUTVER[15:8] | | | | | | | |

The LUTVER[15:0] is read from Flash address from 25001 to 25000.

LUTVER[15:0]: LUT version.

(33) GET STATUS (FLG) (R71H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------|-----|-----|----|----|---------|-----------|-----------|-----|-----|--------|
| Read Flags | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| | 1 | 1 | - | - | I2C_ERR | I2C_BUSYN | Data_flag | PON | POF | BUSY_N |

This command reads the IC status.

I2C_ERR: I²C master error status

I2C_BUSYN: I²C master busy status (low active)

Data_flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY_N: Driver busy status (low active)

(34) AUTO MEASURE VCOM (AMV) (R80H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------|-----|-----|----|----|-----------|----|------|------|-----|------|
| Automatically measure Vcom | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 1 | - | - | AMVT[1:0] | | AMVX | AMVS | AMV | AMVE |

This command implements related VCOM sensing setting.

AMVT[1:0]: Auto Measure Vcom Time

00b: 3s

10b: 8s

01b: 5s (default)

11b: 10s

AMVX: Auto Measure VCOM without XON function

0: Measure VCOM without XON function. (Gate scanning) (default)

1: Measure VCOM with XON function. (All Gate ON)

AMVS: Source output of AMV

0: Set Source output to 0V during Auto Measure VCOM period. (default)

1: Set Source output to VSH_LV during Auto Measure VCOM period.

AMV: Analog signal

0: Get Vcom value with the VV command (R81h) (default)

1: Get Vcom value in analog signal.

AMVE: Auto Measure Vcom Enable (/Disable)

0: Disabled

1: Enabled

(34) VCOM VALUE (VV) (R81H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------|-----|-----|----|---------|----|----|----|----|----|----|
| Automatically measure Vcom | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| | 1 | 1 | - | VV[6:0] | | | | | | |

81h
00h

This command gets the Vcom value.

VV[6:0]: Vcom Value Output

| VV[6:0] | Vcom value |
|-----------|------------|
| 000 0000b | 0 V |
| 000 0001b | -0.05 V |
| 000 0010b | -0.10 V |
| 000 0011b | -0.15 V |
| 000 0100b | -0.20 V |
| : | : |
| 101 0000b | -4.0 V |
| (others) | -4.0 V |

(36) VCM_DC SETTING (VDCS) (R82H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------|-----|-----|----|-----------|----|----|----|----|----|----|
| Set VCM_DC | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | 0 | 1 | - | VDCS[6:0] | | | | | | |

82h
02h

This command sets VCOM_DC value.

VDCS[6:0]: VCOM_DC Setting

| VDCS[6:0] | Vcom_DC value |
|-----------|---------------|
| 000 0000b | (Reserved) |
| 000 0001b | (Reserved) |
| 000 0010b | -0.10 V |
| 000 0011b | -0.15 V |
| 000 0100b | -0.20 V |
| : | : |
| 101 0000b | -4.0 V |
| (others) | -4.0 V |

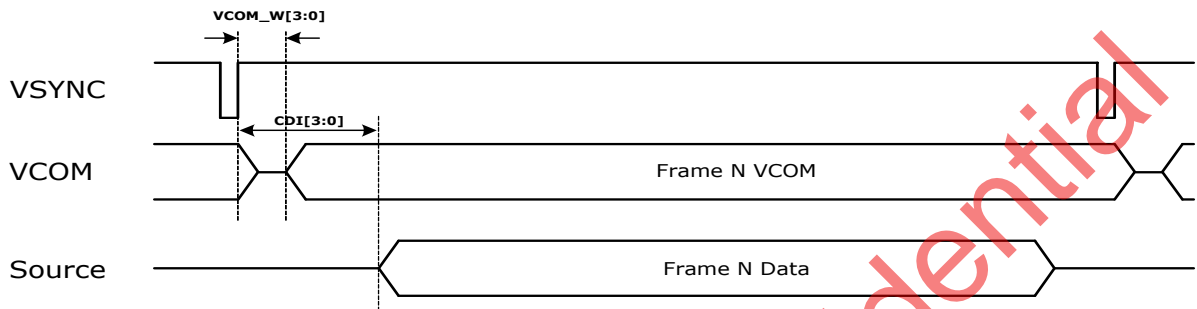
(37) POWER SAVING (PWS) (RE3H)

| Action | W/R | C/D | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------------------|-----|-----|-------------|----|----|----|-----------|----|----|----|
| VCOM/Source Power Saving | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | 0 | 1 | VCOM_W[3:0] | | | | SD_W[3:0] | | | |

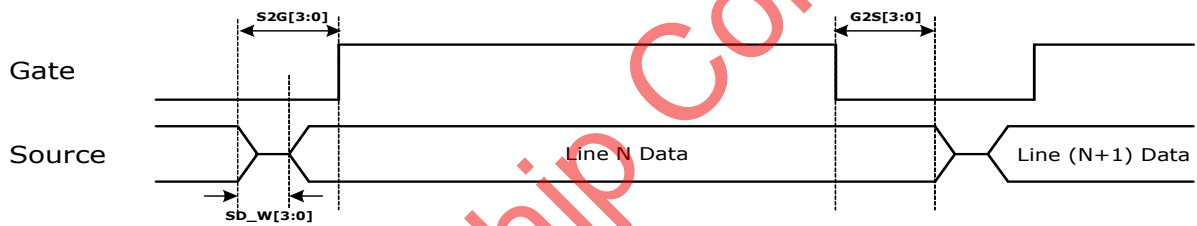
E3h
00h

This command is sets for saving power VCOM/Source power saving during display refresh period. If the output voltage of VCOM/Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W[3:0]: VCOM_power saving width. (unit : line period)



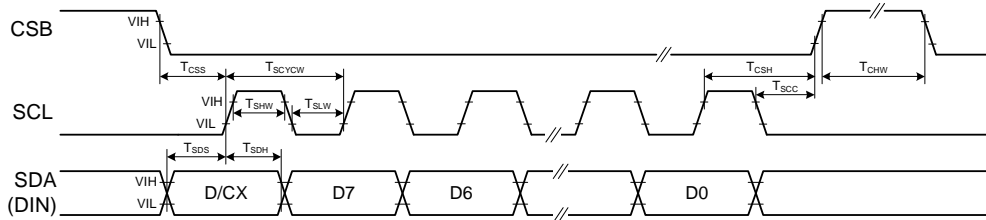
SD_W[3:0]: Source power saving width. (unit : 500ns)



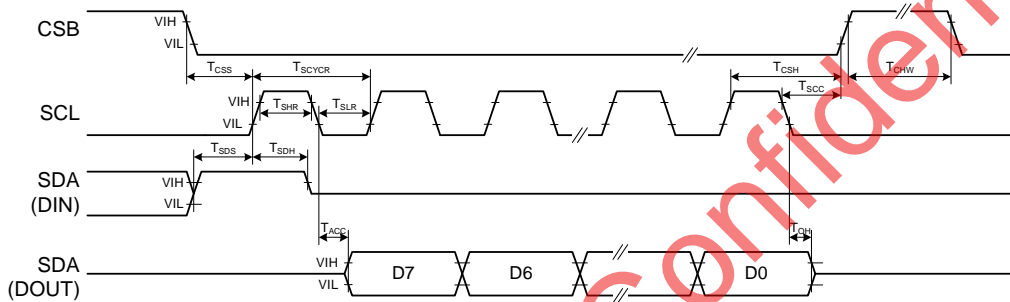
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HOST INTERFACES

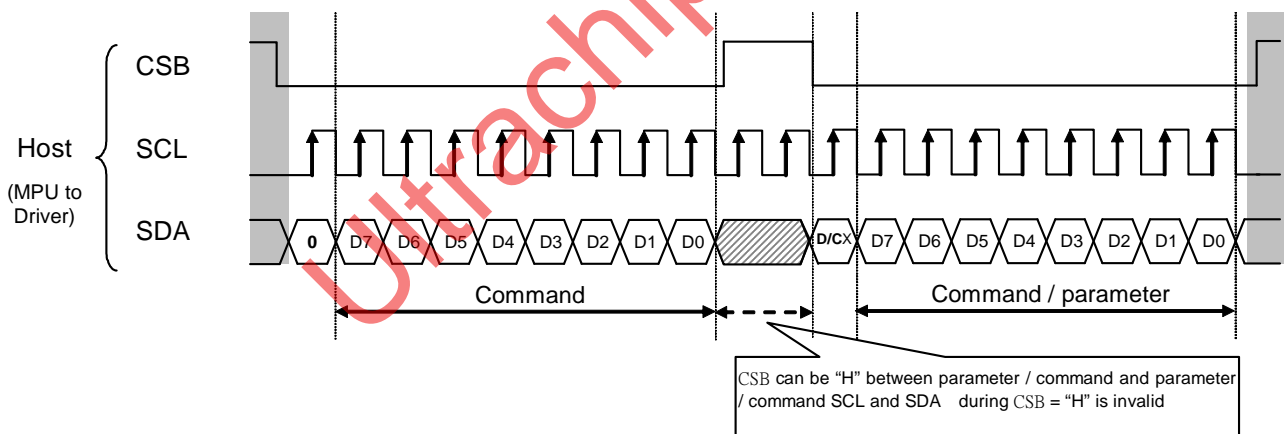
3-WIRE SPI



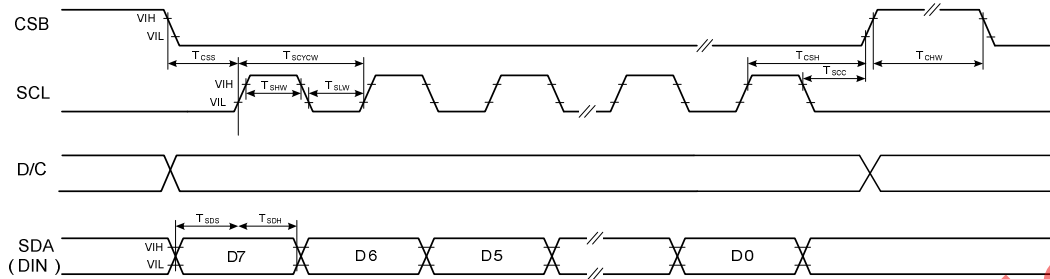
3 pin serial interface characteristics (write mode)



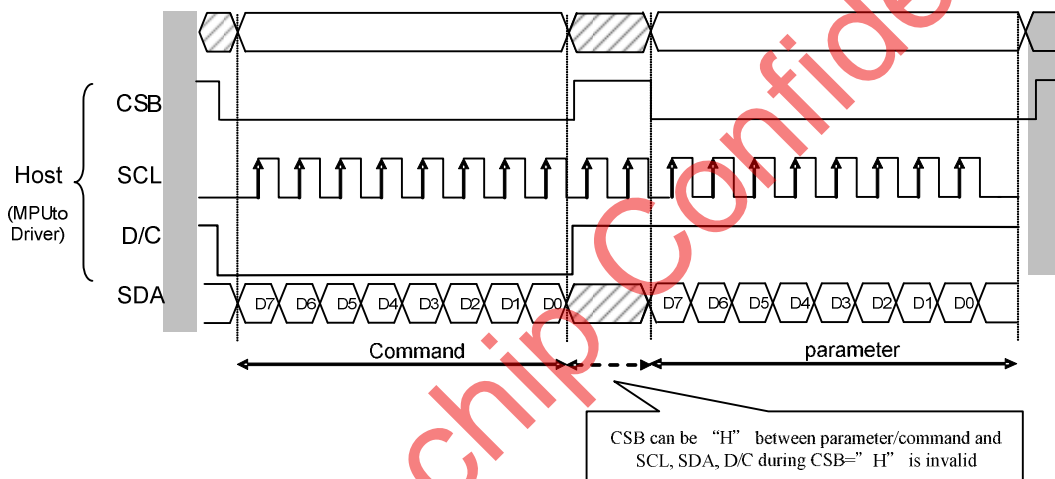
3 pin serial interface characteristics (read mode)



4-WIRE SPI

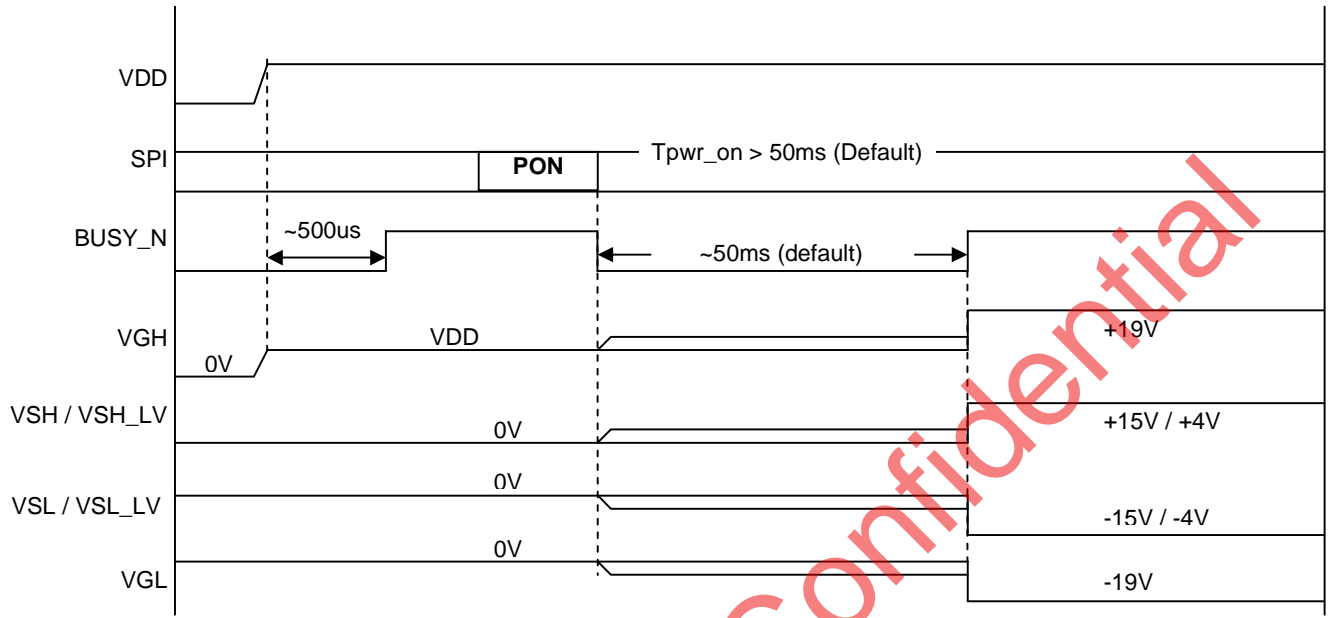


4 pin serial interface characteristics



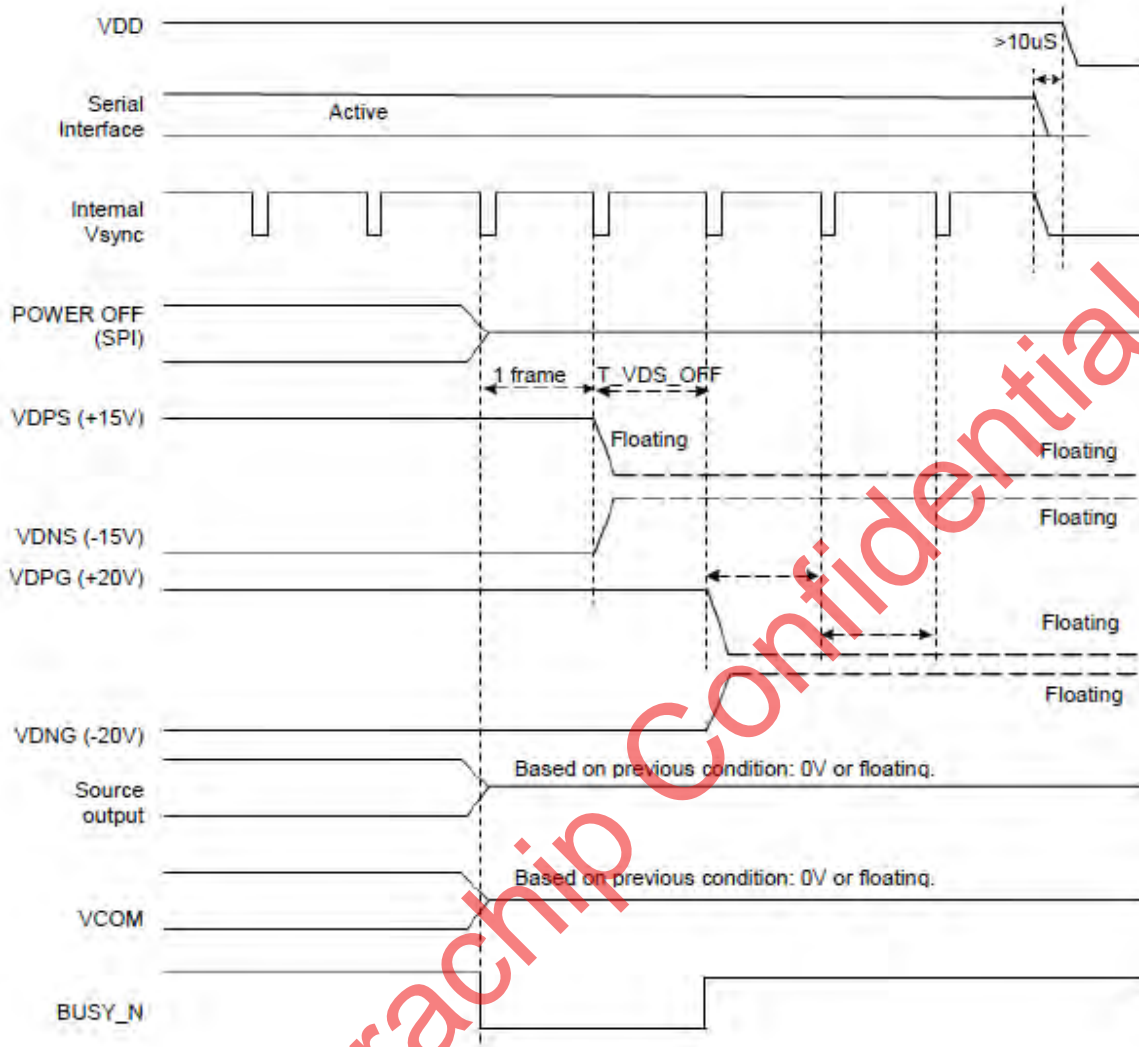
POWER MANAGEMENT

Power ON Sequence



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Power OFF Sequence



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LUT (Lookup Table) Definition

The LUT stored in external flash/EEPROM contains 10 temperature segments for application. And there are waveform, VCOM, XON, VDPS_LVSHC_LVL, VDNS_LVSLC_LVL, etc. After command DSP or DRF is asserted, the driver gets related temperature information and LUT data from the external flash/EEPROM. The corresponding VCOM/LUT/XON waveform will output. The total size of LUT is 25031 bytes.

| Address | Category | Address | Temp. | Address | LUT | Remark | | |
|---------|--|---------|---------------|-----------------|--------------|--|--------------|--------------|
| 00000 | Waveform LUT (T0~T9) (20800) | 0 | T0 (2080) | 0~259 (260) | LUTB | See command LUTB (R21h) for details | | |
| : | | : | | 260~519 (260) | LUTW | LUTW (R22h) | | |
| : | | : | | 520~779 (260) | LUTG1 | LUTG1 (R23h) | | |
| : | | : | | 780~1039 (260) | LUTG2 | LUTG2 (R24h) | | |
| : | | : | | 1040~1299 (260) | LUTR0 | LUTR0 (R25h) | | |
| : | | : | | 1300~1559 (260) | LUTR1 | LUTR1 (R26h) | | |
| : | | : | | 1560~1819 (260) | LUTR2 | LUTR2 (R27h) | | |
| : | | : | | 1820~2079 (260) | LUTR3 | LUTR3 (R28h) | | |
| 20799 | | | | (2080) | T1 | 2080~4159 | 8 LUT | (Same as T0) |
| | | | | (2080) | T2 | 4160~6239 | 8 LUT | (Same as T0) |
| | | | (2080) | T3 | 6240~8319 | 8 LUT | (Same as T0) | |
| | | | (2080) | T4 | 8320~10399 | 8 LUT | (Same as T0) | |
| | | | (2080) | T5 | 10400~12479 | 8 LUT | (Same as T0) | |
| | | | (2080) | T6 | 12480~14559 | 8 LUT | (Same as T0) | |
| | | (2080) | T7 | 14560~16639 | 8 LUT | (Same as T0) | | |
| | | (2080) | T8 | 16640~18719 | 8 LUT | (Same as T0) | | |
| | | (2080) | T9 | 18720~20799 | 8 LUT | (Same as T0) | | |
| 20800 | VCOM LUT (T0~T9) (2200) | (220) | T0 | 20800~21019 | VCOM | See command LUTC (R20h) for details | | |
| : | | (220) | T1 | 21020~21239 | | | | |
| : | | (220) | T2 | 21240~21459 | | | | |
| : | | (220) | T3 | 21460~21679 | | | | |
| : | | (220) | T4 | 21680~21899 | | | | |
| : | | (220) | T5 | 21900~22119 | | | | |
| | | (220) | T6 | 22120~22339 | | | | |
| | | (220) | T7 | 22340~22559 | | | | |
| | | (220) | T8 | 22560~22779 | | | | |
| 22999 | | | (220) | T9 | | | 22780~22999 | |
| 23000 | XON LUT (T0~T9) (2000) | (200) | T0 | 23000~23199 | XON | See command LUTXON (R29h) for details | | |
| : | | (200) | T1 | 23200~23399 | | | | |
| : | | (200) | T2 | 23400~23599 | | | | |
| : | | (200) | T3 | 23600~23799 | | | | |
| | | (200) | T4 | 23800~23999 | | | | |
| | | (200) | T5 | 24000~24199 | | | | |
| | | (200) | T6 | 24200~24399 | | | | |
| | | (200) | T7 | 24400~24599 | | | | |
| | | (200) | T8 | 24600~24799 | | | | |
| 24999 | | | (200) | T9 | | | 24800~24999 | |
| 25000 | Waveform version | (2) | -- | 25000~25001 | LUTVER | If both are FFh, this flash is not programmable yet. | | |
| 25002 | Temperature Boundary (TB0~TB8) | (9) | -- | 25002~25010 | TB | 9 temperature boundary for LUT | | |
| 25010 | | | | | | | | |
| 25011 | T0_VSHC_LVL, T0_VSLC_LVL, T1_VSHC_LVL, T1_VSLC_LVL, : T9_VSHC_LVL, T9_VSLC_LVL | (20) | T0 T9 | 25011~25030 | VSHC VSLC | See VSH_LV / VSL_LV voltage setting (R01h) | | |
| 25030 | | | | | | | | |

Temperature Segment Selection

There are 10 temperature segments which could be selected by specifying TB0~TB8 (address: 25002~25010). The comparison condition between real environment temperature and TB0~TB8 is illustrated as the below table.

| Order | Comparison Condition | Segment |
|-------|------------------------|------------|
| 1 | Real Temp. < TB0 | T0 Segment |
| 2 | TB0 ≤ Real Temp. < TB1 | T1 Segment |
| 3 | TB1 ≤ Real Temp. < TB2 | T2 Segment |
| 4 | TB2 ≤ Real Temp. < TB3 | T3 Segment |
| 5 | TB3 ≤ Real Temp. < TB4 | T4 Segment |
| 6 | TB4 ≤ Real Temp. < TB5 | T5 Segment |
| 7 | TB5 ≤ Real Temp. < TB6 | T6 Segment |
| 8 | TB6 ≤ Real Temp. < TB7 | T7 Segment |
| 9 | TB7 ≤ Real Temp. < TB8 | T8 Segment |
| 10 | TB8 ≤ Real Temp. | T9 Segment |

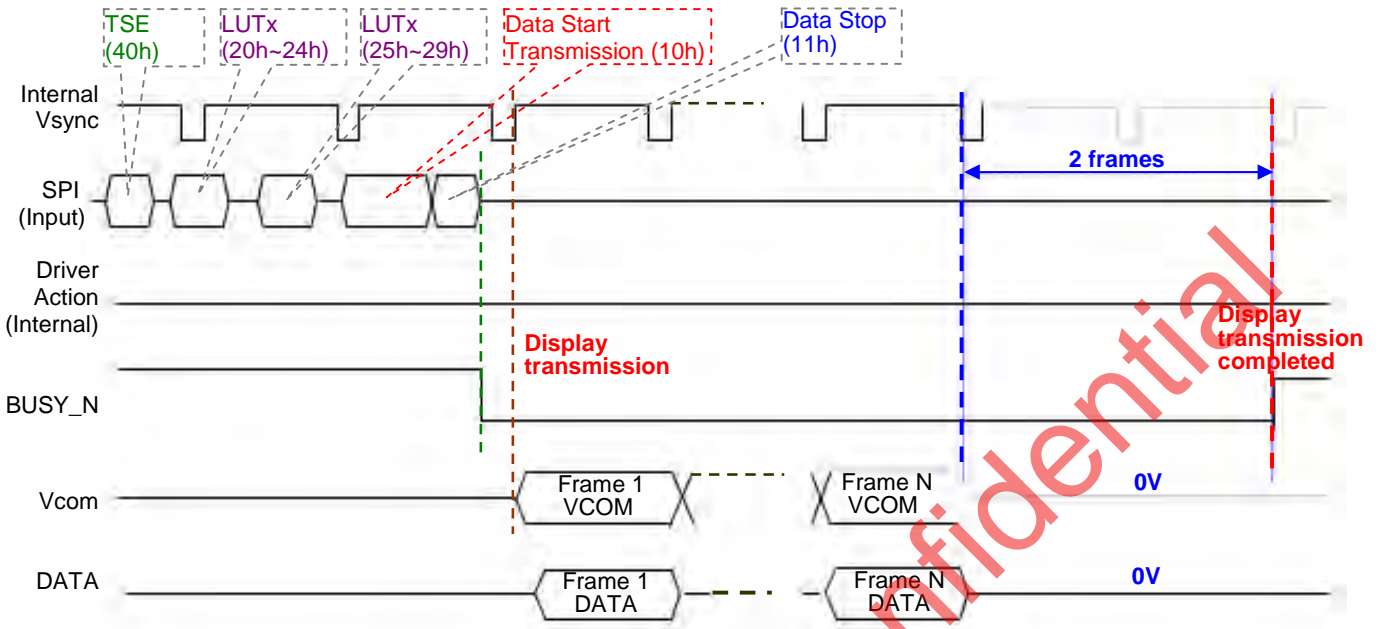


The format of TB0~TB8 is as the below.

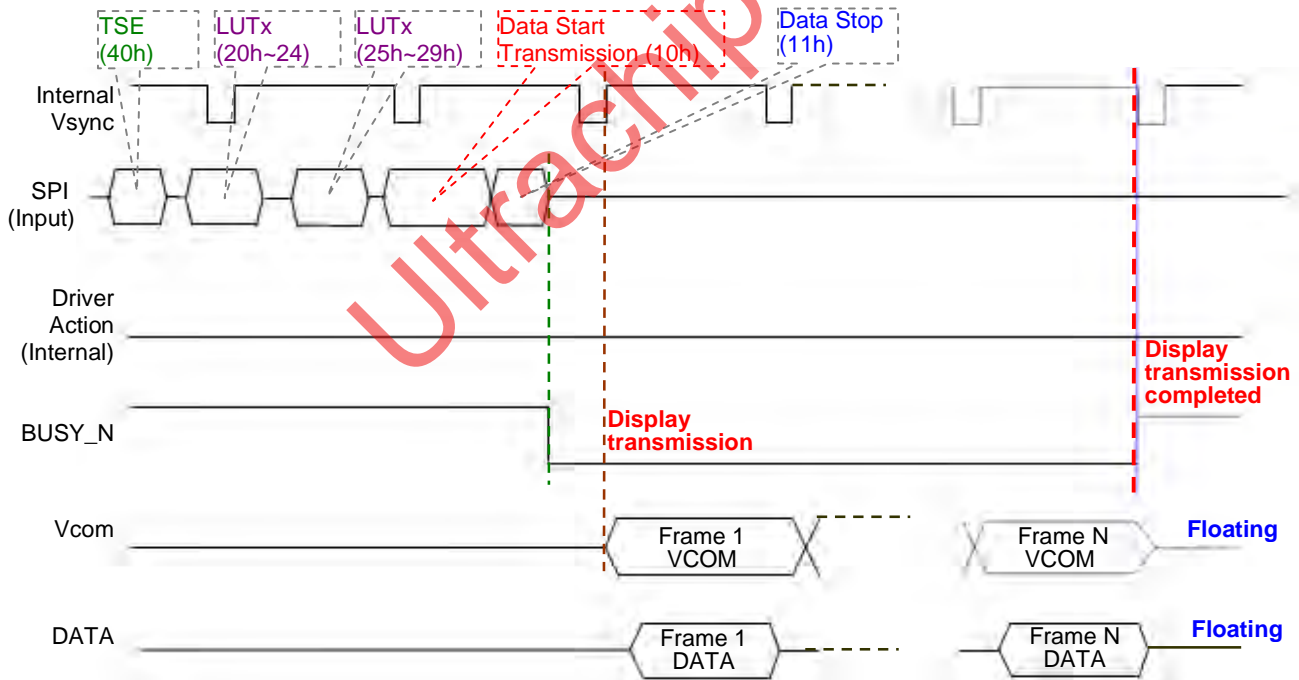
| Bit7-0 | Temperature (°C) |
|------------|------------------|
| 0000 0000b | 0 |
| 0000 0001b | 0.5 |
| 0000 0010b | 1 |
| 0000 0011b | 1.5 |
| : | : |
| 0111 1000b | 60 |

Data Transmission Waveform

Example 1: LUT all states (20 states) complete or phase number=0, the driver will send 2 frames VCOM and data to 0 V.

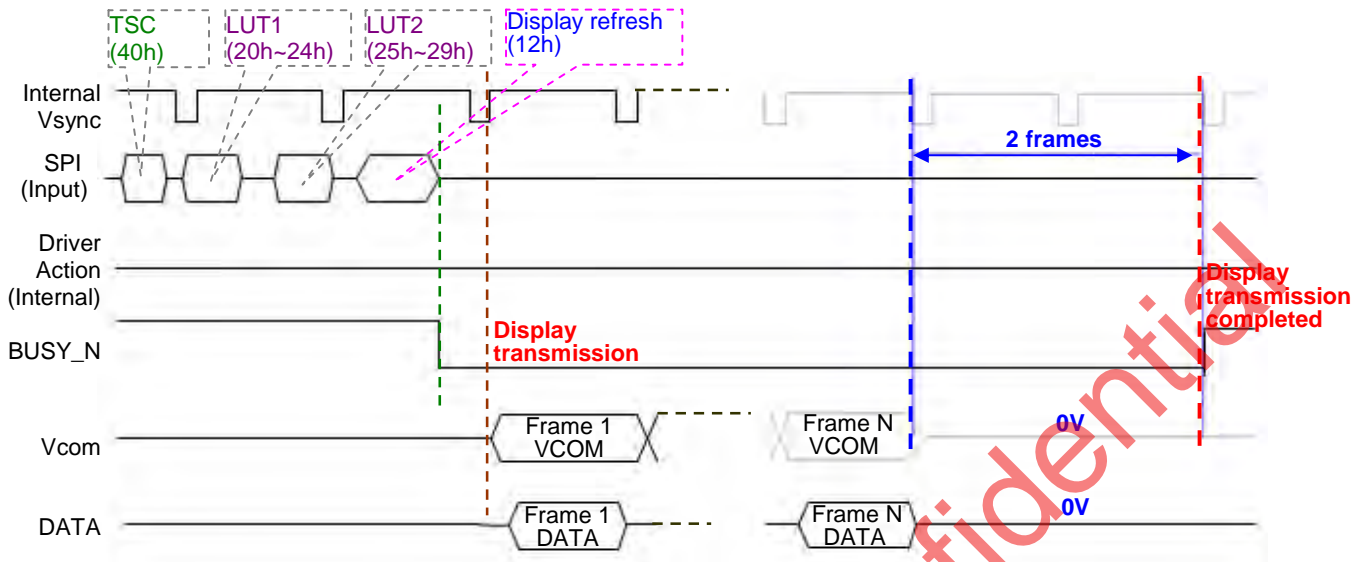


Example 2: While level selection in LUT is "11", the driver will float VCOM and data.

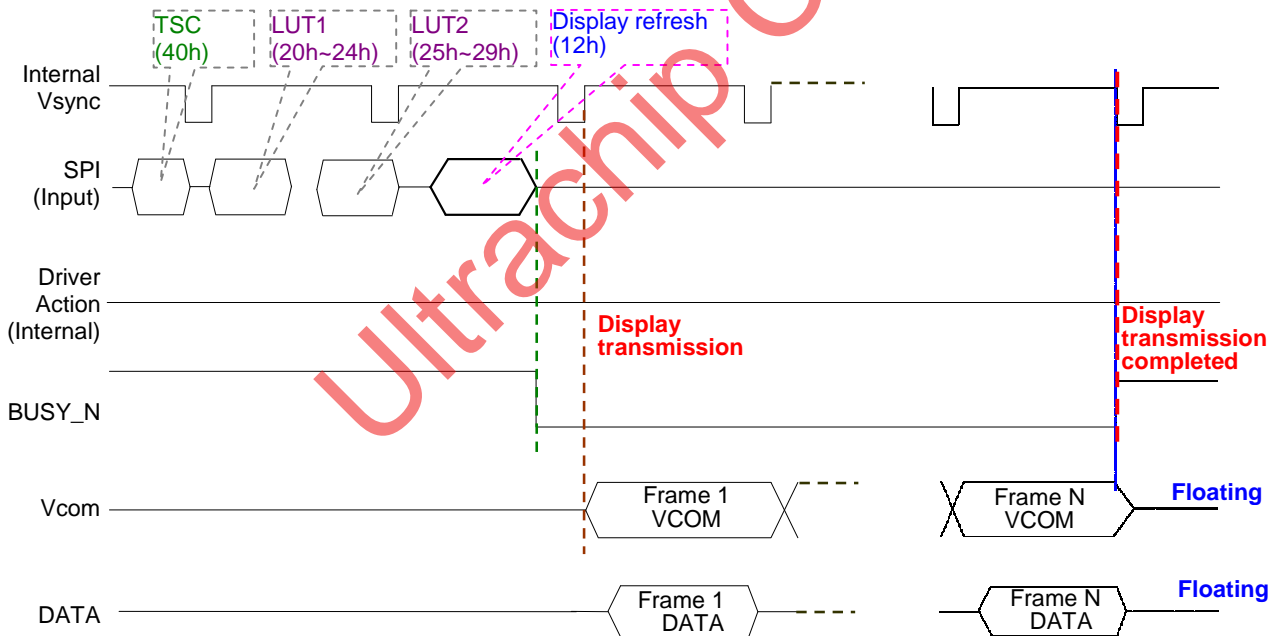


Display Refresh Waveform

Example 1: LUT all states (20 states) complete or phase number=0, the driver will send 2 frames VCOM and data to 0 V.



Example 2: While level selection in LUT is "11", the driver will float VCOM and data.



BUSY_N Signal / Command Restriction

All write commands are "UNAVAILABLE" when BUSY_N=0 asserted by reset, DSP (R11h), DRF (R12h) or IPC (R13h).

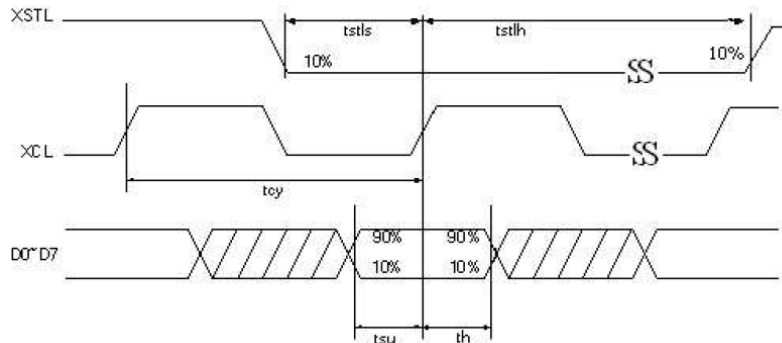
All read commands are always "AVAILABLE" regardless of BUSY_N is 0 or 1.

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Pure Driver Mode

Enable pure driver mode when input pin DEN=1. In pure driver mode, command R01, R02, R03, R04, R61, R82 are still useful.

Source Signal Timing (Clock & data timing)



Data arrangement: Control by command R02H, EDATA_SET bit.

3 bit mode: EDATA_SET=0,

| | D0~7 | | | | | | | |
|-----------|------|------------|------|------|------|----------|------|------|
| | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
| 1st Data | - | Pixel 1 | | | - | Pixel 2 | | |
| 2nd Data | - | Pixel 3 | | | - | Pixel 4 | | |
| ... | - | | | | - | | | |
| N-th Data | - | Pixel 2N-1 | | | - | Pixel 2N | | |

If SHL=1, pixel 1 is output to S0, pixel 2 is output to S1, and so on.

If SHL=0, pixel 1 is output to Sn-1, pixel 2 is output to Sn-2, and so on.

And each pixel level selection:

| Pixel bit | Level selection |
|-----------|-----------------|
| 000 | 0v. |
| 001 | 15v. (VSH). |
| 010 | -15v. (VSL). |
| 011 | VSH_LV |
| 100 | VSL_LV |
| 101 | VSH_LVX |
| 110 | VSL_LVX |
| 111 | Floating. |

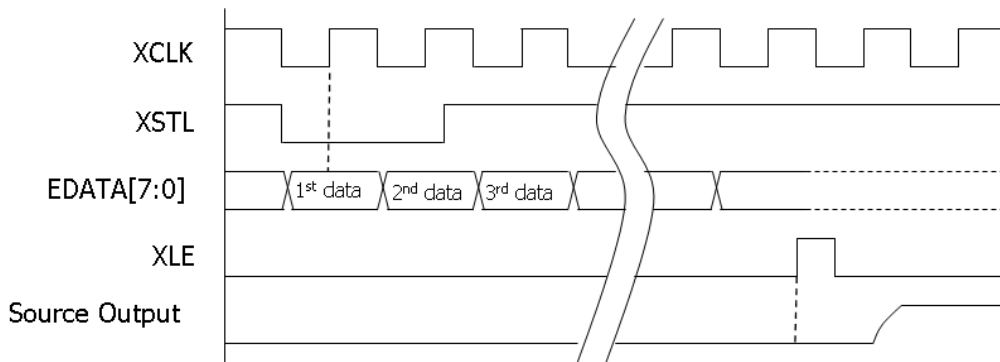
2 bit mode: EDATA_SET=1,

| | D0~7 | | | | | | | |
|-----------|------------|------|------------|------|------------|------|----------|------|
| | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
| 1st Data | Pixel 1 | | Pixel 2 | | Pixel 3 | | Pixel 4 | |
| 2nd Data | Pixel 5 | | Pixel 6 | | Pixel 7 | | Pixel 8 | |
| ... | - | | | | - | | | |
| N-th Data | Pixel 4N-3 | | Pixel 4N-2 | | Pixel 4N-1 | | Pixel 4N | |

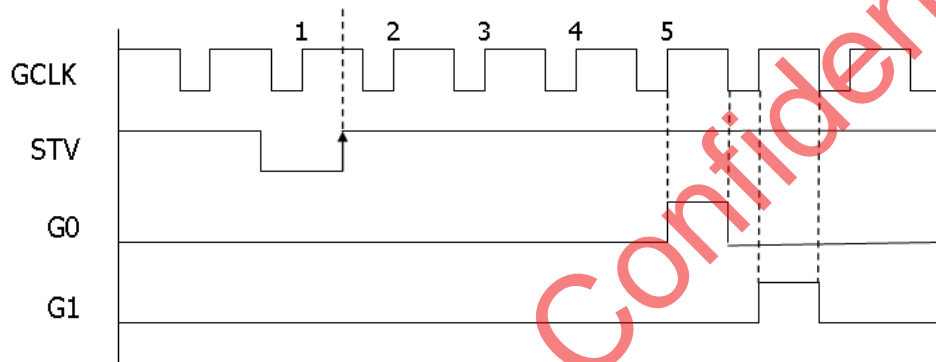
| Pixel bit | Level selection |
|-----------|------------------|
| 00 | 0v. |
| 01 | 15v. (VSH). |
| 10 | -15v. (VSL). |
| 11 | VSH_LV or VSL_LV |

The level selection of "pixel bit =11" is define by EDATA_SEL bit (R01 command), voltage level output VSH_LV when EDATA_SEL=0, output VSL_LV when EDATA_SEL=1.

Output latch control signal

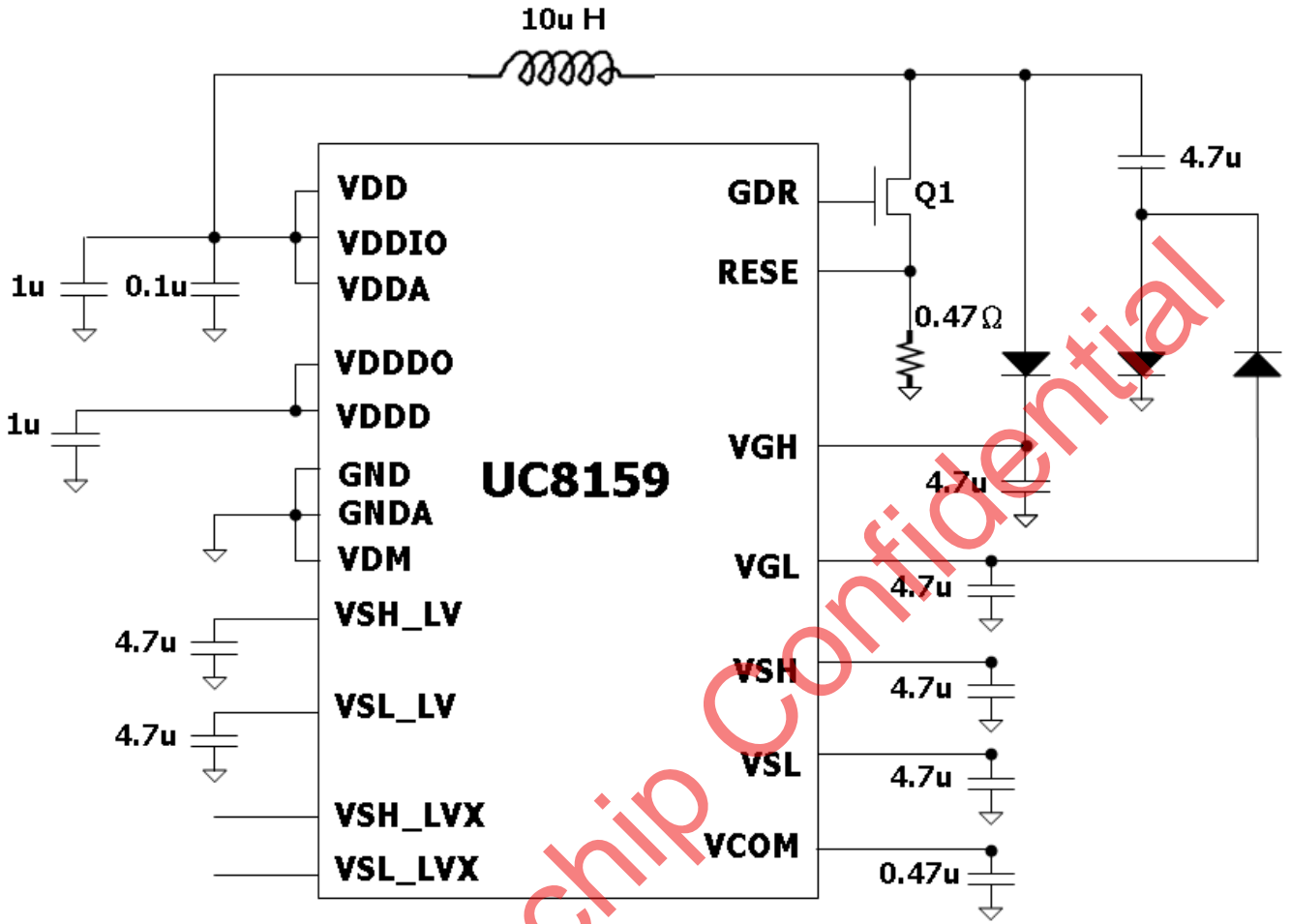


Gate Signal Timing



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Booster Application Circuit



Recommended Device:

- (1) NMOS Switch Q1: ROHM RUF015N02 ($V_{DS} \geq 20V$, $I_D \geq 1.2A$, $V_{GS(TH)} < 1.5V$, $R_{DS(ON)} < 350m\Omega$)
- (2) Schottky Diode: OnSemi MBR0530 ($V_R \geq 20V$, $I_F \geq 500mA$, $I_R < 1mA$)

ABSOLUTE MAXIMUM RATINGS

| Signal | Item | Min | Max. | Unit |
|------------------|-----------------------------------|----------|-----------|------|
| VDD, VDDA, VDDIO | Logic Supply voltage | +2.3 | +3.6 | V |
| Vi | Digital input range | -0.3 | VDDIO+0.3 | V |
| VGH-VGL | Supply range | VGH-0.3 | VGL+0.3 | V |
| Source | | | | |
| VSH | Analog supply voltage – positive | +15 | | V |
| VSL | Analog supply voltage – negative | -15 | | V |
| VSH_LV | Analog supply voltage – positive | +3 ~ +15 | | V |
| VSL_LV | Analog supply voltage – negative | -3 ~ -15 | | V |
| Gate | | | | |
| VGH | Analog supply voltage – positive | -17 | +20 | V |
| VGL | Analog supply voltage -- negative | -17 | -20 | V |
| IVGH | Input rush current for VGH | (TBD) | (TBD) | mA |
| IVGL | Input rush current for VGL | (TBD) | (TBD) | mA |
| TSTG | Storage temperature range | -55 | +125 | °C |

Warning:

If ICs are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

| DC CHARACTERISTICS | | | | | | |
|--------------------|----------------------------|---|-----------|------|-----------|------|
| Symbol | Parameter | Conditions | MIN. | TYP. | MAX. | Unit |
| VDDIO | IO supply voltage | | 2.3 | 3.3 | 3.6 | V |
| VDD | Supply voltage | | 2.3 | 3.3 | 3.6 | V |
| VDDA | DCDC driver supply voltage | | 2.3 | 3.3 | 3.6 | V |
| VDDD | Supply voltage | | | 1.8 | | |
| VIH | HIGH Level input voltage | Digital input pins | 0.8xVDDIO | -- | VDDIO | V |
| VIL | LOW Level input voltage | Digital input pins | GND | -- | 0.2xVDDIO | V |
| VOH | HIGH Level output voltage | Digital output pins, IOH=400uA | 0.8xVDDIO | -- | -- | V |
| VOL | LOW Level Output voltage | Digital output pins, IOL=-400uA | GND | -- | 0.2xVDDIO | V |
| IIN | Input leakage current | Digital input pins except pull-up, pull-down pin | -1.0 | -- | 1.0 | uA |
| RIN | Pull-up/down impedance | | | 200 | | KΩ |
| IVDD | Digital deep sleep current | VDDD OFF | -- | 0.1 | -- | uA |
| | Digital stand-by current | VDD=3.3V, all stopped | -- | 0.5 | 2.0 | uA |
| | Digital operating current | VDD=3.3V | | | | uA |
| IVDDIO | IO deep sleep current | VDDD OFF | | 0.4 | 1.0 | uA |
| | IO stand-by current | VDDIO=3.3V, all stopped | | -- | 0.2 | uA |
| | IO operating current | VDDIO=3.3V | | | | uA |
| IVDDA | Analog deep sleep current | all stopped (power off mode) | | 0.3 | | uA |
| | Analog stand-by current | VDDA=3.3V, all stopped | | | | uA |
| | Analog operating current | VDDA=3.3V DC/DC ON No waveform output, fcdc=250kHz, External cap :415pF NMOS=340pF, No load | | -- | 2 | mA |
| Top | Operating temperature | | -30 | | 85 | °C |

Note: TYP. and MAX. values are to be confirmed by design.

| ANALOG DC CHARACTERISTICS | | | | | | |
|---------------------------|---|--|------|------|---------|------|
| Symbol | Parameter | Conditions | MIN. | TYP. | MAX. | Unit |
| VSH | Supply Voltage | For source driver/VCOM | | 15 | | V |
| dVSH | Supply voltage deviation | | -300 | 0 | +300 | mV |
| VSL | Supply Voltage | For source driver/VCOM | | -15 | | V |
| dVSL | Supply voltage deviation | | -300 | 0 | +300 | mV |
| Idd | Analog Operating Current | No load, | | TBD | | mA |
| Vvd | Voltage Deviation of Outputs | | -- | ±16 | ±35 | mV |
| Vdr | Dynamic Range of Output | | 0.1 | -- | VSH-0.1 | V |
| VGH-VGL | Voltage Range of VGH - VGL | | 12 | | 40 | V |
| VGL | VGL voltage Range | For gate driver | -20 | | -18 | V |
| dVGL | VGL Supply voltage dev | | -400 | 0 | +400 | mV |
| VGH | VGH voltage Range | For gate driver | 20 | | 22 | V |
| dVGH | VGH Supply voltage dev | | -400 | 0 | +400 | mV |
| IstVSH | Positive HV Stand-by Current (power off mode) | Include VSH power With load | - | 0 | 0.01 | µA |
| IVSH | Positive HV Operating Current | Include VSH power With load all SD=L VCOM external resistor divider not included | - | 0.7 | 1.1 | mA |
| | | Include VSH power With load all SD=H VCOM external resistor divider not included | - | 0.8 | 1.2 | mA |
| IstVSL | Negative HV Stand-by Current (power off mode) | Include VSL power With load | - | 0 | 0.01 | µA |
| IVSL | Negative HV Operating Current | Include VSL power With load all SD=L | - | 0.8 | 1.2 | mA |
| | | Include VSL power With load all SD=H | - | 0.9 | 1.3 | mA |

Note: TYP. and MAX. values are to be confirmed by design.

AC CHARACTERISTICS

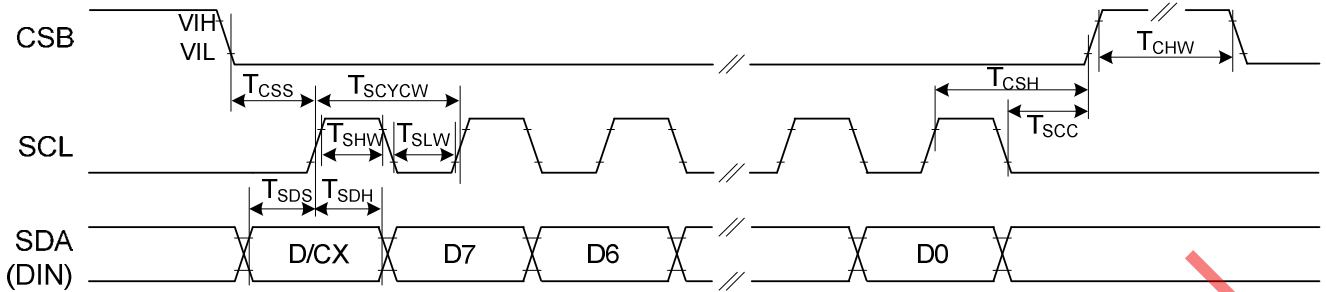


Figure: 3-wire Serial Interface Characteristics (Write mode)

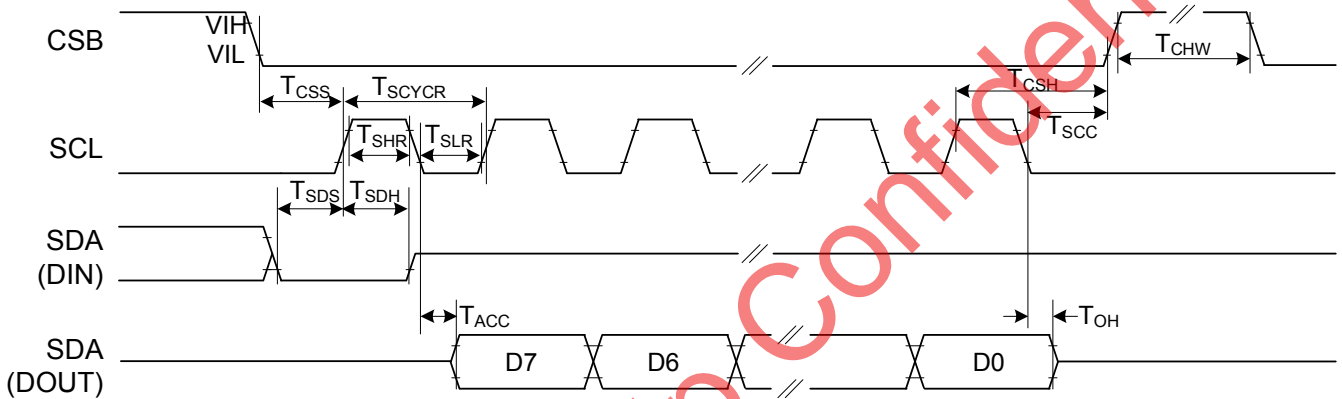


Figure: 3-wire Serial Interface Characteristics (Read mode)

| Symbol | Signal / Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-------------|--------------------|-----------------------------|------|------|------|------|
| T_{CSS} | CSB | Chip select setup time | 60 | | | ns |
| T_{CSH} | | Chip select hold time | 65 | | | ns |
| T_{SCC} | | Chip select setup time | 20 | | | ns |
| T_{CHW} | | Chip select setup time | 40 | | | ns |
| T_{SCYCW} | SCL | Serial clock cycle (Write) | 100 | | | ns |
| T_{SHW} | | SCL "H" pulse width (Write) | 35 | | | ns |
| T_{SLW} | | SCL "L" pulse width (Write) | 35 | | | ns |
| T_{SCYCR} | | Serial clock cycle (Read) | 150 | | | ns |
| T_{SHR} | | SCL "H" pulse width (Read) | 60 | | | ns |
| T_{SLR} | | SCL "L" pulse width (Read) | 60 | | | ns |
| T_{SDS} | SDA (DIN) | Data setup time | 30 | | | ns |
| T_{SDH} | | Data hold time | 30 | | | ns |
| T_{ACC} | SDA | Access time | | | 50 | ns |
| T_{OH} | SDA (DOUT) | Output disable time | 15 | | | ns |

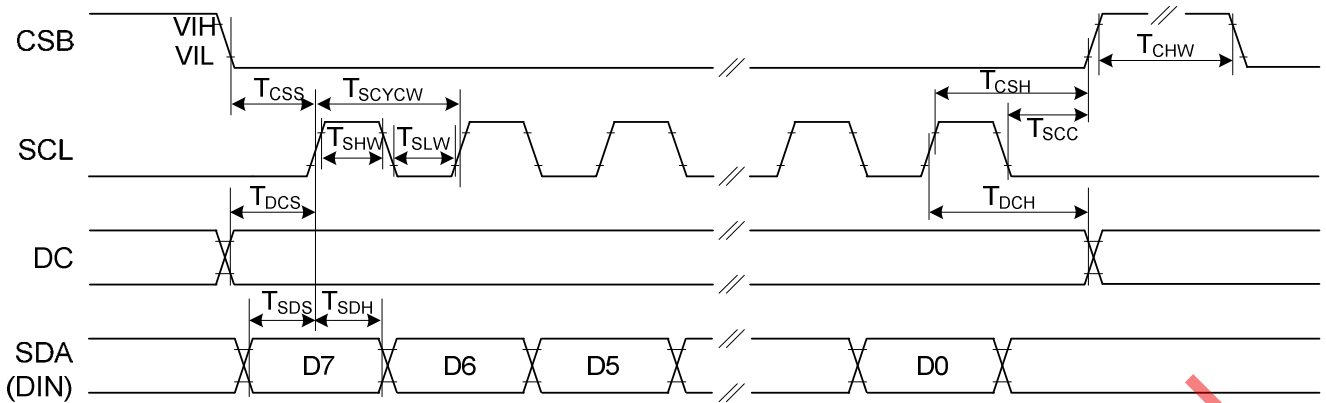


Figure: 4-wire Serial Interface Characteristics (Write mode)

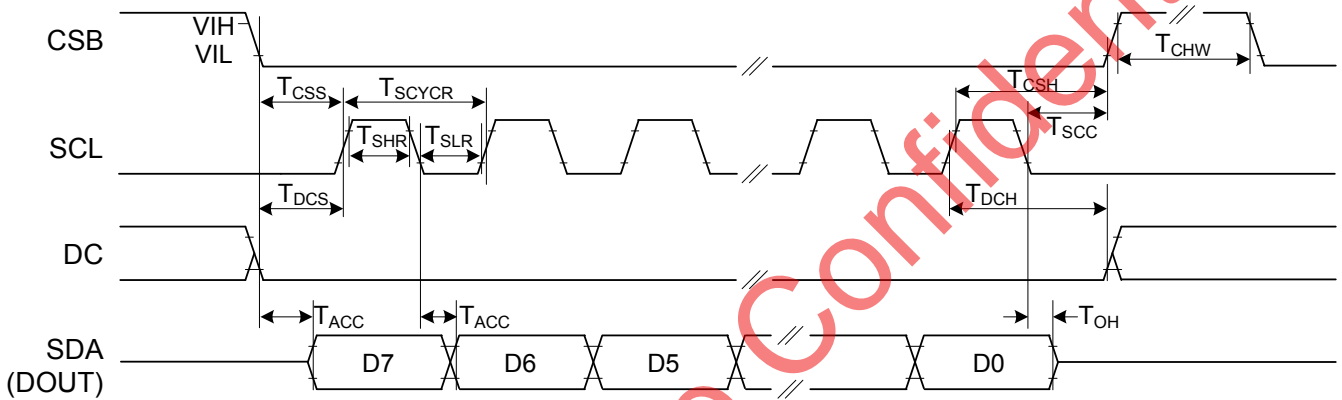
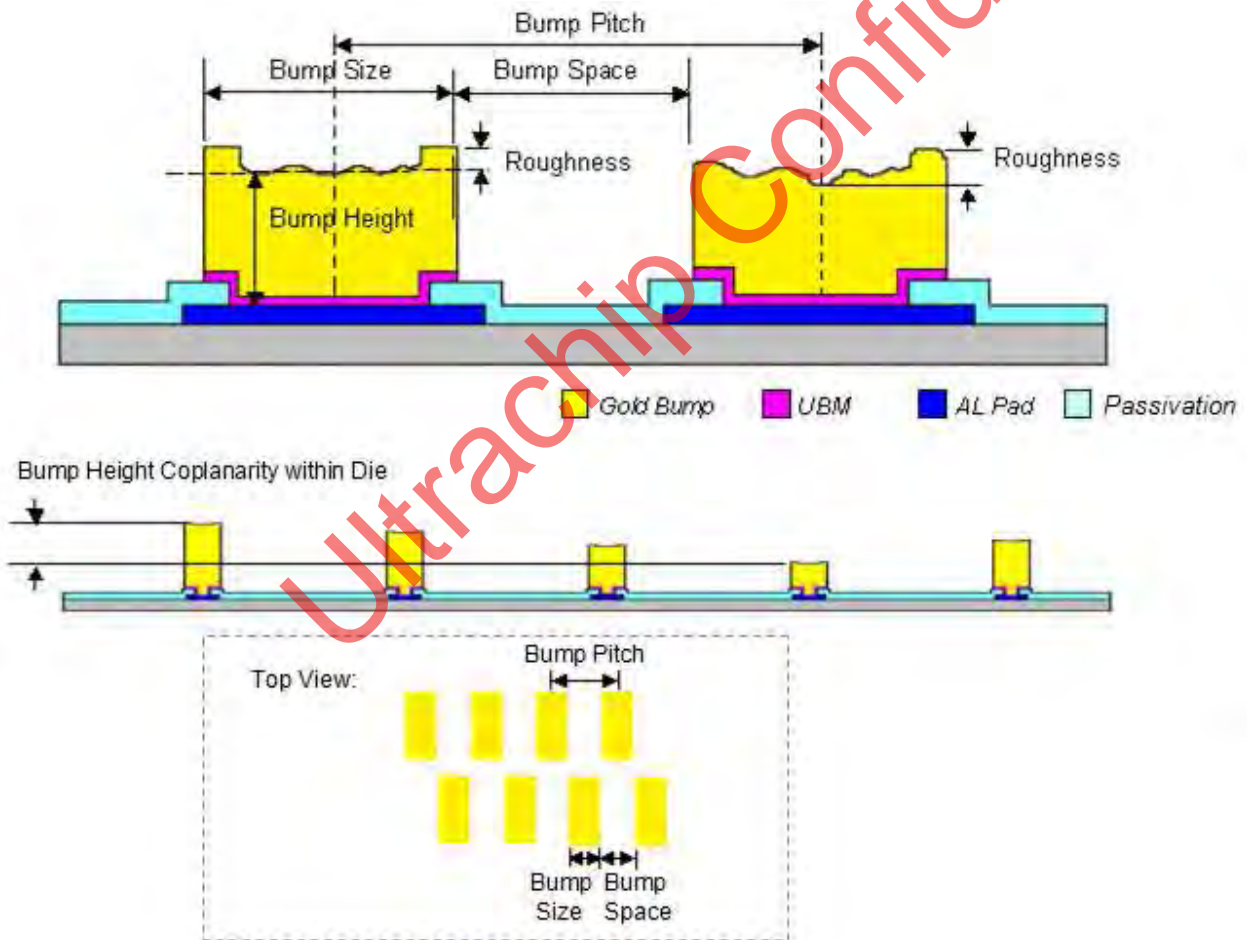


Figure: 4-wire Serial Interface Characteristics (Read mode)

| Symbol | Signal / Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-------------|--------------------|-----------------------------|------|------|------|------|
| T_{CSS} | CSB | Chip select setup time | 60 | | | ns |
| T_{CSH} | | Chip select hold time | 65 | | | ns |
| T_{SCC} | | Chip select setup time | 20 | | | ns |
| T_{CHW} | | Chip select setup time | 40 | | | ns |
| T_{SCYCW} | SCL | Serial clock cycle (Write) | 100 | | | ns |
| T_{SHW} | | SCL "H" pulse width (Write) | 35 | | | ns |
| T_{SLW} | | SCL "L" pulse width (Write) | 35 | | | ns |
| T_{SCYCR} | | Serial clock cycle (Read) | 150 | | | ns |
| T_{SHR} | | SCL "H" pulse width (Read) | 60 | | | ns |
| T_{SLR} | | SCL "L" pulse width (Read) | 60 | | | ns |
| T_{DCS} | DC | DC setup time | 30 | | | ns |
| T_{DCH} | | DC hold time | 30 | | | ns |
| T_{SDS} | SDA (DIN) | Data setup time | 30 | | | ns |
| T_{SDH} | | Data hold time | 30 | | | ns |
| T_{ACC} | SDA (DOUT) | Access time | | | 50 | ns |
| T_{OH} | SDA (DOUT) | Output disable time | 15 | | | ns |

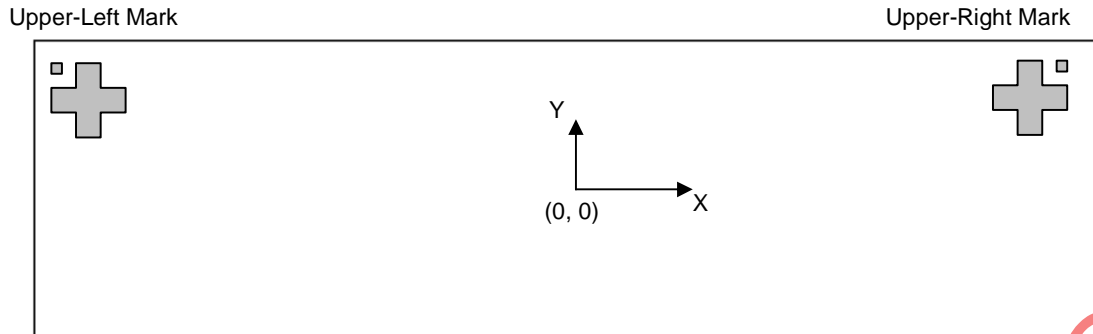
PHYSICAL DIMENSIONS

| | |
|--------------------|---|
| Die Size: | $(17620 \mu\text{M} \pm 40\mu\text{M}) \times (1670 \mu\text{M} \pm 40\mu\text{M})$ |
| Die Thickness: | $180 \mu\text{M} \pm 20\mu\text{M}$ |
| Die TTV: | $(D_{\text{MAX}} - D_{\text{MIN}})$ within die $\leq 2\mu\text{M}$ |
| Bump Height: | $12 \mu\text{M} \pm 3\mu\text{M}$ $(H_{\text{MAX}} - H_{\text{MIN}})$ within die $\leq 2\mu\text{M}$ |
| Hardness: | $65 \text{ Hv} \pm 15\text{Hv}$ |
| Bump Size: | $12 \mu\text{M} \times 100 \mu\text{M} \pm 2\mu\text{M}$ |
| Bump Area: | $1200 \mu\text{M}^2$ |
| Bump Pitch: | $30 \mu\text{M}$ |
| Bump Gap: | $20.38 \mu\text{M} \pm 3\mu\text{M}$ |
| Shear: | $\geq 5\text{g/Mil}^2$ |
| Coordinate origin: | Chip center |
| Pad reference: | Pad center |

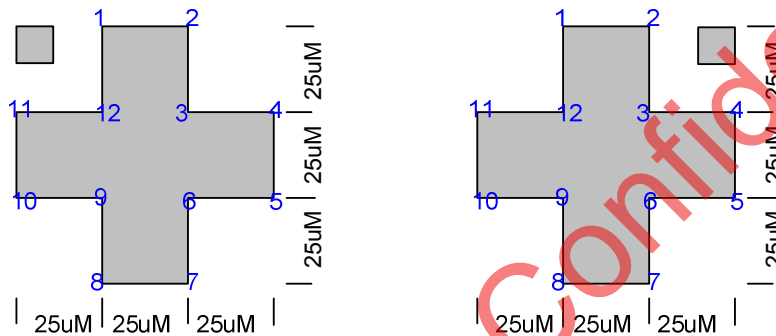


ALIGNMENT MARK INFORMATION

Location:



Shapes and Points:



Point Coordinates:

| Point | Upper-Left Mark | | Upper-Right Mark | |
|--------|-----------------|-------|------------------|-------|
| | X | Y | X | Y |
| Center | -8700 | 725 | 8700 | 725 |
| 1 | -8712.5 | 762.5 | 8687.5 | 762.5 |
| 2 | -8687.5 | 762.5 | 8712.5 | 762.5 |
| 3 | -8687.5 | 737.5 | 8712.5 | 737.5 |
| 4 | -8662.5 | 737.5 | 8737.5 | 737.5 |
| 5 | -8662.5 | 712.5 | 8737.5 | 712.5 |
| 6 | -8687.5 | 712.5 | 8712.5 | 712.5 |
| 7 | -8687.5 | 687.5 | 8712.5 | 687.5 |
| 8 | -8712.5 | 687.5 | 8687.5 | 687.5 |
| 9 | -8712.5 | 712.5 | 8687.5 | 712.5 |
| 10 | -8737.5 | 712.5 | 8662.5 | 712.5 |
| 11 | -8737.5 | 737.5 | 8662.5 | 737.5 |
| 12 | -8712.5 | 737.5 | 8687.5 | 737.5 |

PAD COORDINATES

| No. | Name | X | Y | W | H |
|-----|---------|-------|------|----|----|
| 1 | DUMMY | -8610 | -755 | 40 | 50 |
| 2 | VCOM | -8550 | -755 | 40 | 50 |
| 3 | VCOM | -8490 | -755 | 40 | 50 |
| 4 | VCOM | -8430 | -755 | 40 | 50 |
| 5 | VCOM | -8370 | -755 | 40 | 50 |
| 6 | VCOM | -8310 | -755 | 40 | 50 |
| 7 | VCOM | -8250 | -755 | 40 | 50 |
| 8 | VCOM | -8190 | -755 | 40 | 50 |
| 9 | VCOM | -8130 | -755 | 40 | 50 |
| 10 | PATH1 | -8070 | -755 | 40 | 50 |
| 11 | VDM | -8010 | -755 | 40 | 50 |
| 12 | VDM | -7950 | -755 | 40 | 50 |
| 13 | VGL | -7890 | -755 | 40 | 50 |
| 14 | VGL | -7830 | -755 | 40 | 50 |
| 15 | VGL | -7770 | -755 | 40 | 50 |
| 16 | VGL | -7710 | -755 | 40 | 50 |
| 17 | VGL | -7650 | -755 | 40 | 50 |
| 18 | VGL | -7590 | -755 | 40 | 50 |
| 19 | VGL | -7530 | -755 | 40 | 50 |
| 20 | VGL | -7470 | -755 | 40 | 50 |
| 21 | VGL | -7410 | -755 | 40 | 50 |
| 22 | VGL | -7350 | -755 | 40 | 50 |
| 23 | VGL | -7290 | -755 | 40 | 50 |
| 24 | VGL | -7230 | -755 | 40 | 50 |
| 25 | VGL | -7170 | -755 | 40 | 50 |
| 26 | VGL | -7110 | -755 | 40 | 50 |
| 27 | VGL | -7050 | -755 | 40 | 50 |
| 28 | VGL | -6990 | -755 | 40 | 50 |
| 29 | GND | -6930 | -755 | 40 | 50 |
| 30 | VSL | -6870 | -755 | 40 | 50 |
| 31 | VSL | -6810 | -755 | 40 | 50 |
| 32 | VSL | -6750 | -755 | 40 | 50 |
| 33 | VSL | -6690 | -755 | 40 | 50 |
| 34 | VSL | -6630 | -755 | 40 | 50 |
| 35 | VSL | -6570 | -755 | 40 | 50 |
| 36 | VSL | -6510 | -755 | 40 | 50 |
| 37 | VSL | -6450 | -755 | 40 | 50 |
| 38 | VSL | -6390 | -755 | 40 | 50 |
| 39 | VSL | -6330 | -755 | 40 | 50 |
| 40 | GND | -6270 | -755 | 40 | 50 |
| 42 | VSL_LV | -6210 | -755 | 40 | 50 |
| 41 | VSL_LV | -6150 | -755 | 40 | 50 |
| 43 | VSL_LV | -6090 | -755 | 40 | 50 |
| 44 | VSL_LV | -6030 | -755 | 40 | 50 |
| 45 | VSL_LV | -5970 | -755 | 40 | 50 |
| 46 | VSL_LV | -5910 | -755 | 40 | 50 |
| 47 | VSL_LV | -5850 | -755 | 40 | 50 |
| 48 | VSL_LV | -5790 | -755 | 40 | 50 |
| 49 | VSL_LV | -5730 | -755 | 40 | 50 |
| 50 | VSL_LV | -5670 | -755 | 40 | 50 |
| 51 | GND | -5610 | -755 | 40 | 50 |
| 52 | VSL_LVX | -5550 | -755 | 40 | 50 |
| 53 | VSL_LVX | -5490 | -755 | 40 | 50 |
| 54 | VSL_LVX | -5430 | -755 | 40 | 50 |
| 55 | VSL_LVX | -5370 | -755 | 40 | 50 |
| 56 | VSL_LVX | -5310 | -755 | 40 | 50 |
| 57 | VSL_LVX | -5250 | -755 | 40 | 50 |
| 58 | VSL_LVX | -5190 | -755 | 40 | 50 |

| No. | Name | X | Y | W | H |
|-----|---------|-------|------|----|----|
| 59 | VSL_LVX | -5130 | -755 | 40 | 50 |
| 60 | GND | -5070 | -755 | 40 | 50 |
| 61 | VGH | -5010 | -755 | 40 | 50 |
| 62 | VGH | -4950 | -755 | 40 | 50 |
| 63 | VGH | -4890 | -755 | 40 | 50 |
| 64 | VGH | -4830 | -755 | 40 | 50 |
| 65 | VGH | -4770 | -755 | 40 | 50 |
| 66 | VGH | -4710 | -755 | 40 | 50 |
| 67 | VGH | -4650 | -755 | 40 | 50 |
| 68 | VGH | -4590 | -755 | 40 | 50 |
| 69 | VGH | -4530 | -755 | 40 | 50 |
| 70 | VGH | -4470 | -755 | 40 | 50 |
| 71 | VGH | -4410 | -755 | 40 | 50 |
| 72 | VGH | -4350 | -755 | 40 | 50 |
| 73 | GND | -4290 | -755 | 40 | 50 |
| 74 | VSH | -4230 | -755 | 40 | 50 |
| 75 | VSH | -4170 | -755 | 40 | 50 |
| 76 | VSH | -4110 | -755 | 40 | 50 |
| 77 | VSH | -4050 | -755 | 40 | 50 |
| 78 | VSH | -3990 | -755 | 40 | 50 |
| 79 | VSH | -3930 | -755 | 40 | 50 |
| 80 | VSH | -3870 | -755 | 40 | 50 |
| 81 | VSH | -3810 | -755 | 40 | 50 |
| 82 | VSH | -3750 | -755 | 40 | 50 |
| 83 | VSH | -3690 | -755 | 40 | 50 |
| 84 | GND | -3630 | -755 | 40 | 50 |
| 85 | VSH_LV | -3570 | -755 | 40 | 50 |
| 86 | VSH_LV | -3510 | -755 | 40 | 50 |
| 87 | VSH_LV | -3450 | -755 | 40 | 50 |
| 88 | VSH_LV | -3390 | -755 | 40 | 50 |
| 89 | VSH_LV | -3330 | -755 | 40 | 50 |
| 90 | VSH_LV | -3270 | -755 | 40 | 50 |
| 91 | VSH_LV | -3210 | -755 | 40 | 50 |
| 92 | VSH_LV | -3150 | -755 | 40 | 50 |
| 93 | VSH_LV | -3090 | -755 | 40 | 50 |
| 94 | VSH_LV | -3030 | -755 | 40 | 50 |
| 95 | GND | -2970 | -755 | 40 | 50 |
| 96 | VSH_LVX | -2910 | -755 | 40 | 50 |
| 97 | VSH_LVX | -2850 | -755 | 40 | 50 |
| 98 | VSH_LVX | -2790 | -755 | 40 | 50 |
| 99 | VSH_LVX | -2730 | -755 | 40 | 50 |
| 100 | VSH_LVX | -2670 | -755 | 40 | 50 |
| 101 | VSH_LVX | -2610 | -755 | 40 | 50 |
| 102 | VSH_LVX | -2550 | -755 | 40 | 50 |
| 103 | VSH_LVX | -2490 | -755 | 40 | 50 |
| 104 | GND | -2430 | -755 | 40 | 50 |
| 105 | VDDD | -2370 | -755 | 40 | 50 |
| 106 | VDDD | -2310 | -755 | 40 | 50 |
| 107 | VDDD | -2250 | -755 | 40 | 50 |
| 108 | VDDD | -2190 | -755 | 40 | 50 |
| 109 | VDDD | -2130 | -755 | 40 | 50 |
| 110 | VDDD | -2070 | -755 | 40 | 50 |
| 111 | VDDDO | -2010 | -755 | 40 | 50 |
| 112 | VDDDO | -1950 | -755 | 40 | 50 |
| 113 | VDDDO | -1890 | -755 | 40 | 50 |
| 114 | VDDDO | -1830 | -755 | 40 | 50 |
| 115 | VDDDO | -1770 | -755 | 40 | 50 |
| 116 | VDDDO | -1710 | -755 | 40 | 50 |

| No. | Name | X | Y | W | H |
|-----|--------|------|-----|----|-----|
| 597 | S<63> | 3855 | 626 | 12 | 100 |
| 598 | S<64> | 3840 | 751 | 12 | 100 |
| 599 | S<65> | 3825 | 626 | 12 | 100 |
| 600 | S<66> | 3810 | 751 | 12 | 100 |
| 601 | S<67> | 3795 | 626 | 12 | 100 |
| 602 | S<68> | 3780 | 751 | 12 | 100 |
| 603 | S<69> | 3765 | 626 | 12 | 100 |
| 604 | S<70> | 3750 | 751 | 12 | 100 |
| 605 | S<71> | 3735 | 626 | 12 | 100 |
| 606 | S<72> | 3720 | 751 | 12 | 100 |
| 607 | S<73> | 3705 | 626 | 12 | 100 |
| 608 | S<74> | 3690 | 751 | 12 | 100 |
| 609 | S<75> | 3675 | 626 | 12 | 100 |
| 610 | S<76> | 3660 | 751 | 12 | 100 |
| 611 | S<77> | 3645 | 626 | 12 | 100 |
| 612 | S<78> | 3630 | 751 | 12 | 100 |
| 613 | S<79> | 3615 | 626 | 12 | 100 |
| 614 | S<80> | 3600 | 751 | 12 | 100 |
| 615 | S<81> | 3585 | 626 | 12 | 100 |
| 616 | S<82> | 3570 | 751 | 12 | 100 |
| 617 | S<83> | 3555 | 626 | 12 | 100 |
| 618 | S<84> | 3540 | 751 | 12 | 100 |
| 619 | S<85> | 3525 | 626 | 12 | 100 |
| 620 | S<86> | 3510 | 751 | 12 | 100 |
| 621 | S<87> | 3495 | 626 | 12 | 100 |
| 622 | S<88> | 3480 | 751 | 12 | 100 |
| 623 | S<89> | 3465 | 626 | 12 | 100 |
| 624 | S<90> | 3450 | 751 | 12 | 100 |
| 625 | S<91> | 3435 | 626 | 12 | 100 |
| 626 | S<92> | 3420 | 751 | 12 | 100 |
| 627 | S<93> | 3405 | 626 | 12 | 100 |
| 628 | S<94> | 3390 | 751 | 12 | 100 |
| 629 | S<95> | 3375 | 626 | 12 | 100 |
| 630 | S<96> | 3360 | 751 | 12 | 100 |
| 631 | S<97> | 3345 | 626 | 12 | 100 |
| 632 | S<98> | 3330 | 751 | 12 | 100 |
| 633 | S<99> | 3315 | 626 | 12 | 100 |
| 634 | S<100> | 3300 | 751 | 12 | 100 |
| 635 | S<101> | 3285 | 626 | 12 | 100 |
| 636 | S<102> | 3270 | 751 | 12 | 100 |
| 637 | S<103> | 3255 | 626 | 12 | 100 |
| 638 | S<104> | 3240 | 751 | 12 | 100 |
| 639 | S<105> | 3225 | 626 | 12 | 100 |
| 640 | S<106> | 3210 | 751 | 12 | 100 |
| 641 | S<107> | 3195 | 626 | 12 | 100 |
| 642 | S<108> | 3180 | 751 | 12 | 100 |
| 643 | S<109> | 3165 | 626 | 12 | 100 |
| 644 | S<110> | 3150 | 751 | 12 | 100 |
| 645 | S<111> | 3135 | 626 | 12 | 100 |
| 646 | S<112> | 3120 | 751 | 12 | 100 |
| 647 | S<113> | 3105 | 626 | 12 | 100 |
| 648 | S<114> | 3090 | 751 | 12 | 100 |
| 649 | S<115> | 3075 | 626 | 12 | 100 |
| 650 | S<116> | 3060 | 751 | 12 | 100 |
| 651 | S<117> | 3045 | 626 | 12 | 100 |
| 652 | S<118> | 3030 | 751 | 12 | 100 |
| 653 | S<119> | 3015 | 626 | 12 | 100 |
| 654 | S<120> | 3000 | 751 | 12 | 100 |
| 655 | S<121> | 2985 | 626 | 12 | 100 |
| 656 | S<122> | 2970 | 751 | 12 | 100 |

| No. | Name | X | Y | W | H |
|-----|--------|------|-----|----|-----|
| 657 | S<123> | 2955 | 626 | 12 | 100 |
| 658 | S<124> | 2940 | 751 | 12 | 100 |
| 659 | S<125> | 2925 | 626 | 12 | 100 |
| 660 | S<126> | 2910 | 751 | 12 | 100 |
| 661 | S<127> | 2895 | 626 | 12 | 100 |
| 662 | S<128> | 2880 | 751 | 12 | 100 |
| 663 | S<129> | 2865 | 626 | 12 | 100 |
| 664 | S<130> | 2850 | 751 | 12 | 100 |
| 665 | S<131> | 2835 | 626 | 12 | 100 |
| 666 | S<132> | 2820 | 751 | 12 | 100 |
| 667 | S<133> | 2805 | 626 | 12 | 100 |
| 668 | S<134> | 2790 | 751 | 12 | 100 |
| 669 | S<135> | 2775 | 626 | 12 | 100 |
| 670 | S<136> | 2760 | 751 | 12 | 100 |
| 671 | S<137> | 2745 | 626 | 12 | 100 |
| 672 | S<138> | 2730 | 751 | 12 | 100 |
| 673 | S<139> | 2715 | 626 | 12 | 100 |
| 674 | S<140> | 2700 | 751 | 12 | 100 |
| 675 | S<141> | 2685 | 626 | 12 | 100 |
| 676 | S<142> | 2670 | 751 | 12 | 100 |
| 677 | S<143> | 2655 | 626 | 12 | 100 |
| 678 | S<144> | 2640 | 751 | 12 | 100 |
| 679 | S<145> | 2625 | 626 | 12 | 100 |
| 680 | S<146> | 2610 | 751 | 12 | 100 |
| 681 | S<147> | 2595 | 626 | 12 | 100 |
| 682 | S<148> | 2580 | 751 | 12 | 100 |
| 683 | S<149> | 2565 | 626 | 12 | 100 |
| 684 | S<150> | 2550 | 751 | 12 | 100 |
| 685 | S<151> | 2535 | 626 | 12 | 100 |
| 686 | S<152> | 2520 | 751 | 12 | 100 |
| 687 | S<153> | 2505 | 626 | 12 | 100 |
| 688 | S<154> | 2490 | 751 | 12 | 100 |
| 689 | S<155> | 2475 | 626 | 12 | 100 |
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| 723 | S<189> | 1965 | 626 | 12 | 100 |
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| 728 | S<194> | 1890 | 751 | 12 | 100 |
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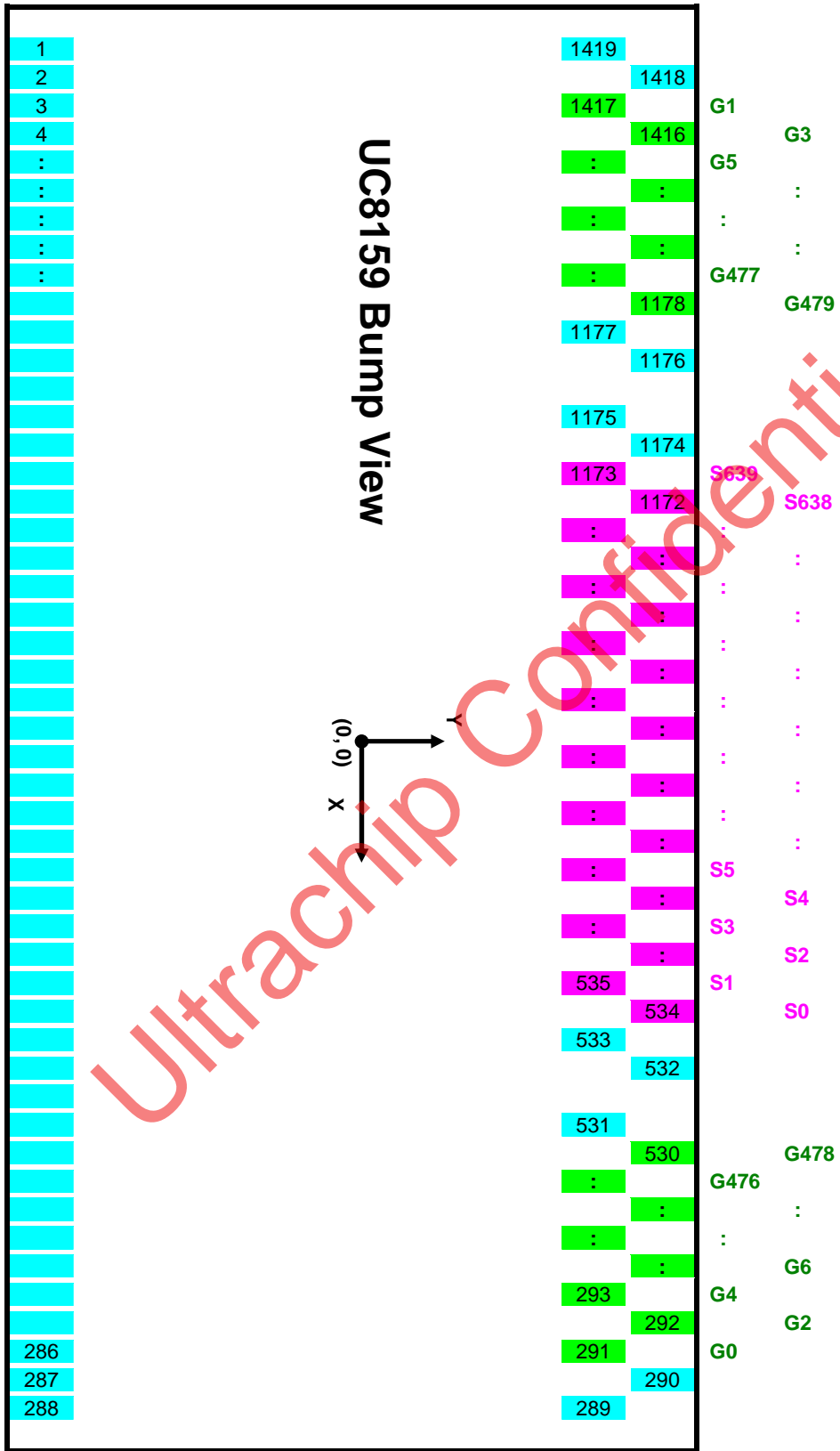
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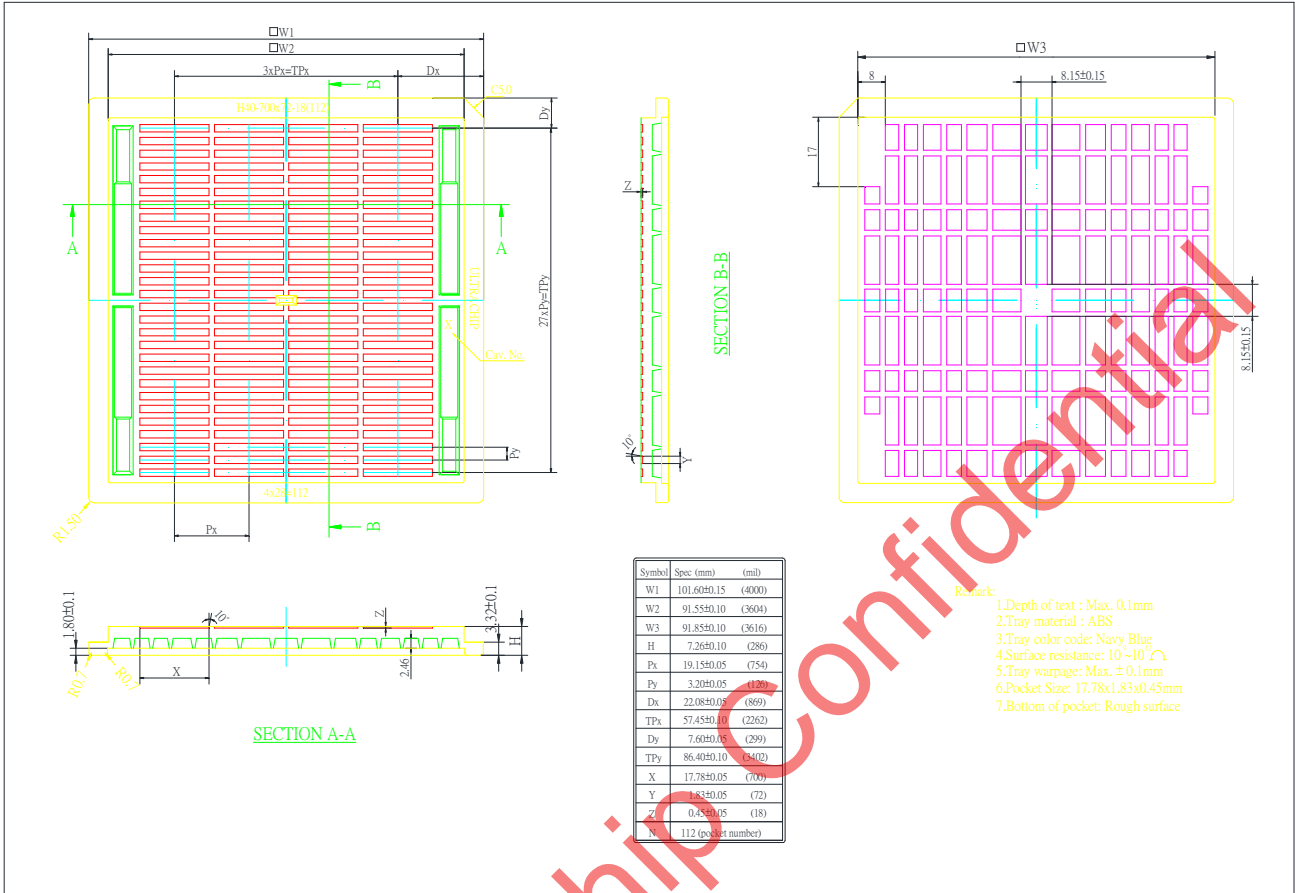
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Output Pad Location :



TRAY INFORMATION



REVISION HISTORY

| Revision | Contents | Date |
|----------|----------|------|
| | (N/A) | |

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